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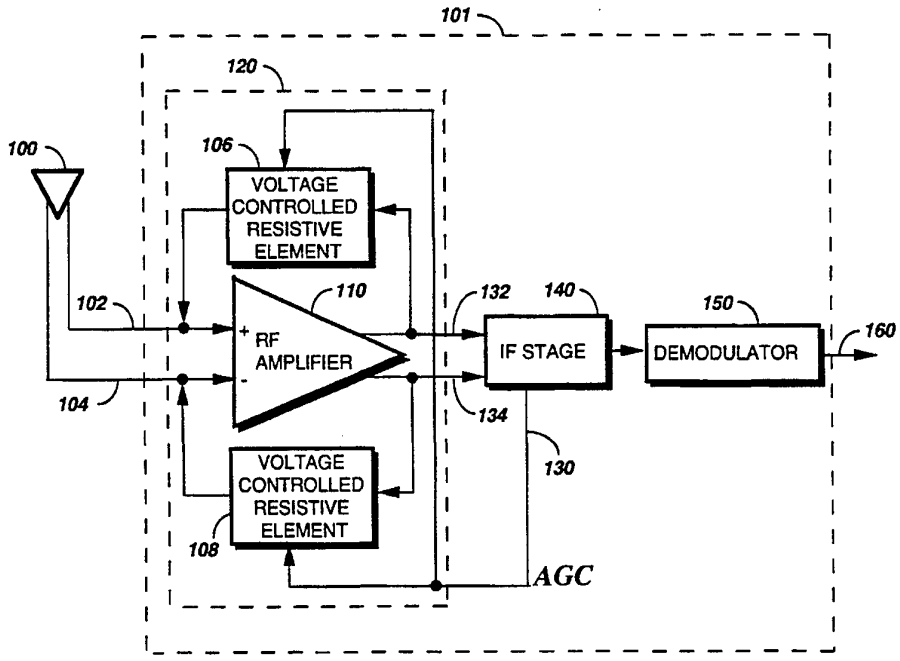

(57) **Abstract**

The radio frequency (RF) receiver (101) comprises an RF amplifier (110), a circuit for producing a control signal (130), and a voltage dependent resistive element (108), coupled between the input and the output of the RF amplifier (110), for controlling the gain of the RF amplifier (110) in response to the control signal (130). The RF amplifier (110) has an amplifier gain and an input (104) for receiving at least one RF input signal and has an output (134) from which at least one RF output signal is generated amplified by the amplifier gain. The control signal (130) varies in response to a received signal strength.

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RADIO FREQUENCY AMPLIFIER WITH VARIABLE GAIN CONTROL

Field of the Invention

This invention relates in general to radio frequency (RF) amplifiers, and in particular to controlled gain RF amplifiers.

BACKGROUND OF THE INVENTION

Many small, portable radio frequency (RF) devices today use bipolar integrated circuit amplifiers to amplify low level received RF input signals into high level, low impedance RF output signals. These circuits need to be integrated to achieve a small product size and low current drain. Low current drain is important to preserve battery life. Cascode and differential neutralized bipolar integrated circuit RF amplifiers are known which will provide the high gain needed to amplify extremely small RF signals into high level RF output signals without adding significant noise and distortion to the output. However, when higher level RF input signals are presented to such amplifier circuits, the amplifier circuits will amplify certain undesirable RF signals in a disproportional manner, causing an output signal with excessive distortion. This undesirable RF signal amplification is common in RF receiving circuits and is characterized and measured as intermodulation (IM) distortion. The amplification of the undesirable signals is due to the non-linear nature of such amplifier circuits.

In an intermediate frequency stage of a receiver section of the RF communicating device, the output of the RF amplifier is typically coupled to subsequent amplifier, filter, and mixer circuits. The subsequent amplifier, filter, and mixer circuits are typically coupled in series to process the RF signal and generate the analog and/or digital information signal at the output of the receiver portion. New, undesirable RF signals are generated within these subsequent circuits in the receiver section of the RF communications device. The subsequent amplifier and mixer circuits exhibit the characteristic of generating IM distortion from these new undesirable RF signals which increases in a manner disproportional to the increase of the input signal to each circuit.

Thus, it can be seen that it is important to both minimize the IM distortion generated within the RF amplifiers and to keep the level of the RF output signal of the RF amplifier at low to moderate levels, even with higher level RF input signals. This will result in a good signal to IM distortion ratio at the output of the receiver.

A known means of reducing the gain of the RF amplifier at higher RF input signal levels is to reduce the amplifier current consumption when the input signal is at the higher levels, using a bipolar transistor circuit. This reduces the RF amplifier gain and the output signal level, but with moderate increase of the signal to IM distortion ratio. This also causes an increase in the noise figure of the RF amplifier, which is another undesirable result.

Another known means of reducing the intermodulation distortion, which has also been used successfully, has been to add a circuit which reduces the input signal level presented to the RF amplifier by reducing the impedance between the input signal and ground as the RF input signal power increases. This method, while effective, also has the drawback of increasing the amplifier's noise figure and can cause increased current drain.

Thus, what is needed is a means to reduce the gain of the RF amplifier and improve the RF output signal to IM distortion ratio when the RF input signal strength is strong. More ideally it is desireable to continuously decrease the gain of the RF amplifier as the received RF signal strength increases, in a manner which does not increase the noise figure or current drain of the RF amplifier, while keeping the signal to IM distortion ratio good.

SUMMARY OF THE INVENTION

Accordingly, in a first embodiment of the present invention a radio frequency (RF) receiver comprises an RF amplifier, means for producing a control signal which varies in response to a received signal strength, and a voltage dependent resistive element, coupled between the input and the output of the RF amplifier, for controlling the gain of the RF amplifier in response to the control signal. The RF amplifier has an amplifier gain and an input for receiving at least one RF input signal and

an output from which at least one RF output signal is generated amplified by the amplifier gain.

In a second embodiment of the present invention a radio frequency communications device comprises an antenna, an RF receiver, a decoder, and presentation means. The antenna is coupled to the RF receiver which comprises an amplifier, means for producing a control signal which varies in response to a received signal strength, a voltage dependent resistive element, and means for processing the RF output of the RF amplifier and demodulating the processed signal. The RF amplifier has an amplifier gain and an input for receiving at least one RF input signal and has an output from which at least one RF output signal is generated amplified by the amplifier gain. The voltage dependent resistive element is coupled between the input and the output of the RF amplifier and controls the gain of the RF amplifier in response to the control signal. The decoder decodes the demodulated signal to generate information. The information generated in response to the decoded signal is presented by the presentation means.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is an electrical block diagram of a radio frequency (RF) receiver in accordance with a first embodiment of the present invention.

FIG. 2 is a graph showing the level of the intermodulation distortion generated in a typical RF amplifier.

FIG. 3 is a graph of the output level of received signal strength versus the input signal strength of an RF amplifier having gain control in accordance with the embodiment of the present invention.

FIG. 4 is an electrical block diagram of an RF receiver in accordance with a second embodiment of the present invention.

FIG. 5 is an electrical block diagram of an RF receiver in accordance with a third embodiment of the present invention.

FIG. 6 is an electrical block diagram of an RF receiver in accordance with a fourth embodiment of the present invention.

FIG. 7 is an electrical schematic diagram of a bipolar transistor/field effect transistor (FET) cascode differential RF amplifier suitable for use in the RF receivers of FIG. 1 or FIG. 4.

FIG. 8 is an electrical schematic diagram of a neutralized bipolar transistor differential RF amplifier suitable for use in the RF receivers of FIG. 1 or FIG. 4.

FIG. 9 is an electrical schematic diagram of a bipolar transistor cascode single ended RF amplifier suitable for use in the RF receivers of FIG. 5 or FIG. 6.

FIG. 10 is an electrical block diagram of an RF communications device utilizing any one of the RF receivers in accordance with the embodiments of the present invention shown in FIG. 1, FIG. 4, FIG. 5, or FIG. 6.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1, an electrical block diagram of a radio frequency (RF) receiver 101 in accordance with a first embodiment of the present invention is shown. An antenna 100 having differential outputs 102 and 104 is coupled to inputs of the RF receiver 101. The RF receiver 101 comprises a differential RF amplifier stage 120, an intermediate frequency (IF) stage 140 and a demodulator 150. The differential RF amplifier stage 120 accepts and processes the antenna output signals 102 and 104 in a manner which will be described below. Outputs 132 and 134 of the differential RF amplifier stage 120 are coupled to inputs of the IF stage 140 which processes the signal in a manner well known in the art e.g., to remove unwanted RF signals that are received at antenna 100 and amplified in the differential RF amplifier stage 120. An output of the IF stage 140 is coupled to an input of the demodulator 150 which demodulates the signal in a manner well known in the art e.g., to remove the RF portion of the signal and generate an analog and/or digital information portion of the signal 160. Within the IF stage 140, a signal substantially proportional to the logarithm of the received signal strength is also produced at output 130 using a signal strength detecting circuit, such as a received signal strength indicating (RSSI) circuit. The signal generated at output 130 is coupled to an automatic gain control (AGC) input of the differential RF amplifier stage 120.

Referring back to FIG. 1, the differential RF amplifier stage 120 comprises a differential RF amplifier 110 and two voltage dependent resistive elements 106 and 108 integrated using a bipolar and

complementary metal oxide semiconductor (BiCMOS) technology, as will be described below. The AGC input 130 of the differential RF amplifier stage 120 is coupled to control inputs of the voltage dependent resistive elements 106 and 108. The outputs of the differential RF amplifier 110 are coupled to the signal input of each of the voltage dependent resistive elements 106 and 108 and the signal output of each of the voltage dependent resistive elements is coupled to a corresponding input of the differential RF amplifier 110. Other portions of the RF receiver 101 may be also integrated and manufactured using BiCMOS circuit devices.

Referring to FIG. 2, an example from an article entitled "receiver noise figure sensitivity and dynamic range - what the numbers mean" by author James R. Fisk, published in Ham Radio, October 1975, page 20 is depicted, showing the intermodulation distortion caused by the non-linear amplification of the input signal levels of an RF amplifier that does not have reduced gain with higher input signal levels. Two curves are shown: Curve 170 represents the amplified input signal level without the intermodulation distortion, and curve 172 represents the intermodulation distortion signal level. The total output signal level of the amplifier is the sum of these two signals.

Referring to FIG. 3, Curve 174 shows the amount of gain reduction that would cause the RF amplifier of FIG. 2 to operate with its output level reduced significantly at the higher input levels, thereby avoiding the disproportional rise of intermodulation distortion. Curve 176 illustrates typical control signal voltage levels that would be expected from a received signal strength indicator (RSSI) circuit. An appropriate voltage dependent resistive element which is controlled by a signal such as that shown in curve 176 produces the gain reduction shown in curve 174.

For example, if the amplifier of FIG. 2 were given an input signal level of +10 dBm, the output signal level would be +5 dBm and the intermodulation distortion would be at -40 dBm, or a signal to noise ratio of approximately 45 dB. With the gain reduction shown in FIG. 3, and with the same input signal level of +10dBm, the output signal would be reduced by 27dB to -17dBm and the associated intermodulation distortion would be -102dBm. This results in a much better signal to noise ratio of 85dB and a lower RF output signal. This is the type of improvement exemplary by use of any of the embodiments of the present invention

and it is accomplished without the negative side affects of either increased noise figure or increased current drain as found in the prior art.

Referring to FIG. 4, an electrical block diagram of an RF receiver 101 in accordance with a second embodiment of the present invention is shown. The RF receiver 101 is the same as described above for the block diagram in FIG. 1, but with the AGC signal 130 being generated from a separate RF signal strength detector circuit 250. The RF signal strength detector circuit 250 accepts as inputs the differential signals 102 and 104 from the output of antenna 100. The RF signal strength detector circuit 250 generates a signal substantially proportional to the logarithm of received signal strength at the output 130 which is then coupled to the AGC input of the differential RF amplifier stage 120, as shown.

The differential RF amplifier stage 120 comprises the same elements as those described above for the electrical block diagram in FIG. 1

Referring to FIG. 5, an electrical block diagram of an RF receiver 301 in accordance with a third embodiment of the present invention is shown. In this case, an antenna 300 produces a single ended (unbalanced) output 302, as contrasted to the differential (balanced) outputs 132 and 134 in FIG. 1 and FIG. 4. The antenna output signal is coupled to input 302 of the single ended RF amplifier stage 320. A single ended output 324 of the single ended RF amplifier stage 320 is coupled to the input of an IF stage 340 which in all respects is the same as IF stage 140 in FIG. 1, other than accepting a single ended input 324 as contrasted to accepting differential inputs 132 and 134 as in FIG. 1. The AGC signal is coupled to the automatic gain control (AGC) input 130 of the single ended RF amplifier stage 320.

In this third embodiment of the present invention, the single ended RF amplifier stage 320 comprises a single ended RF amplifier 310 and one voltage dependent resistive element 108 integrated in BiCMOS technology, as will be described below. The AGC input 130 of the single ended RF amplifier stage 320 is coupled to a control input of the voltage dependent resistive element 108. The output of the single ended RF amplifier 310 is coupled to the signal input of the voltage dependent resistive element 108 and the signal output of the voltage dependent resistive element is coupled to the input of the amplifier 310.

Referring to FIG. 6, an electrical block diagram of a RF receiver 301 in accordance with a fourth embodiment of the present invention is

shown. The RF receiver 301 is the same as described above for the block diagram in FIG. 5 but with the AGC signal 130 being generated from a separate RF signal strength detector circuit 450 as described above for the block diagram in FIG. 4, except having a single ended input.

The single ended RF amplifier stage 320 comprises the same elements as those described above for the block diagram in FIG. 5.

Referring to FIG. 7, an electrical schematic diagram of a differential RF amplifier 120 suitable for use in the RF receiver 101 of FIG. 1 or FIG. 4 is shown. Differential RF amplifier 120 comprises a bipolar transistor/field effect transistor (FET) cascode differential RF amplifier 110 and voltage dependent resistive elements 106 and 108.

A first differential input 102 is coupled to one terminal of a capacitor 503. The other terminal of capacitor 503 is coupled to the base of a bipolar NPN transistor 514 and the source 550 of a p-channel FET 530. A second differential input 104 is coupled to a first terminal of capacitor 505. The other terminal of capacitor 505 is coupled to the base of a bipolar NPN transistor 516 and the source 552 of a p-channel FET 540. The collector of NPN transistor 514 is coupled to the source 523 of a n-channel FET 524. The collector of NPN transistor 516 is coupled to the source 529 of a n-channel FET 526. The emitters of NPN transistors 514 and 516 are coupled to each other and a terminal of bias current source 535. The other terminal of bias current source 535 couples to a first supply voltage B-, such as ground. The gates 521 and 527 of n-channel FETs 524 and 526 are coupled to each other and to a first terminal of a resistor 525. The other terminal of resistor 525 is coupled to a second supply voltage such as B++. A first differential output signal 132 is coupled from the drain 522 of n-channel FET 524 which also is coupled to the drain 554 of p-channel FET 530. A second differential output signal 134 is coupled from drain 528 of n-channel FET 526 which is also coupled to the drain 556 of p-channel FET 540. The AGC input 130 is coupled to the gate 546 of p-channel FET 530 and also to the gate 558 of p-channel FET 540.

The bipolar transistor/FET cascode differential RF amplifier 110 comprises transistors 514, 516, 524, 526, capacitors 503, 505, resistor 525, and bias current supply 535. Capacitors 503, and 505 are RF impedance matching capacitors that present very low to moderate impedances at the RF frequency range for which the bipolar transistor/FET cascode differential RF amplifier 110 is designed and act as coupling capacitors for

the inputs 102 and 104 respectively. Bias current for transistors 514 and 516 is provided by the bias supply 535. Resistor 525 is coupled to the positive supply voltage B++ to provide bias to the n-channel FET devices 524 and 526. Balanced low level RF voltage signals applied to the inputs 102 and 104 are amplified such that the magnitude of each output signal 132 and 134 is a high level, inverted, nearly linear multiple of the respective input signals in a manner well known to those skilled in the art.

The p-channel FET 530 functions as the voltage dependent resistive element 106 to provide a negative feedback path between output 132 and input 510, and p-channel FET 540 functions as the voltage dependent resistive element 108 to provide a negative feedback path between output 134 and input 520.

The unique addition of the voltage dependent resistive elements 106 and 108, comprising p-channel FETs 530 and 540 respectively, is preferably enabled by the use of BiCMOS technology. The AGC input 130 to the p-channel FETs 530 and 540 provides a means of reducing the gain of the bipolar transistor/FET cascode differential RF amplifier 110 with decreased input voltage, by altering the resistive path between the source 550 and drain 554 of p-channel FET 530 and the source 552 and drain 556 of p-channel FET 540. The signal for the AGC input 130 is provided either from the IF stage 140 after the RF amplifier stage 120 as shown in FIG 1, or from an RF single strength detector circuit 250 prior to the RF amplifier stage 120 as shown in FIG 4.

Referring to FIG. 8, an electrical schematic diagram of a differential RF amplifier 120 suitable for use in the RF receiver 101 of FIG. 1 or FIG. 4 is shown. Differential RF amplifier 120 comprises a neutralized bipolar transistor differential RF amplifier 110 and voltage dependent resistive elements 106 and 108.

A first differential input 102 is coupled to one terminal of a capacitor 503. The other terminal of capacitor 503 is coupled to the base of a bipolar NPN transistor 514, to the source 550 of a p-channel field effect transistor 530, and also to the base of a bipolar NPN transistor 626. A second differential input 104 is coupled to a first terminal of capacitor 505. The other terminal of capacitor 505 is coupled to the base of a bipolar NPN transistor 516, to the source 552 of a p-channel FET 540, and also to the base of NPN transistor 624. The emitters of NPN transistor 624 and NPN

transistor 626 are left uncoupled. The emitters of NPN transistors 514 and 516 are coupled to each other and a terminal of bias current source 535. The other terminal of bias current source 535 couples to a first supply voltage B-, such as ground. A first differential output signal 132 is coupled from the collector of NPN transistor 514 which also is coupled to the drain 554 of p-channel FET 530 and to the collector of NPN transistor 624. A second differential output signal 134 is coupled from the collector of NPN transistor 516 which is also coupled to the drain 556 of p-channel FET 540 and to the collector of NPN transistor 626. The AGC input 130 is coupled to the gate 546 of p-channel FET 530 and also to the gate 558 of p-channel FET 540.

The neutralized bipolar transistor differential RF amplifier 110 comprises transistors 514, 516, 624, 626, capacitors 503, 505, and bias current supply 535. Capacitors 503 and 505 are RF impedance matching capacitors that present very low to moderate impedances at the RF frequency range for which the neutralized bipolar transistor differential RF amplifier 110 is designed and act as coupling capacitors for the inputs 102 and 104 respectively. Bias current for transistors 514 and 516 is provided by the bias supply 535. Balanced low level RF voltage signals applied to the inputs 102 and 104 are amplified such that the magnitude of each output signal 132 and 134 is a high level, inverted, nearly linear multiple of the respective input signals in a manner well known to those skilled in the art.

The p-channel FET 530 functions as the voltage dependent resistive element 106 to provide a negative feedback path between output 132 and input 102, and p-channel FET 540 functions as the voltage dependent resistive element 108 to provide a negative feedback path between output 134 and input 104.

The unique addition of the voltage dependent resistive elements 106 and 108, comprising p-channel FETs 530 and 540 respectively, is enabled by the use of BiCMOS technology. The AGC input 130 to the p-channel FETs 530 and 540 provides a means of reducing the gain of the neutralized bipolar transistor differential RF amplifier 110 with decreased input voltage, by altering the resistive path between the source 550 and drain 554 of p-channel FET 530 and the source 552 and drain 556 of p-channel FET 540. The signal for the AGC input 130 is provided either from the IF stage 140 after the RF amplifier stage 120 as shown in FIG 1,

or from an RF signal strength detector circuit 250 prior to the RF amplifier stage 120 as shown in FIG 4.

Referring to FIG. 9, an electrical schematic diagram of a single ended RF amplifier 320 suitable for use in the RF receiver 301 of FIG. 5 or FIG. 6 is shown. The single ended RF amplifier 320 comprises a bipolar transistor cascode single ended RF amplifier 310 and voltage dependent resistive element 108.

A single ended input 302 is coupled to one terminal of a capacitor 703. The other terminal of capacitor 703 is coupled to the base of a bipolar NPN transistor 714, and also to a first terminal of a capacitor 768. The other terminal of capacitor 768 is coupled to the source 552 of a p-channel field effect transistor (FET) 540. The collector of NPN transistor 714 is coupled to the emitter of NPN transistor 716. The base of NPN transistor 714 is also coupled to a terminal of bias current source 735 and a bias resistor 745. The other terminal of bias current source 735 couples to a regulated voltage source V_{REG} which is derived from a second supply voltage B++ in a manner well know to those skilled in the art. The other terminal of the bias resistor 745 is connected to the second supply voltage B++. The emitter of NPN transistor 714 is coupled to a first supply voltage B-, such as ground. A single ended output signal 324 is coupled from the collector of NPN transistor 716 which also is coupled to the drain 556 of p-channel FET 540. The base of the NPN transistor 716 is coupled to a first terminal of a resistor 730 and also to a first terminal of a capacitor 734. The other terminal of resistor 730 is coupled to the second supply voltage B++. The other terminal of capacitor 734 is coupled to the first supply voltage B-. The AGC input 130 is coupled to the gate 558 of the p-channel FET 540.

The bipolar transistor cascode single ended RF amplifier 310 comprises transistors 714, 716, capacitors 703, 734, 768, bias resistors 730 and 745, and bias current supply 735. The capacitors 734 and 768 are direct current (DC) blocking capacitors that present very low impedances at the RF frequency range for which the RF amplifier is designed. The capacitor 703 is an impedance matching capacitor which acts as the RF coupling capacitor for the input 302. The capacitor 768 acts as the RF coupling capacitor for the feedback output from the source 552 of the p-channel FET 540. The capacitor 734 acts as the RF coupling capacitor to provide an RF ground for the base of transistor 716. Low level RF voltage signals

applied to the input 102 are amplified such that the magnitude of the output signal 132 is a high level, inverted, nearly linear multiple of the input signal 102 in a manner well known to those skilled in the art. The p-channel FET 540 functions as the voltage dependent resistive element 108 to provide a negative feedback path between output 324 and input 302.

The unique addition of the voltage dependent resistive element 108, comprising p-channel FET 540, is enabled by the use of BiCMOS technology. The AGC input 130 to the p-channel FET 540 provides a means of reducing the gain of the single ended RF amplifier 320 with decreased input voltage, by altering the resistive path between the source 552 and drain 556 of p-channel FET 540. The signal for the AGC input 130 is provided either from the IF stage 340 after the RF amplifier stage 320 as shown in FIG 5, or from an RF single strength detection stage 450 prior to the RF amplifier stage 320 as shown in FIG 6.

Referring back to FIG. 7, FIG. 8, and FIG. 9, the voltage dependent resistive devices 106 and 108 could also be implemented using p-channel enhancement mode FETs, or n-channel depletion mode FETs, or p-channel depletion mode FETs, or n-channel enhancement mode FETs. The p-channel enhancement mode FET is the preferred embodiment. Also, it will be appreciated that the source and drain coupling shown in the figures could be reversed for any of the alternative embodiments. Such changes would require coupling and biasing modifications that are well known to those skilled in the art.

Referring to FIG. 10, an electrical block diagram of an RF communications device utilizing an RF receiver 801 in accordance with any one of the embodiments of the present invention of FIG. 1, FIG. 4, FIG. 5, or FIG. 6 is shown.

In accordance with the first and second embodiments of the RF receiver 101 described in FIG. 1 and FIG. 4, signals 803 and 805 are coupled from an antenna 800 to an antenna coupler 806. These signals are coupled to the differential inputs of an RF receiver 801 and to the differential outputs of an RF transmitter 880, as determined by the state of a control signal 818 coupled from a controller 810 to the antenna coupler 806. The audio and digital information demodulated in the receiver 801 is coupled to the controller 810 and also to an audio interface circuit 860. The controller 810 is coupled by a multiplicity of bi-directional

digital signals 835 to address memory 840, is coupled to annunciator 830 by output control signal 815, is coupled to display 850 by a multiplicity of output digital signals 845, is coupled to controls 820 by a multiplicity of input control signals 825, and is also coupled to the RF transmitter 880 by digital output signal 828. The audio interface circuit 860 is coupled to a speaker 865 by an analog output signal 874 and is coupled to a microphone 875 by an analog input signal.

The demodulated information 160 received by the controller 810 is processed digitally by the controller 810. An address portion of the processed digital information is used to determine if the remaining processed digital information is intended for other uses within this RF communications device. This is accomplished by comparing the address portion of the processed digital information with address information which has been stored in the address memory 840. When the remaining processed digital information is determined to be for use within this RF communications device, then controller 810 uses the remaining processed digital information in a manner dictated by information contained in the remaining portion of the digital information. Possible uses include displaying received or stored information on the display or creating a sound pattern, such as an alert tone, by means of the annunciator. A portion or all of the demodulated signal 160 that is analog can also be used to drive the speaker 865. The demodulated signal 160 is amplified within the audio interface 860 and coupled to speaker 865 under the control of controller output 872.

The controller 810, in response to settings or changes of controls 820, or in response to received information, causes RF transmissions from the RF communications device which contain digital and/or analog information. For example, a voice transmit control, such as a push to talk button, included in controls 820 is activated to initiate a transmission of voice information coupled from microphone 875 to the audio interface circuit 860. The controller 810 prevents the audio from being processed by the audio interface circuit for a short time while coupling the address information from the controller output 828 to the RF transmitter 880, and then coupling the audio processed by the audio interface circuit 860 from the microphone 875 to the RF transmitter 880.

The RF communications device can be embodied as a duplex RF communications device, capable of RF transmission and reception

simultaneously, or embodied as a simplex RF communications device, capable of either transmission or reception but not both simultaneously. When embodied as a simplex RF communications device, the coupler 806 is an RF switch which connects the antenna signals 803 and 805 either to the RF receiver input signals 802 and 804 or the RF transmitter outputs 807 and 808. When embodied as a duplex RF communications device, the coupler 806 is a device which simultaneously couples received signals of a first RF frequency from the antenna 800 to the receiver 801 while coupling transmit signals of a second RF frequency from the RF transmitter 880 to the antenna 800, with virtually no portion of the transmit signal coupled to the RF receiver input signals 802 and 804.

In accordance with the third and fourth embodiments of the RF receiver 301 described in FIG. 5 and FIG. 6, signals 805, 804, and 808 are single ended instead of differential, and the couplings 803, 802, and 807 do not exist. In all other respects, the RF communications device is as described above.

There exist other variations to the RF communications device described above which are commonly known. Those which contain at least the antenna 800 and the receiver 801 will benefit from one or more of the embodiments of the present invention. One such common RF communications device is a pager, which provides a receive only function, thus utilizing only those elements associated with receiving and displaying a message.

By now it should be appreciated that there has been provided an apparatus which can be integrated, using such processes as a BiCMOS technology, into the same circuit as an RF amplifier, and which allows for the control of the gain of the RF amplifier without increasing the noise figure of the RF amplifier, and which improves the IM distortion of the RF amplifier, thereby greatly reducing intermodulation distortion of the RF receiver output at higher RF input signal levels.

I claim:

1. A radio frequency (RF) communications device comprising:

an antenna;

a radio frequency (RF) receiver with an input coupled to the antenna wherein said RF receiver comprises

an RF amplifier having an amplifier gain and an input for receiving at least one RF input signal and having an output from which at least one RF output signal is generated amplified by the amplifier gain,

means for producing a control signal which varies in response to a received signal strength,

a voltage dependent resistive element, coupled between the input and the output of the RF amplifier, for controlling the gain of the RF amplifier in response to the control signal, and

means for processing the at least one RF output signal of the RF amplifier and demodulating the processed signal;

a decoder for decoding the demodulated signal to generate information; and

presentation means for presenting the information generated from the decoded signal.

2. An RF communications device of claim 1 wherein the RF communications device is a pager, and wherein said pager further comprises selective call receiving means which presents at least some of the information when a predetermined portion of the information is substantially equivalent to an address which is stored in said pager.

3. The RF communications device of claim 1 further comprising an intermediate frequency (IF) stage coupled to the output of the RF amplifier, said IF stage having a signal strength detecting circuit, wherein said means for producing the control signal comprises said signal strength detecting circuit.

4. The RF communications device of claim 1 wherein said means for producing the control signal comprises an RF signal strength detector circuit coupled to the input of said RF amplifier.

5. The RF communications device of claim 1 wherein the voltage dependent resistive element is a field effect transistor (FET).

6. The RF communications device of claim 5 wherein said RF amplifier and said FET are integrated in a monolithic bipolar and complementary metal oxide (BiCMOS) integrated circuit.

7. The RF communications device of claim 5 wherein said FET is a p-channel FET.

8. The RF communications device of claim 5 wherein said FET is a n-channel FET.

9. The RF communications device of claim 1 wherein said RF amplifier is a differential RF amplifier and wherein said input and output each comprise two nodes.

10. The RF communications device of claim 9 wherein said differential RF amplifier is a bipolar transistor/field effect transistor (FET) cascode differential RF amplifier and wherein said voltage dependent resistive element comprises two FETs.

19. The RF communications device of claim 13 wherein said RF amplifier is a differential RF amplifier and wherein said input and output each comprise two nodes.

20. The RF communications device of claim 19 wherein said differential RF amplifier is a bipolar transistor/field effect transistor (FET) cascode differential RF amplifier and wherein said voltage dependent resistive element comprises two FETs.

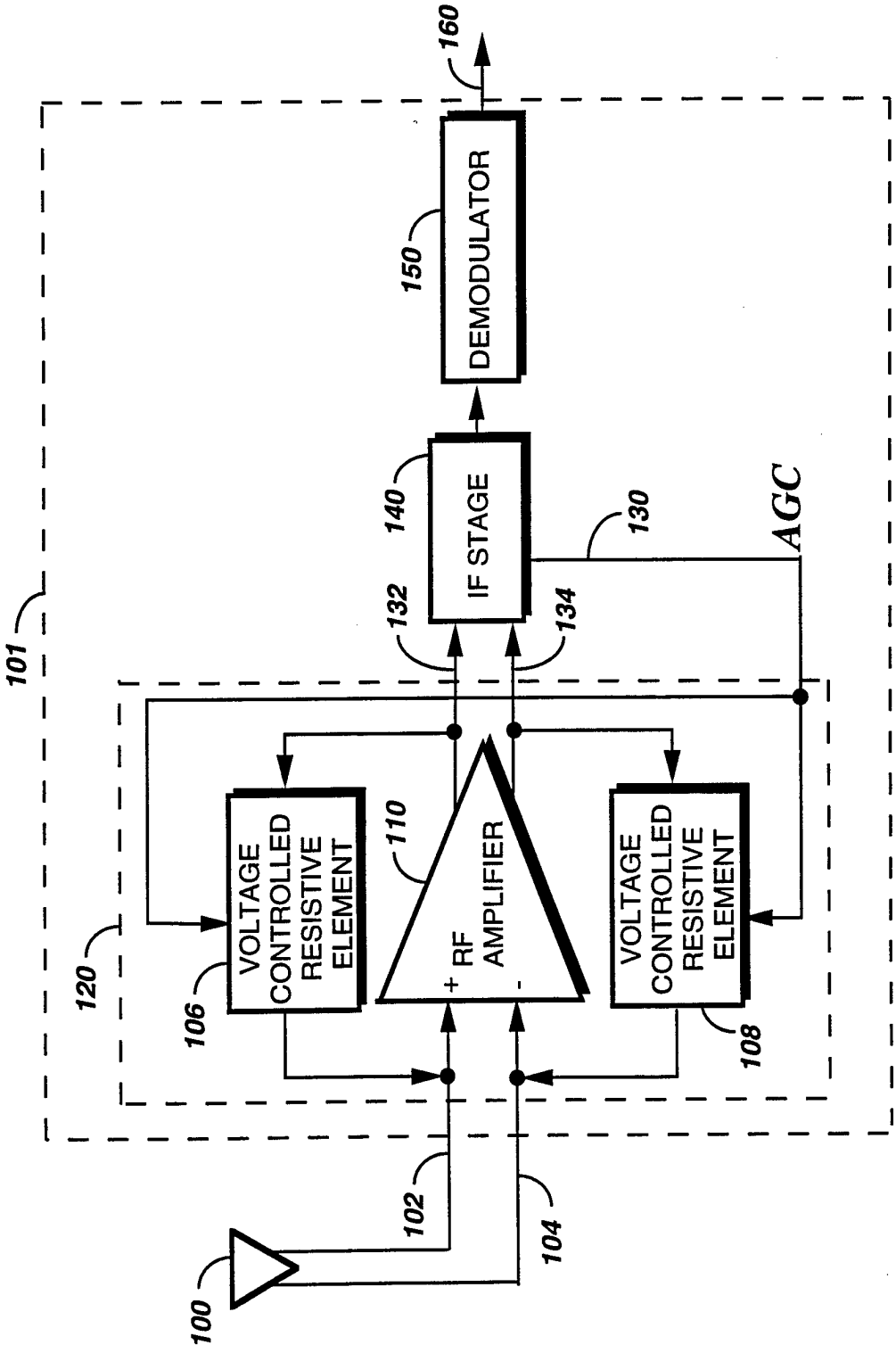
160
150
DEMODULATOR
140
IF STAGE
130
AGC
132
134
101
VOLTAGE CONTROLLED RESISTIVE ELEMENT
110
RF AMPLIFIER
+
-
VOLTAGE CONTROLLED RESISTIVE ELEMENT
120
106
108
102
104
100

FIG. 1

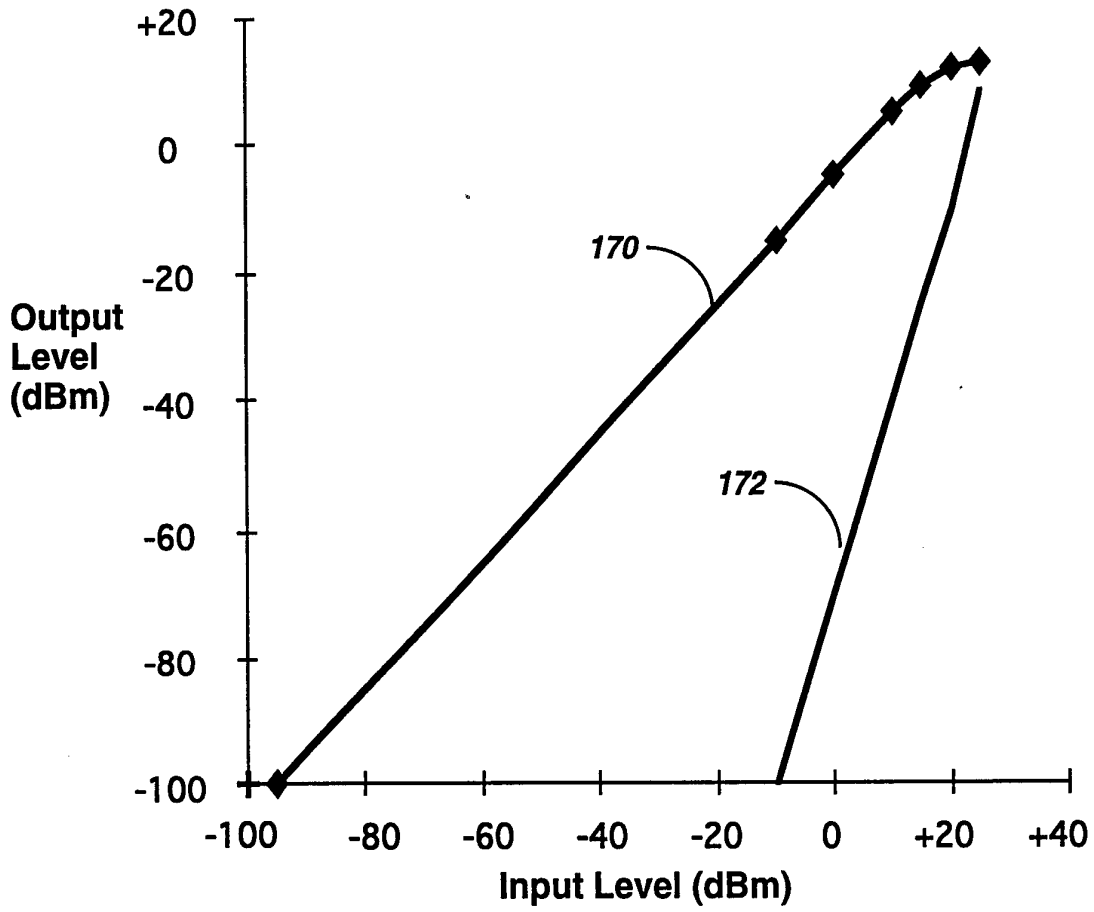
+20
0
-20
-40
-60
-80
-100
Output Level (dBm)
170
172
-100
-80
-60
-40
-20
0
+20
+40
Input Level (dBm)

FIG. 2

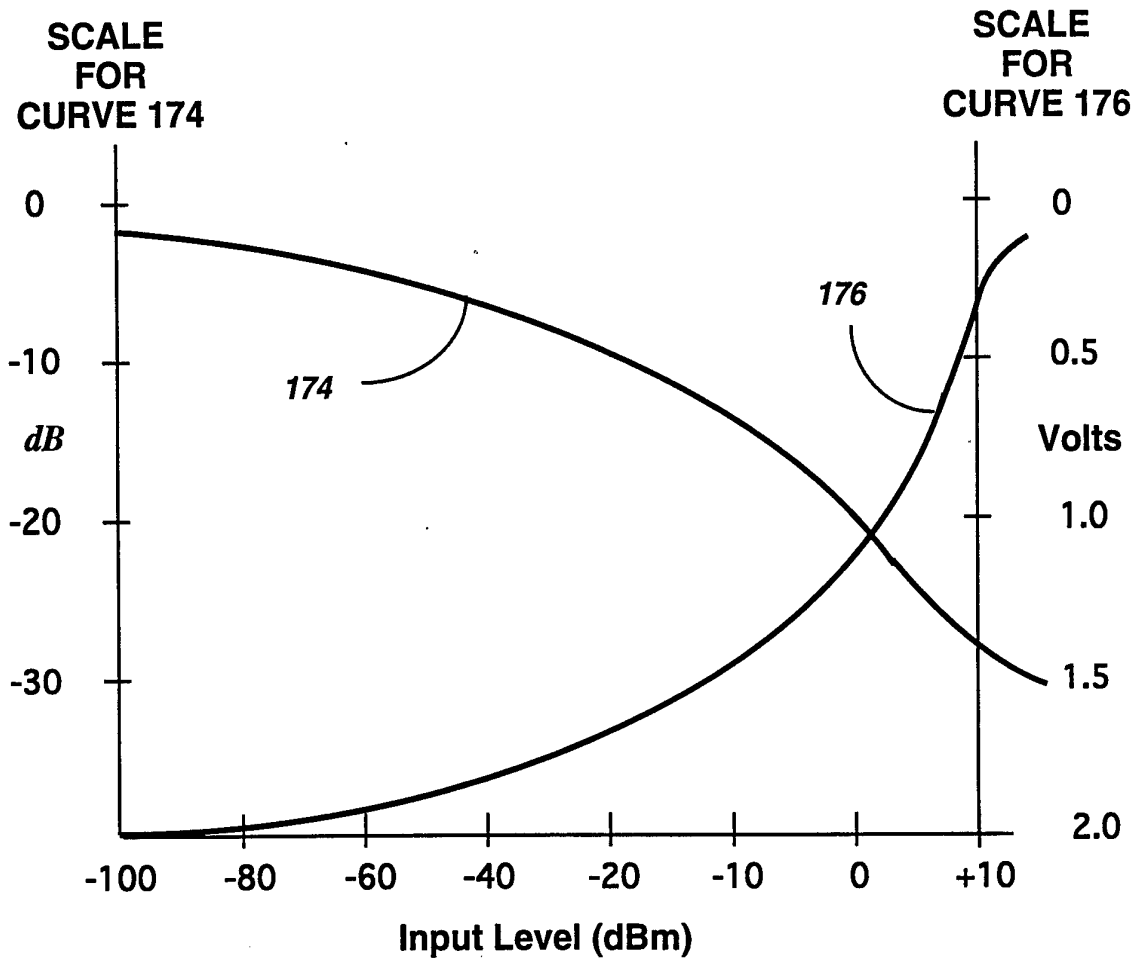
SCALE FOR CURVE 174
SCALE FOR CURVE 176
0
-10
dB
-20
-30
174
176
0
0.5
Volts
1.0
1.5
2.0
-100
-80
-60
-40
-20
-10
0
+10
Input Level (dBm)

FIG. 3

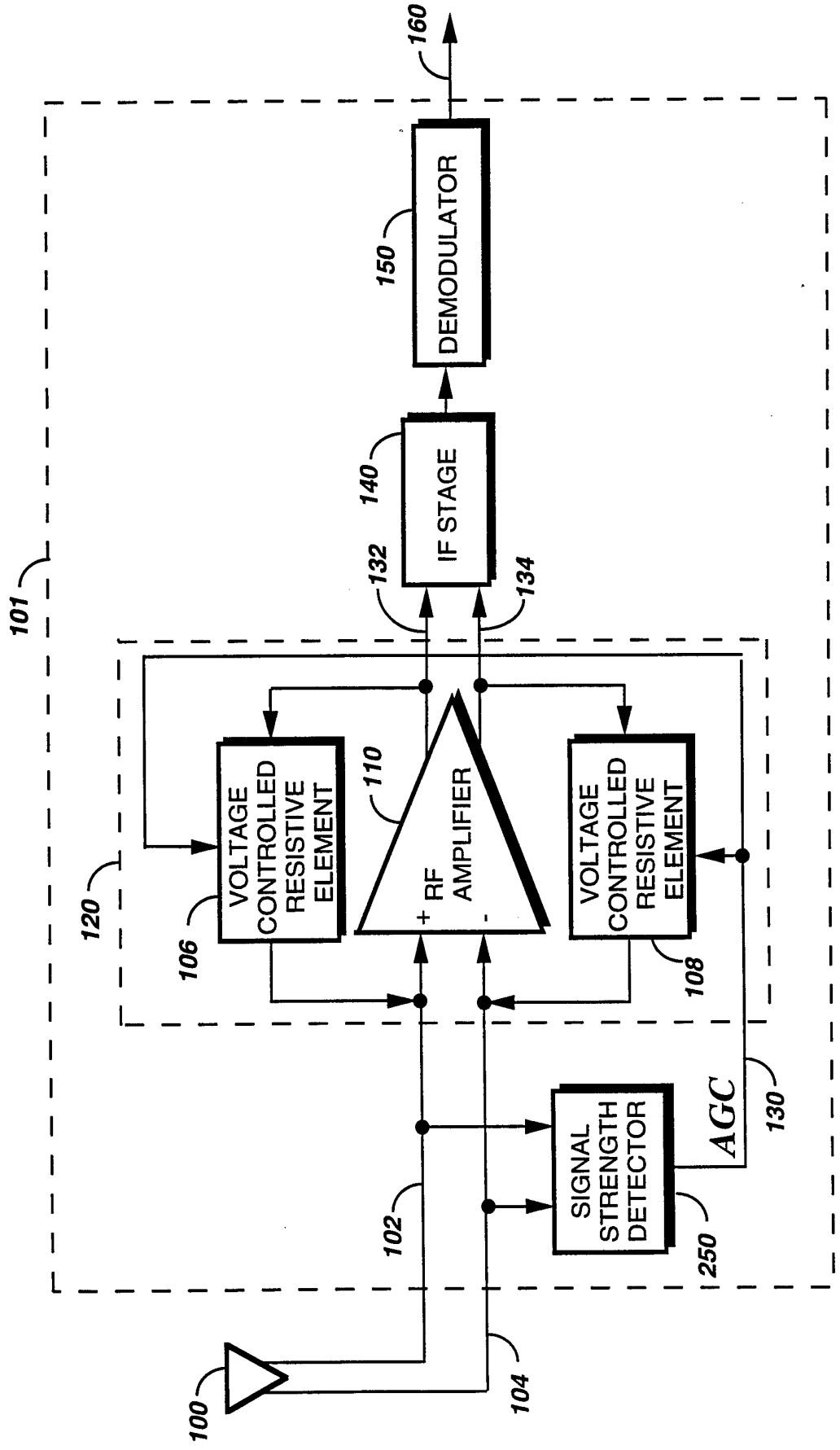
160
150
DEMODULATOR
140
IF STAGE
132
134
101
120
VOLTAGE CONTROLLED RESISTIVE ELEMENT
106
110
RF AMPLIFIER
+
-
VOLTAGE CONTROLLED RESISTIVE ELEMENT
108
AGC
130
SIGNAL STRENGTH DETECTOR
250
102
104
100

FIG. 4

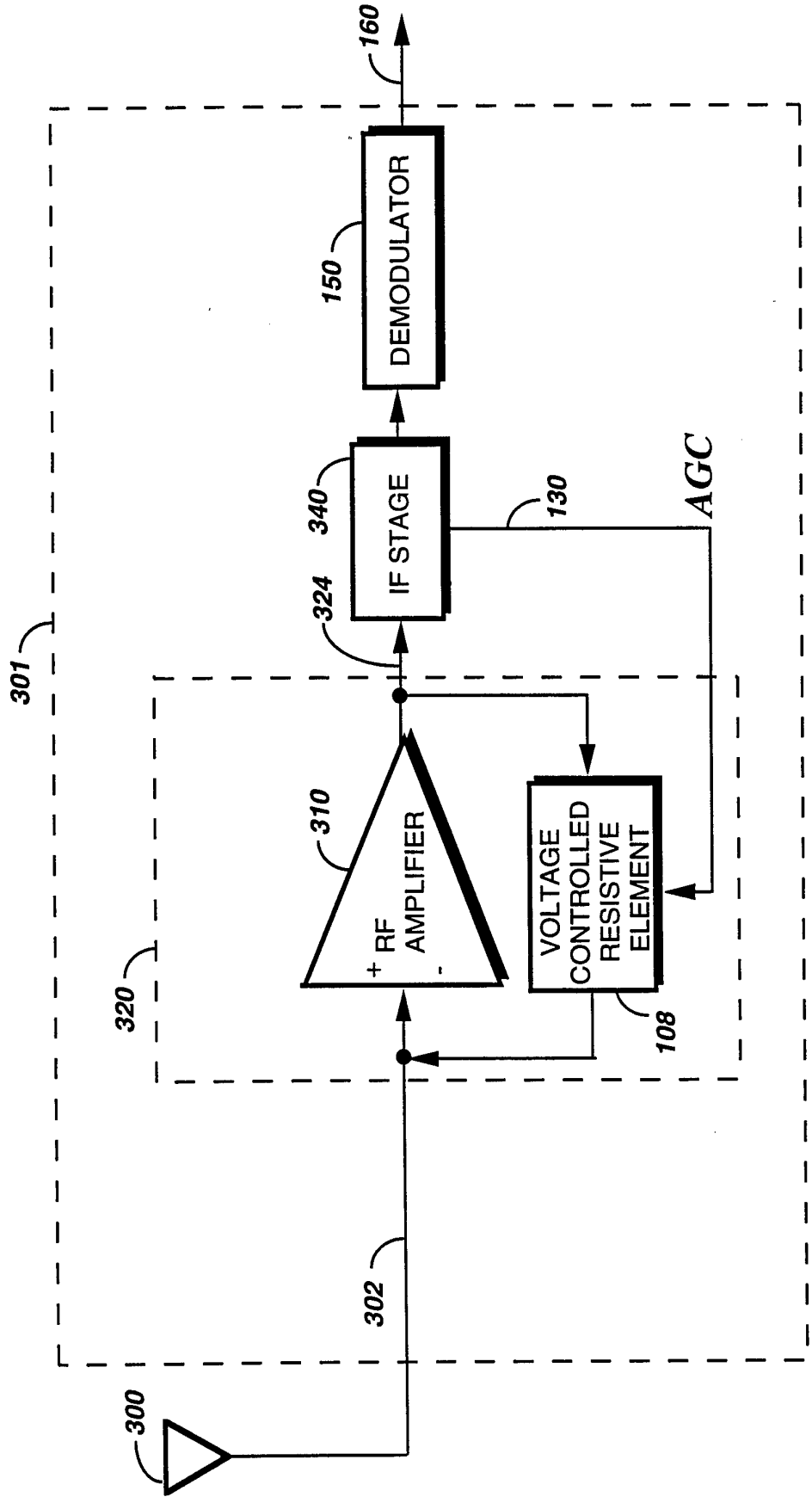
160
150
DEMODULATOR
340
IF STAGE
130
AGC
324
301
310
RF AMPLIFIER
+
-
320
VOLTAGE CONTROLLED RESISTIVE ELEMENT
108
302
300

FIG. 5

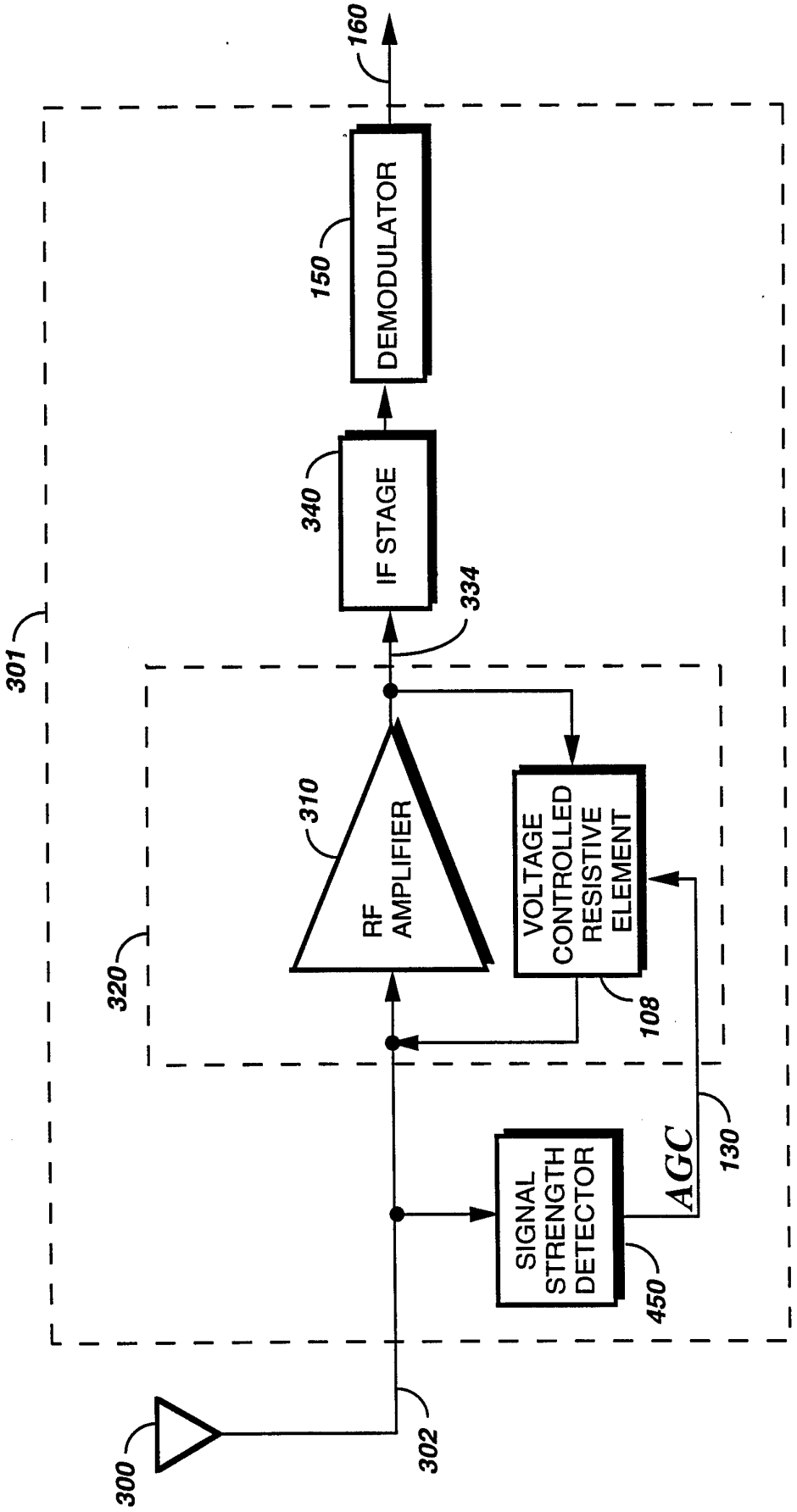
160
150
DEMODULATOR
340
IF STAGE
334
301
310
RF AMPLIFIER
320
VOLTAGE CONTROLLED RESISTIVE ELEMENT
108
AGC
130
SIGNAL STRENGTH DETECTOR
450
300
302

FIG. 6

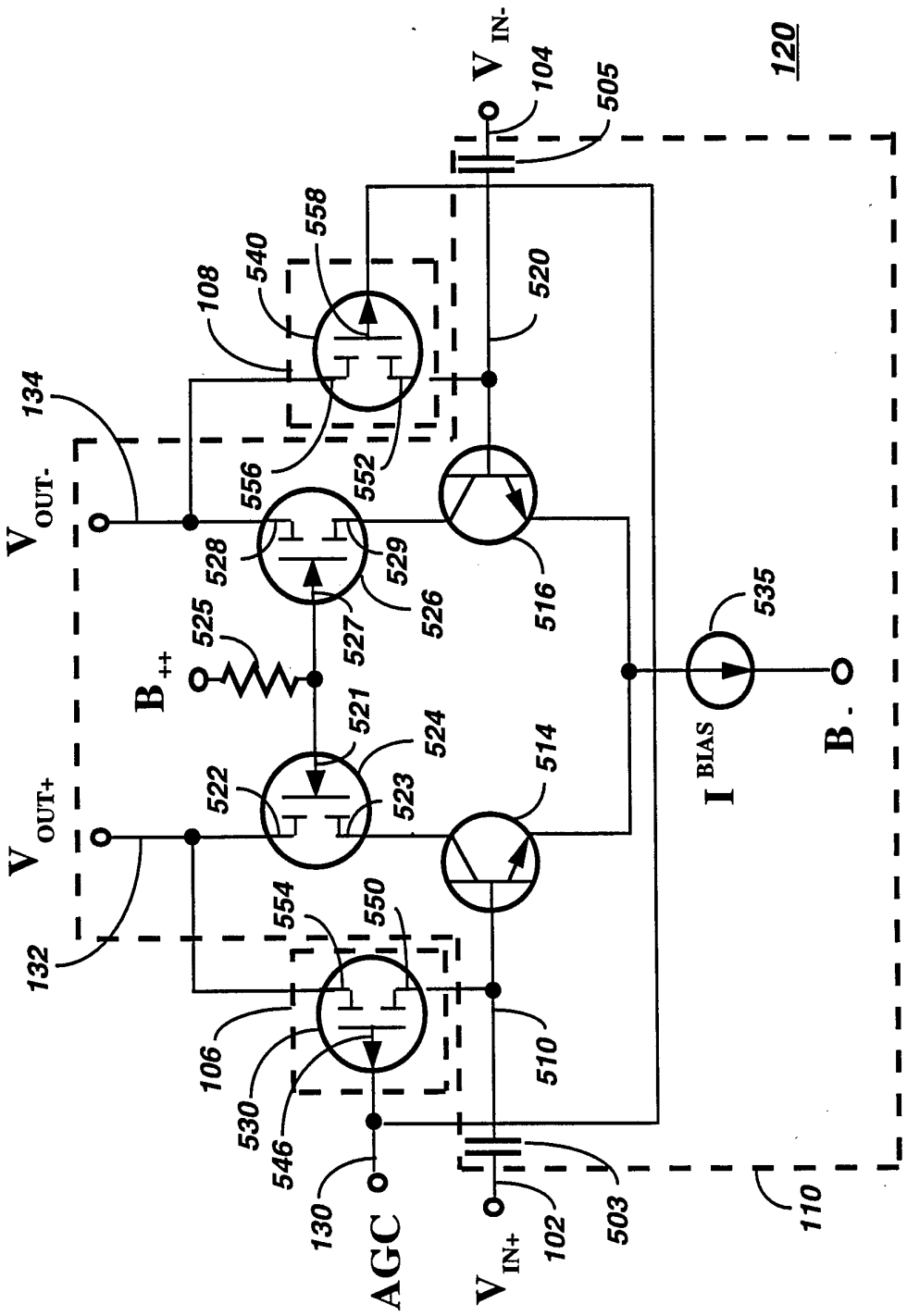
120
V_{IN-}
104
505
558
540
108
520
134
V_{OUT-}
556
552
528
529
526
527
516
525
B_{++}
535
521
524
514
522
523
I_{BIAS}
B_-
V_{OUT+}
132
554
550
106
530
546
510
130
AGC
V_{IN+}
102
503
110

FIG. 7

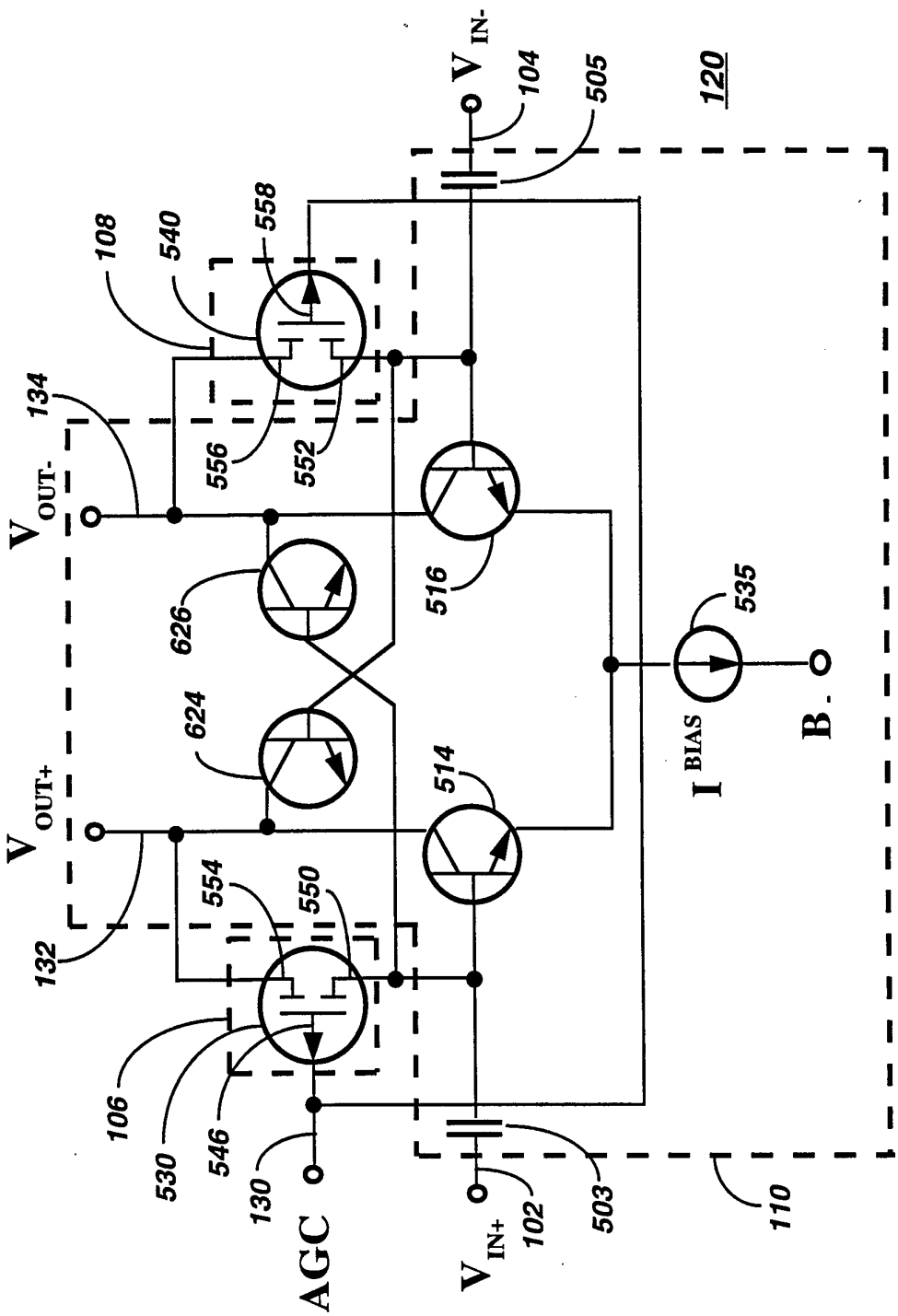
V IN-
104
505
120
108
540
558
134
V OUT-
556
552
626
516
535
624
514
I BIAS
B.
V OUT+
554
550
132
106
530
546
130
AGC
V IN+
102
503
110

FIG. 8

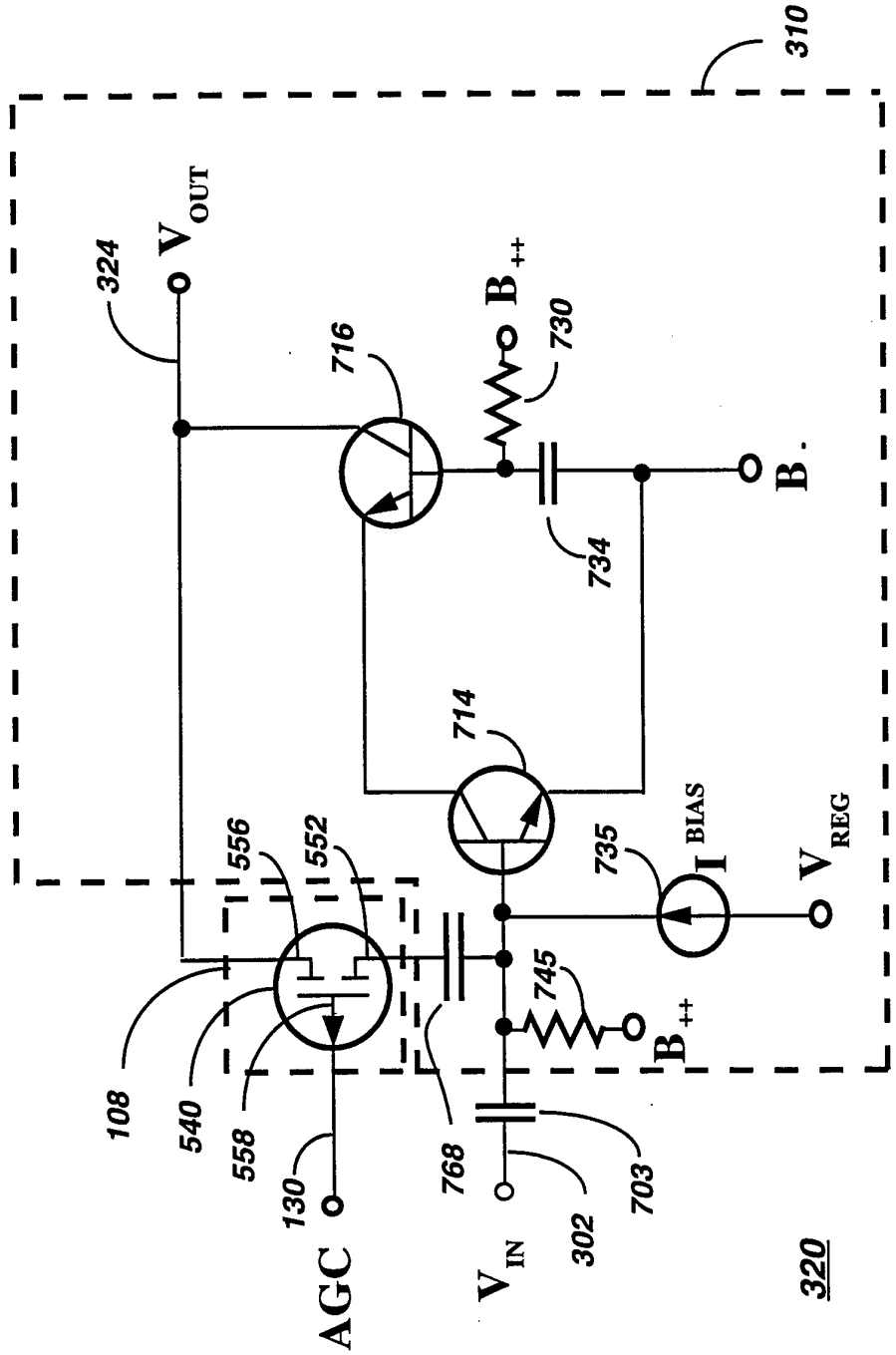
310
324
V_{OUT}
716
B_{++}
730
B.
734
714
556
552
735
I_{BIAS}
V_{REG}
745
B_{++}
108
540
558
130
768
703
302
AGC
V_{IN}
320

FIG. 9

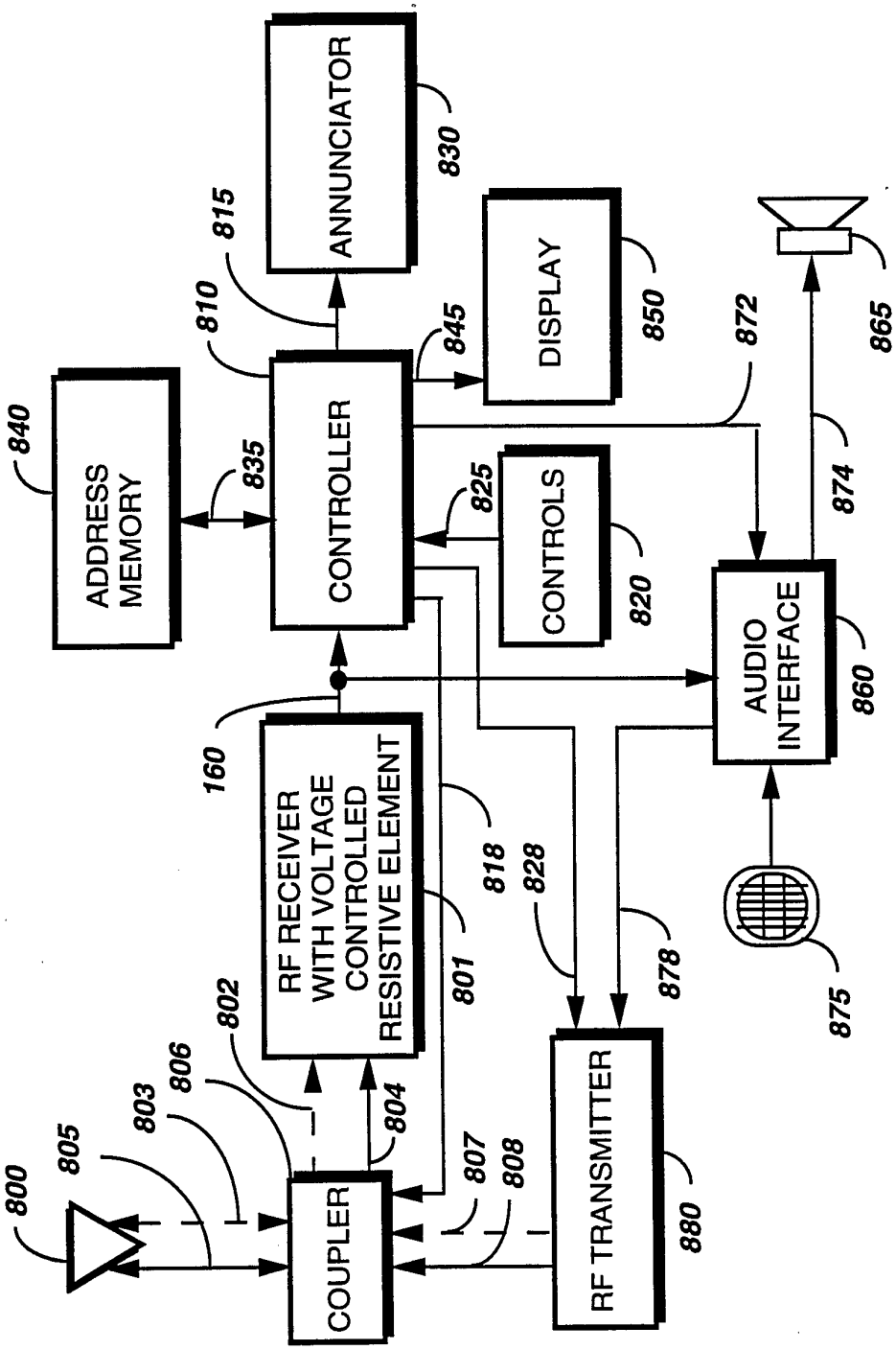
ANNUNCIATOR
830
815
810
DISPLAY
850
845
872
865
840
ADDRESS MEMORY
835
CONTROLLER
825
CONTROLS
820
874
AUDIO INTERFACE
860
160
RF RECEIVER WITH VOLTAGE CONTROLLED RESISTIVE ELEMENT
818
828
801
878
875
802
806
803
805
804
807
808
800
COUPLER
RF TRANSMITTER
880

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/06333

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04B 1/16; H03G 3/20.
US CL :455/234.1, 250.1; 330/282, 254.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/234.1, 250.1, 232.1, 235.1, 248.1, 252.1, 254; 330/282, 254, 285, 86; 340/825.44, 311.1.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

None

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US, A, 3,368,156 (KAM) 06 February 1968 See figures 1-2, columns 3-6.	1-2 ----- 3-10
Y	GB, A, 2223146 (KASAI) 28 March 1990 See figure 1.	3
Y	US, A, 4,531,234 (BELL) 23 July 1985 See figure 2, column 6, lines 3-31.	4
Y	US, A, 5,047,731 (LEE) 10 September 1991 See figures 1-3, column 2, lines 25-26, column 3, lines 30-38, column 4, lines 33-43.	5-8
Y	US, A, 3,500,223 (THURNELL) 10 March 1970 See the sole figure, column2, lines 33-40.	9-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 19 JULY 1994	Date of mailing of the international search report SEP 20 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer NGUYEN VO Telephone No. (703) 308-6728

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/06333

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 19-20
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Claim 19 depends on claim 13. Claim 20 depends on claim 19. Claims 13 and 19, however, are not found in the present application. Therefore, claims 19-20 have no clear meaning and incomplete. Accordingly, claims 19-20 are unsearchable.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.