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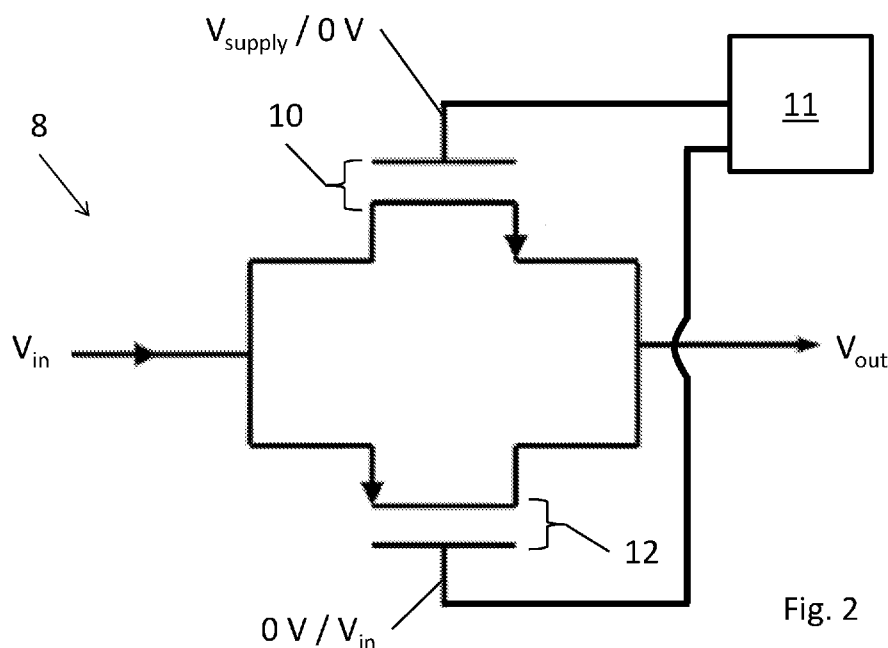


Fig. 2

(57) **Abstract:** A transmission gate circuit portion (8) is arranged selectively to pass an input signal V_{in} from an input node to an output node. A control circuit portion (11) arranged to provide a first control voltage $V_{supply} / 0 V$ and a second control voltage $0 V / V_{in}$. A first field-effect-transistor (10) has its drain terminal connected to the input node, its source terminal connected to the output node, and its gate terminal connected to the first control voltage $V_{supply} / 0 V$. A second field-effect-transistor (12) has its drain terminal connected to the output node, its source terminal connected to the input node, and its gate terminal connected to the second control voltage $0 V / V_{in}$. The drain-source breakdown voltages of the two transistors (10), (12) are substantially equal. At least one of the first and second field-effect transistors (10), (12) has its respective drain-source breakdown voltage greater than its respective gate-source, gate-drain, and gate-body breakdown voltages of the respective field-effect-transistor (10), (12).



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Transmission Gates

5 The present invention relates to transmission gates, particularly transmission gates for use in analogue-to-digital converters.

Modern electronic circuits, including analogue-to-digital converters (ADCs), employ a particular circuit element known as a transmission gate. A transmission gate is effectively a switch that can either provide a bidirectional signal path or can (ideally) block signals from passing through it. The transmission gate can be switched between these two modes through use of a control signal. Such transmission gates therefore pass a signal from an input terminal to an output terminal or block it, depending on the value of the control signal, e.g. if the control signal is logic high, the transmission gate will pass the signal or, if the control signal is logic low, the transmission gate will block the signal, or *vice versa*.

Typical transmission gates are constructed using complementary metal-oxide-semiconductor (CMOS) technology, wherein a complementary, matched pair of transistors – a p-channel metal-oxide-semiconductor field-effect-transistor (pMOSFET) and an n-channel metal-oxide-semiconductor field-effect-transistor (nMOSFET) – are connected in parallel with one another. The input terminal is typically connected to one terminal of each transistor (e.g. the source terminals of each) and the output terminal is connected to the other terminal of each transistor (e.g. the drain terminal of each). The control signal is applied to the gate terminal of one of the transistors and a logical negation of the control signal is applied to the gate terminal of the other transistor. This ensures that both transistors are on, or both transistors are off, at the same time. Such a conventional transmission gate structure can be found on page 123 of the textbook "CMOS Analog Circuit Design, Second Edition" by Douglas R. Holberg and Phillip E. Allen.

CMOS-based transmission gates are particularly suited for digital circuits due to their ability to pass both "strong" digital '0's and strong digital '1's from the input to the output when compared to a single nMOSFET (which can typically only pass a strong '0' but a poor '1') or a single pMOSFET (which can typically only pass a strong '1' but a poor '0') used as a switch. One exemplary application of the use of

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a transmission gate of the kind described is an ADC for use in battery voltage measurement – i.e. for checking the voltage produced by a battery. Such a battery measurement ADC may, for example, require a 5 V transmission gate.

5 When analysing the performance of a transmission gate, two important measures are the "on-resistance" R_{on} and the "off-resistance" R_{off} of the transmission gate. The on-resistance R_{on} is the resistance of the transmission gate while it is switched on (i.e. when signals may pass through it). Similarly, the off-resistance R_{off} is the resistance of the transmission gate while it is switched off (i.e. when signals are
10 supposed to be blocked). However, the Applicant has appreciated that the on and off-resistances R_{on} , R_{off} typically vary depending on the input voltage presented at the input terminal.

The Applicant has appreciated that it would be advantageous for a transmission
15 gate to exhibit a greater degree of linearity with respect to the on and off-resistances R_{on} , R_{off} across a range of different input voltages.

When viewed from a first aspect, the present invention provides a transmission gate circuit portion arranged selectively to pass an input signal from an input node to an
20 output node, said transmission gate comprising:

a control circuit portion arranged to provide first and second control voltages;

a first field-effect-transistor having a drain terminal connected to the input node, a source terminal connected to the output node, and a gate terminal
25 connected to the first control voltage, said first field-effect-transistor having a first drain-source breakdown voltage, a first gate-source breakdown voltage, a first gate-drain breakdown voltage, and a first gate-body breakdown voltage; and

a second field-effect-transistor having a drain terminal connected to the output node, a source terminal connected to the input node, and a gate terminal
30 connected to the second control voltage, said second field-effect-transistor having a second drain-source breakdown voltage, a second gate-source breakdown voltage, a second gate-drain breakdown voltage, and a second gate-body breakdown voltage;

wherein the first drain-source breakdown voltage is substantially equal to
35 the second drain-source breakdown voltage; and

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wherein at least one of the first and second field-effect transistors has its respective drain-source breakdown voltage greater than its respective gate-source, gate-drain, and gate-body breakdown voltages of the respective field-effect-transistor.

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Thus it will be appreciated by those skilled in the art that the present invention provides a transmission gate that exhibits less variation in the on-resistance and off-resistance presented by the transmission gate across a range of input voltages compared to conventional transmission gate arrangements, thus leading to improvements in the linearity of the transmission gate. The improved linearity arises due to at least one of FETs being arranged such that its drain-source breakdown voltage is higher than its respective gate-source, gate-drain, and gate-body breakdown voltages.

Those skilled in the art will appreciate that, in general, the drain-source breakdown voltage of a FET is the maximum rated voltage that can be applied between the drain and source terminals of the FET without it breaking down electrically. Typically the drain-source breakdown voltage is different across different device categories. Similarly, the gate-source, gate-drain, and gate-body breakdown voltages are typically different across different device categories.

For example, typically, a '5 V' PMOS-based FET might typically exhibit drain-source, gate-source, gate-drain, and gate-body breakdown voltages of approximately between 5 V and 6 V, for example 5.5 V. Conversely, a '3 V' NMOS-based FET might typically exhibit drain-source, gate-source, gate-drain, and gate-body breakdown voltages of approximately between 3 V and 4 V, for example 3.6 V.

The Applicant has appreciated that a FET (or FETs) having a greater drain-source breakdown voltage than the other breakdown voltages is effectively a device of a 'lower device category' but that exhibits an atypically high drain-source breakdown voltage. Thus, in accordance with embodiments of the present invention, a special FET is used where the gate-source, gate-drain, and gate-body breakdown voltages are typical of a different device category to that associated with the drain-source breakdown voltage.

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The off-resistance exhibited by the transmission gate is effectively the parallel combination of the off-resistance of the first FET and the off-resistance of the second FET. Due to at least one of these FETs being from a 'lower' device category but with a higher drain-source breakdown voltage, this FET (or FETs) exhibit a smaller off-resistance than a conventional FET having that drain-source breakdown voltage. As such, the off-resistance of the transmission gate is dominated by the off-resistance of the FET (or FETs) with the increased drain-source breakdown voltage.

Similarly, the on-resistance exhibited by the transmission gate is effectively the parallel combination of the on-resistance of the first FET and the on-resistance of the second FET. As, the FET with the increased drain-source breakdown voltage has a smaller on-resistance than a conventional FET, the on-resistance of the transmission gate is also dominated by the on-resistance of the FET (or FETs) with the increased drain-source breakdown voltage.

A transmission gate in accordance with some embodiments of the present invention may be constructed from two different, unmatched field-effect-transistors (FETs), i.e. the two FETs may have different gate-source, gate-drain, and gate-body breakdown voltages to one another but have the same drain-source breakdown voltage. This unconventional arrangement provides a transmission gate that uses FETs that effectively belong in different device categories. In particularly preferred set of such embodiments, the first drain-source breakdown voltage is greater than the first gate-source, gate-drain, and gate-body breakdown voltages.

However, both the first and second FETs may exhibit this property. Thus, in some alternative embodiments, the first drain-source breakdown voltages is greater than the first gate-source, gate-drain, and gate-body breakdown voltages; and the second drain-source breakdown voltages is greater than the second gate-source, gate-drain, and gate-body breakdown voltages.

The two FETs are each arranged such that the drain terminal of each is connected to the source terminal of the other. In some embodiments, at least one of the first and second field-effect-transistors is an n-channel metal-oxide-semiconductor field-

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effect-transistor and the other of said first and second field-effect-transistors is a p-channel metal-oxide-semiconductor field-effect-transistor. It will be appreciated that these could be either way around depending on which of the input and output nodes is generally at the greater voltage. However, typically the input node is at a greater voltage than the output node and thus, in at least some preferred embodiments, the first field-effect-transistor comprises an n-channel metal-oxide-semiconductor field-effect-transistor and the second field-effect-transistor comprises a p-channel metal-oxide-semiconductor field-effect-transistor.

While the field-effect-transistors could be depletion-type FETs, it is preferred that these are enhancement type. Thus in a set of embodiments, the first field-effect-transistor is enhancement type. In a potentially overlapping set of embodiments, the second field-effect-transistor is enhancement type. Thus in a preferred set of embodiments, the first field-effect-transistor comprises an enhancement type n-channel metal-oxide-semiconductor field-effect-transistor and the second field-effect-transistor comprises an enhancement type p-channel metal-oxide-semiconductor field-effect-transistor. In some embodiments, the first drain-source breakdown voltage is greater than 5 V, e.g. between 5 V and 6 V, e.g. 5.5 V.

In some embodiments, the first gate-source breakdown voltage is between 2 V and 5 V, e.g. between 3 V and 4 V, e.g. 3.6 V.

In some embodiments, the first gate-drain breakdown voltage is between 2 V and 5 V, e.g. between 3 V and 4 V, e.g. 3.6 V.

In some embodiments, the first gate-body breakdown voltage is between 2 V and 5 V, e.g. between 3 V and 4 V, e.g. 3.6 V.

In some embodiments, the second drain-source breakdown voltage is greater than 5 V, e.g. between 5 V and 6 V, e.g. 5.5 V.

In some embodiments, the second gate-source breakdown voltage is greater than 5 V, preferably between 5 V and 6 V, and is preferably 5.5 V.

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In some embodiments, the second gate-drain breakdown voltage is greater than 5 V, preferably between 5 V and 6 V, and is preferably 5.5 V.

5 In some embodiments, the second gate-body breakdown voltage is greater than 5 V, preferably between 5 V and 6 V, and is preferably 5.5 V.

In some embodiments, the transmission gate circuit portion is arranged such that:
in a first mode of operation, the first control voltage is set to a non-zero value different to the input voltage and the second control voltage is set to zero; and
10 in a second mode of operation, the first control voltage is set to zero and the second control voltage is set to the input voltage. Those skilled in the art will appreciate that by setting the first control voltage to a non-zero value different to the input voltage and choosing this voltage appropriately, the off-resistance presented by the transmission gate can be made more consistent across a range of different
15 input voltages than would be typical of a conventional transmission gate.

This is novel and inventive in its own right and thus, when viewed from a second aspect, the present invention provides a method of operating a transmission gate circuit portion arranged selectively to pass an input signal from an input node to an
20 output node said transmission gate comprising:

a control circuit portion arranged to provide first and second control voltages;

a first field-effect-transistor having a drain terminal connected to the input node, a source terminal connected to the output node, and a gate terminal
25 connected to the first control voltage; and

a second field-effect-transistor having a drain terminal connected to the output node, a source terminal connected to the input node, and a gate terminal connected to the second control voltage;

wherein the method comprises:

30 in a first mode of operation, setting the first control voltage to a non-zero value different to the input voltage and setting the second control voltage to zero; and

in a second mode of operation, setting the first control voltage to zero and setting the second control voltage to the input voltage.

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Those skilled in the art will appreciate that the features described in relation to various embodiments of the first aspect of the invention apply equally, where appropriate, to the second aspect of the invention.

5 While it will be appreciated by those skilled in the art that there are many applications to which transmission gate circuit portions in accordance with the present invention may be readily applied, in a preferred set of embodiments, the input node is connected to a battery. Thus, in accordance with such embodiments, the transmission gate circuit portion is arranged to pass a voltage from a battery
10 from the input node to the output node, e.g. for digitisation by an ADC.

This is novel and inventive in its own right and thus, when viewed from a third aspect, the present invention provides an electronic circuit portion comprising:

a battery having first and second terminals and providing a battery voltage;
15 and

a transmission gate circuit portion arranged selectively to pass the battery voltage from an input node to an output node, said transmission gate comprising: a first field-effect-transistor having a drain terminal connected to the input node, a source terminal connected to the output node, and a gate terminal connected to a first control voltage; and
20

a second field-effect-transistor having a drain terminal connected to the output node, a source terminal connected to the input node, and a gate terminal connected to a second control voltage;

wherein the transmission gate circuit portion is arranged such that:
25 in a first mode of operation, the first control voltage is set to a non-zero value different to the battery voltage and the second control voltage is set to zero; and

in a second mode of operation, the first control voltage is set to zero and the second control voltage is set to the battery voltage.

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Those skilled in the art will appreciate that the features described in relation to various embodiments of the first and second aspects of the invention apply equally, where appropriate, to the third aspect of the invention.

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An embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram of a conventional transmission gate circuit portion;

Fig. 2 is a circuit diagram of a transmission gate circuit portion in
5 accordance with an embodiment of the present invention;

Fig. 3 is a graph comparing a simulation of the on-resistance of the transmission gate circuit portion of Fig. 2 of the conventional transmission gate circuit portion of Fig. 1; and

Fig. 4 is a graph comparing a simulation of the off-resistance of the
10 transmission gate circuit portion of Fig. 2 to the conventional transmission gate circuit portion of Fig. 1.

Fig. 1 is a circuit diagram of a conventional transmission gate circuit portion 2. The transmission gate 2 comprises an n-channel metal-oxide-semiconductor field-effect-
15 transistor (nMOSFET) 4 and a p-channel metal-oxide-semiconductor field-effect-transistor (pMOSFET) 6 arranged in parallel such that the drain terminal of the nMOSFET 4 and the source terminal of the pMOSFET 6 are connected to one another and to an input voltage V_{in} and such that the source terminal of the nMOSFET 4 and the drain terminal of the pMOSFET 6 are connected to one
20 another and produce an output voltage V_{out} . As is typical of such complementary metal-oxide-semiconductor (CMOS) based transmission gates, the nMOSFET 4 and the pMOSFET 6 are "matched" to one another, i.e. they have certain electrical characteristics including their respective drain-source and gate-source breakdown voltages in common with one another.

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Complementary control signals are applied to the gate terminals of the nMOSFET 4 and the pMOSFET 6, i.e. the signal applied to the gate terminal of the pMOSFET 6 is at all times the logical negation of the signal applied to the gate terminal of the nMOSFET 4. This is typically achieved by having a control circuit portion 3 that
30 produces a single control signal (in this example, the one applied to the gate terminal of the nMOSFET 4) and a Boolean inverter 5, connected between the gate terminals of the nMOSFET 4 and the pMOSFET 6, which provides the gate terminal of the pMOSFET 6 with the logical negation of the signal produced by the control circuit portion 3.

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When the transmission gate 2 is driven at "logic high", the gate terminal of the nMOSFET 4 is set to the input voltage V_{in} and the gate terminal of the pMOSFET 6 is set to 0 V. Conversely, when the transmission gate 2 is driven at "logic low", the gate terminal of the nMOSFET 4 is set to 0 V and the gate terminal of the pMOSFET 6 is set to V_{in} .

In the logic high state, the gate-source voltage of the nMOSFET 4 is $V_{in} - V_{out}$ and the gate-source voltage of the pMOSFET 6 is $0 - V_{in} = -V_{in}$. Thus, in the logic high state, both the nMOSFET 4 and the pMOSFET 6 conduct, assuming that their respective gate-source voltages exceed their respective threshold voltages.

Conversely, in the logic low state, the gate-source voltage of the nMOSFET 4 is $0 - V_{out} = -V_{out}$ and the gate-source voltage of the pMOSFET 6 is $V_{in} - V_{in} = 0$. Thus, in the logic low state, neither the nMOSFET 4 nor the pMOSFET 6 conducts, assuming that their respective gate-source voltages are below their respective threshold voltages.

The on-resistance R_{on} and off-resistance R_{off} values (i.e. the effective resistance of the transmission gate circuit portion 2 when it is switched on and switched off respectively) typically presented for two different values of the input voltage V_{in} are given below in Table 1:

V_{in} (V)	R_{on} (Ω)	R_{off} (G Ω)
2.5	258	82.67
4.35	148.58	109.07

Table 1: Comparison of on-resistance R_{on} and off-resistance R_{off} presented by the transmission gate circuit portion 2 for different input voltage V_{in} values.

25

It can be seen from Table 1 that the variation in on-resistance R_{on} between the cases where the input voltage V_{in} is 2.5 V and when it is 4.35 V is $\pm 27\%$. The variation in off-resistance R_{off} between the cases where the input voltage V_{in} is 2.5 V and when it is 4.35 V is $\pm 14\%$. The Applicant has appreciated that these variations in the on-resistance R_{on} and off-resistance R_{off} values across a typical

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range of input voltage V_{in} values are higher than is desirable as these negatively impact the linearity of the transmission gate.

Fig. 2 is a circuit diagram of a transmission gate circuit portion 8 in accordance with an embodiment of the present invention. In common with the conventional arrangement, the transmission gate 8 comprises an n-channel metal-oxide-semiconductor field-effect-transistor (nMOSFET) 10 and a p-channel metal-oxide-semiconductor field-effect-transistor (pMOSFET) 12 arranged in parallel such that the drain terminal of the nMOSFET 10 and the source terminal of the pMOSFET 6 are connected to one another and to an input voltage V_{in} and such that the source terminal of the nMOSFET 10 and the drain terminal of the pMOSFET 12 are connected to one another and are arranged to produce an output voltage V_{out} .

However, unlike the transmission gate circuit portion 2 of Fig. 1, the nMOSFET 10 and the pMOSFET 12 are not "matched" to one another. While the pMOSFET 12 is a standard '5 V' PMOS device having its respective drain-source, gate-source, gate-drain, and gate-body breakdown voltages all approximately equal to 5.5 V; the nMOSFET 10 is an unconventional NMOS device, where its respective gate-source, gate-drain, and gate-body breakdown voltages are typical of a '3 V' NMOS device, i.e. they are around 3.6 V, but the drain-source voltage of the nMOSFET 10 is 5.5 V, i.e. typical of the higher, '5 V', device category.

Furthermore, unlike the transmission gate circuit portion 2 of Fig. 1, the control signals applied to the gate terminals of the nMOSFET 10 and the pMOSFET 12 are not direct complements of each other. Instead, these control signals (labelled $V_{supply} / 0\text{ V}$ and $0\text{ V} / V_{in}$) are both produced by a control circuit portion 11 independently of one another. Similarly to the transmission gate circuit portion 2 of Fig. 1, when the transmission gate 8 is driven at logic low, the gate terminal of the nMOSFET 10 is set to 0 V and the gate terminal of the pMOSFET 12 is set to V_{in} . However, when the transmission gate circuit portion 8 is in the logic high state, the gate terminal of the nMOSFET 10 is set to a supply voltage V_{supply} and the gate terminal of the pMOSFET 12 is set to 0 V, wherein the supply voltage V_{supply} is different to the input voltage V_{in} .

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The supply voltage V_{supply} is lower than the input voltage V_{in} and may be produced from the input voltage V_{in} , for example using a low-dropout (LDO) voltage regulator, known in the art *per se*. A lower voltage (i.e. V_{supply}) can be applied to the gate terminal of the nMOSFET 10 than the voltage applied to the gate terminal of pMOSFET 12 (i.e. V_{in}) because the gate-source, gate-drain, and gate-body breakdown voltages of the nMOSFET 10 are lower than the corresponding breakdown voltages of the pMOSFET 12.

These lower breakdown voltages provide the nMOSFET 10 with more linear on- and off-resistance behaviours across a range of input voltages V_{in} as discussed below with reference to Figs. 3 and 4, while the higher drain-source breakdown voltage of the nMOSFET 10 (i.e. substantially equal to the higher drain-source breakdown voltage of the pMOSFET 12) allows the transmission gate circuit portion 8 to handle the same magnitude of input voltages V_{in} as the conventional transmission gate circuit portion 2 of Fig. 1.

In one exemplary application, the transmission gate circuit portion 8 may be used to monitor a battery voltage. In that example, the battery voltage would serve as the input voltage V_{in} , while V_{supply} would be derived from the battery voltage, for example using a low-dropout (LDO) voltage regulator, known in the art *per se*.

In the logic high state, the gate-source voltage of the nMOSFET 10 is $V_{\text{supply}} - V_{\text{out}}$ and the gate-source voltage of the pMOSFET 12 is $0 - V_{\text{in}} = -V_{\text{in}}$. Thus, in the logic high state, both the nMOSFET 10 and the pMOSFET 12 conduct, assuming that their respective gate-source voltages exceed their respective threshold voltages.

Conversely, in the logic low state, the gate-source voltage of the nMOSFET 10 is $0 - V_{\text{out}} = -V_{\text{out}}$ and the gate-source voltage of the pMOSFET 12 is $V_{\text{in}} - V_{\text{in}} = 0$. Thus, in the logic low state, neither the nMOSFET 10 nor the pMOSFET 12 conducts, assuming that their respective gate-source voltages are below their respective threshold voltages.

Fig. 3 is a graph comparing a simulation of the on-resistance R_{on} of the transmission gate circuit portion 8 of Fig. 2 to the on-resistance R_{on} exhibited by the

conventional transmission gate circuit portion 2 of Fig 1 across different input voltage V_{in} values.

5 The graph of Fig. 3 shows a number of curves 14, 16, 18, 20 corresponding to the on-resistance R_{on} of the transmission gate circuit portions 2, 8 under different operating conditions across a range of input voltage V_{in} values.

A first curve 14, corresponds to the on-resistance R_{on} of the conventional transmission gate circuit portion 2 described previously with reference to Fig. 1.

10 The other three curves 16, 18, 20 correspond to the on-resistance R_{on} of the transmission gate circuit portion 8 in accordance with the embodiment of the invention described previously with reference to Fig. 2 with different supply voltage V_{supply} values: the uppermost curve 16 of these corresponds to the on-resistance R_{on} of the transmission gate circuit portion 8 operated with a supply voltage V_{supply} of 1.62 V; the middle curve 18 corresponds to the on-resistance R_{on} of the transmission gate circuit portion 8 operated with a supply voltage of 3 V; and finally the lowermost curve 20 corresponds to the on-resistance R_{on} of the transmission gate circuit portion 8 operated with a supply voltage of 3.6 V.

20 As can be seen from the graph, the curves 16, 18, 20 corresponding to the on-resistance R_{on} of the transmission gate circuit portion 8 have a much shallower gradient than the curve 14 corresponding to the on-resistance R_{on} of the conventional transmission gate circuit portion 2. This shows that the on-resistance R_{on} of the transmission gate circuit portion 8 of the present invention is significantly more consistent across different input voltage V_{in} values. It can also be seen from the graph that increasing the supply voltage V_{supply} provided to the gate terminal of the nMOSFET 10 in the logic high state reduces the on-resistance R_{on} of the transmission gate circuit portion 8 and also reduces the rate at which the on-resistance R_{on} increases for increasing input voltage V_{in} .

30 The on-resistance R_{on} of the transmission gate circuit portion 8 is more linear than the conventional transmission gate circuit portion 2 due to the on-resistance of the nMOSFET 10 being lower than the on-resistance of the pMOSFET 12, on account of the gate-source, gate-drain, and gate-body breakdown voltages of the nMOSFET 10 being lower than the respective breakdown voltages of the pMOSFET 12. As
35 the on-resistance exhibited by the transmission gate circuit portion 8 is effectively

the parallel combination of the on-resistance of the nMOSFET 10 and the on-resistance of the pMOSFET 12, the on-resistance R_{on} of the transmission gate is dominated by the on-resistance of the nMOSFET 10.

5 The on-resistance of a regular transmission gate constructed from a conventional nMOSFET-pMOSFET pair typically decreases as the input voltage V_{in} increases because the on-resistances of both the conventional nMOSFET and pMOSFET decrease as V_{in} increases. However, the on-resistance behaviour of nMOSFET 10 is different to the on-resistance behaviour exhibited by a conventional nMOSFET as
10 V_{in} increases.

It is clear from the lowermost curve 20 (i.e. $V_{supply} = 3.6$ V) that the on-resistance R_{on} of the transmission gate circuit portion 8 is mainly dominated by the on-resistance of the nMOSFET 10 as the on-resistance of the nMOSFET 10 is much smaller than
15 on-resistance of the pMOSFET 12. Therefore, the on-resistance R_{on} of the transmission gate circuit portion 8 is increases as V_{in} increases.

With a lower supply voltage ($V_{supply} = 1.62$ V, uppermost curve 16), the on-resistance of the nMOSFET 10 is larger than in the $V_{supply} = 3.6$ V case. However,
20 the on-resistance of the nMOSFET 10 is still much smaller than the on-resistance of the pMOSFET 12. As such, the on-resistance R_{on} of the transmission gate circuit portion 8 increases as V_{in} increases.

Fig. 4 is a graph comparing a simulation of the off-resistance of the transmission
25 gate circuit portion 8 of Fig. 2 to the off-resistance R_{off} exhibited by the conventional transmission gate circuit portion 2 of Fig 1 across different input voltage V_{in} values. The graph shows a pair of curves 22, 24, wherein the uppermost curve 22 corresponds to the off-resistance R_{off} of the conventional transmission gate circuit portion 2 of Fig. 1 and the lowermost curve 24 corresponds to the off-resistance R_{off}
30 of the transmission gate circuit portion 8 of Fig. 2 in accordance with an embodiment of the present invention.

Some examples of the on-resistance R_{on} and off-resistance R_{off} values (i.e. the effective resistance of the transmission gate circuit portion 8 when it is switched on

and switched off respectively) typically presented for different values of the input voltage V_{in} and supply voltage V_{supply} are given below in Table 2:

V_{supply} (V)	V_{in} (V)	R_{on} (Ω)	R_{off} (G Ω)
1.62	2.5	155.4	25.75
1.62	4.35	199.6	26.36
3.6	2.5	73.27	25.75
3.6	4.35	93.26	26.36

Table 2: Comparison of on-resistance R_{on} and off-resistance R_{off} presented by the transmission gate circuit portion 8 for different supply voltage V_{supply} and input voltage V_{in} values.

Where the supply voltage V_{supply} is 1.62 V, the variation in on-resistance R_{on} between the cases where the input voltage V_{in} is 2.5 V and when the input voltage V_{in} is 4.35 V is $\pm 12\%$. For the case where the supply voltage V_{supply} is 3.6 V, the variation in the on-resistance R_{on} between the cases where the input voltage V_{in} is 2.5 V and when the input voltage V_{in} is 4.35 V is $\pm 12\%$. Those skilled in the art will appreciate that, compared to the variation of $\pm 27\%$ exhibited by the transmission gate circuit portion 2 of Fig. 1, the transmission gate circuit portion 8 of Fig. 1 provides an improved, more consistent on-resistance R_{on} across different input voltages V_{in} for a given supply voltage V_{supply} .

Furthermore, the variation in off-resistance R_{off} between the cases where the input voltage V_{in} is 2.5 V and when the input voltage V_{in} is 4.35 V, when the supply voltage V_{supply} is 1.62 V or 3.6 V is $\pm 1\%$, a substantial improvement over the variation of $\pm 14\%$ in the off-resistance R_{off} presented by the transmission gate circuit portion 2 of Fig. 1.

It can clearly be seen from the graph that the off-resistance R_{off} of the transmission gate circuit portion 8 is significantly more consistent across the range of input voltage V_{in} values than the off-resistance R_{off} of the conventional transmission gate circuit portion 2, i.e. the gradient of the lower curve 24 is greatly reduced compared to the gradient of the upper curve 22. This is because the off-resistance exhibited by the transmission gate circuit portion 8 is effectively the parallel combination of

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the off-resistance of the nMOSFET 10 and the off-resistance of the pMOSFET 12. As the nMOSFET 10 is effectively from a 'lower' device category but with a higher drain-source breakdown voltage, the nMOSFET 10 exhibit a smaller off-resistance than the conventional nMOSFET 4 used in the transmission gate circuit portion 2 of Fig. 1 (and, in this case, a smaller off-resistance than the pMOSFET 12). As such, the off-resistance of the transmission gate circuit portion 8 is dominated by the off-resistance of the nMOSFET 10.

Thus it will be appreciated by those skilled in the art that embodiments of the present invention provide an improved transmission gate circuit portion that presents more consistent on-resistance and off-resistance values across a range of input voltage values compared to conventional transmission gate circuit portions, therefore providing a transmission gate circuit portion with improved linearity performance. It will be appreciated by those skilled in the art that the embodiment described above is merely exemplary and is not limiting on the scope of the invention.

Claims

1. A transmission gate circuit portion arranged selectively to pass an input signal from an input node to an output node, said transmission gate comprising:
- 5 a control circuit portion arranged to provide first and second control voltages;
- a first field-effect-transistor having a drain terminal connected to the input node, a source terminal connected to the output node, and a gate terminal connected to the first control voltage, said first field-effect-transistor having a first
- 10 drain-source breakdown voltage, a first gate-source breakdown voltage, a first gate-drain breakdown voltage, and a first gate-body breakdown voltage; and
- a second field-effect-transistor having a drain terminal connected to the output node, a source terminal connected to the input node, and a gate terminal connected to the second control voltage, said second field-effect-transistor having a
- 15 second drain-source breakdown voltage, a second gate-source breakdown voltage, a second gate-drain breakdown voltage, and a second gate-body breakdown voltage;
- wherein the first drain-source breakdown voltage is substantially equal to the second drain-source breakdown voltage; and
- 20 wherein at least one of the first and second field-effect transistors has its respective drain-source breakdown voltage greater than its respective gate-source, gate-drain, and gate-body breakdown voltages of the respective field-effect-transistor.
- 25 2. The transmission gate circuit portion as claimed in claim 1, wherein the first drain-source breakdown voltage is greater than the first gate-source, gate-drain, and gate-body breakdown voltages.
- 30 3. The transmission gate circuit portion as claimed in claim 1 or 2, wherein the second drain-source breakdown voltage is greater than the second gate-source, gate-drain, and gate-body breakdown voltages.
4. The transmission gate circuit portion as claimed in any preceding claim, wherein at least one of the first and second field-effect-transistors is an n-channel
- 35 metal-oxide-semiconductor field-effect-transistor and the other of said first and

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second field-effect-transistors is a p-channel metal-oxide-semiconductor field-effect-transistor.

5 5. The transmission gate circuit portion as claimed in claim 4, wherein the first field-effect-transistor comprises an n-channel metal-oxide-semiconductor field-effect-transistor and the second field-effect-transistor comprises a p-channel metal-oxide-semiconductor field-effect-transistor.

10 6. The transmission gate circuit portion as claimed in any preceding claim, wherein the first field-effect-transistor is enhancement type.

7. The transmission gate circuit portion as claimed in any preceding claim, wherein the second field-effect-transistor is enhancement type.

15 8. The transmission gate circuit portion as claimed in any preceding claim, wherein the first drain-source breakdown voltage is between 5 V and 6 V.

20 9. The transmission gate circuit portion as claimed in any preceding claim, wherein the first gate-source breakdown voltage is between 3 V and 4 V.

10. The transmission gate circuit portion as claimed in any preceding claim, wherein the first gate-drain breakdown voltage is between 3 V and 4 V.

25 11. The transmission gate circuit portion as claimed in any preceding claim, wherein the first gate-body breakdown voltage is between 3 V and 4 V.

12. The transmission gate circuit portion as claimed in any preceding claim, wherein the second gate-source breakdown voltage is between 5 V and 6 V.

30 13. The transmission gate circuit portion as claimed in any preceding claim, wherein the second gate-drain breakdown voltage is between 5 V and 6 V.

14. The transmission gate circuit portion as claimed in any preceding claim, wherein the second gate-body breakdown voltage is between 5 V and 6 V.

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15. The transmission gate circuit portion as claimed in any preceding claim, arranged such that:

in a first mode of operation, the first control voltage is set to a non-zero value different to the input voltage and the second control voltage is set to zero; and

5 in a second mode of operation, the first control voltage is set to zero and the second control voltage is set to the input voltage.

16. The transmission gate circuit portion as claimed in any preceding claim, arranged to pass a voltage from a battery from the input node to the output node.

10

17. A method of operating a transmission gate circuit portion arranged selectively to pass an input signal from an input node to an output node said transmission gate comprising:

15 a control circuit portion arranged to provide first and second control voltages;

a first field-effect-transistor having a drain terminal connected to the input node, a source terminal connected to the output node, and a gate terminal connected to the first control voltage; and

20 a second field-effect-transistor having a drain terminal connected to the output node, a source terminal connected to the input node, and a gate terminal connected to the second control voltage;

wherein the method comprises:

25 in a first mode of operation, setting the first control voltage to a non-zero value different to the input voltage and setting the second control voltage to zero; and

in a second mode of operation, setting the first control voltage to zero and setting the second control voltage to the input voltage.

18. An electronic circuit portion comprising:

30 a battery having first and second terminals and providing a battery voltage; and

a transmission gate circuit portion arranged selectively to pass the battery voltage from an input node to an output node, said transmission gate comprising:

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a first field-effect-transistor having a drain terminal connected to the input node, a source terminal connected to the output node, and a gate terminal connected to a first control voltage; and

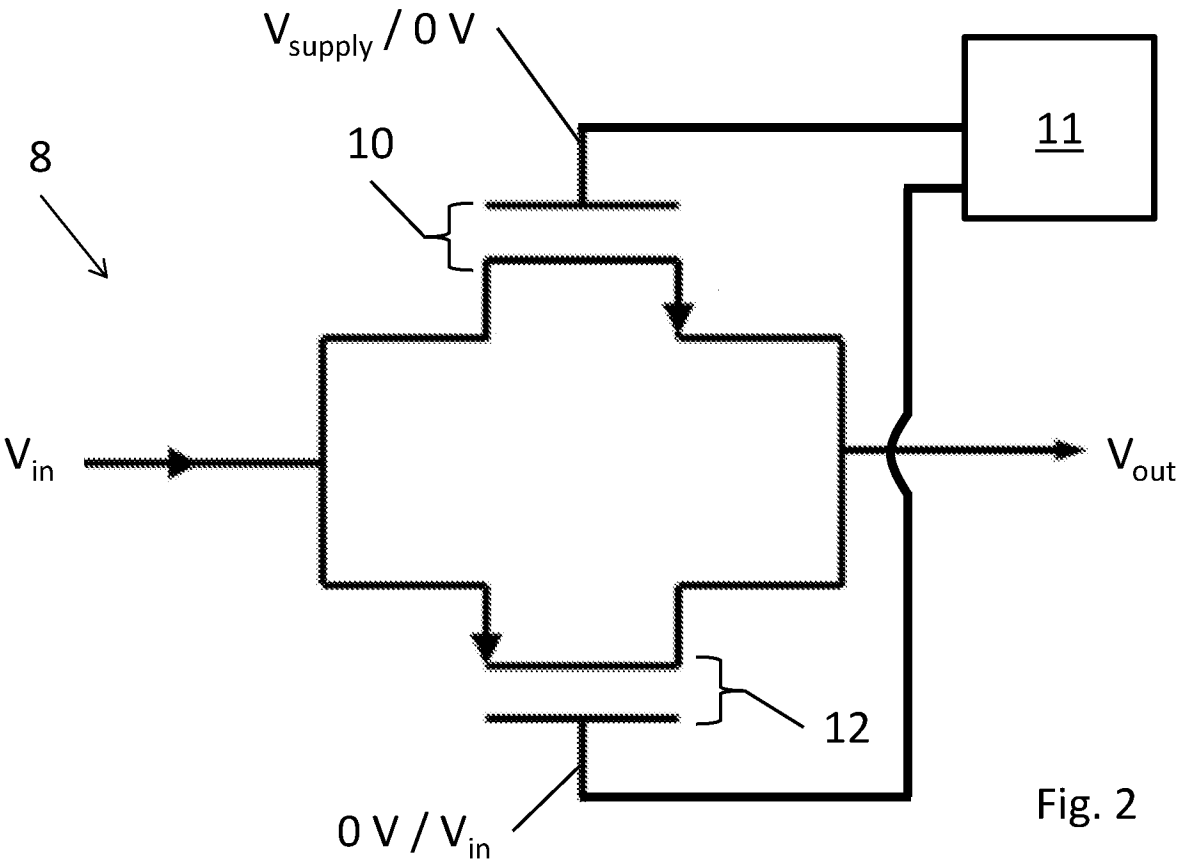
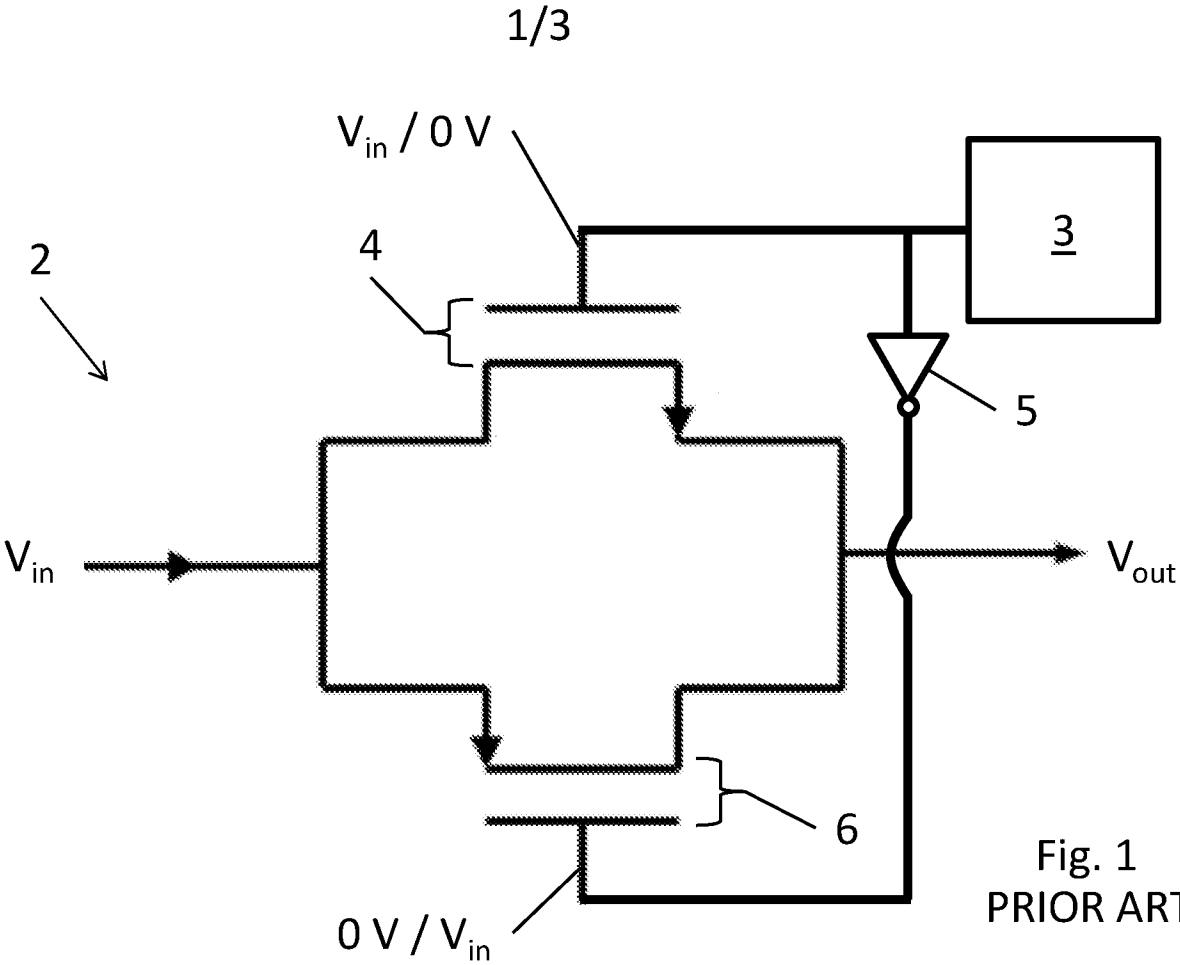
5 a second field-effect-transistor having a drain terminal connected to the output node, a source terminal connected to the input node, and a gate terminal connected to a second control voltage;

wherein the transmission gate circuit portion is arranged such that:

in a first mode of operation, the first control voltage is set to a non-zero value different to the battery voltage and the second control voltage is set to zero;

10 and

in a second mode of operation, the first control voltage is set to zero and the second control voltage is set to the battery voltage.



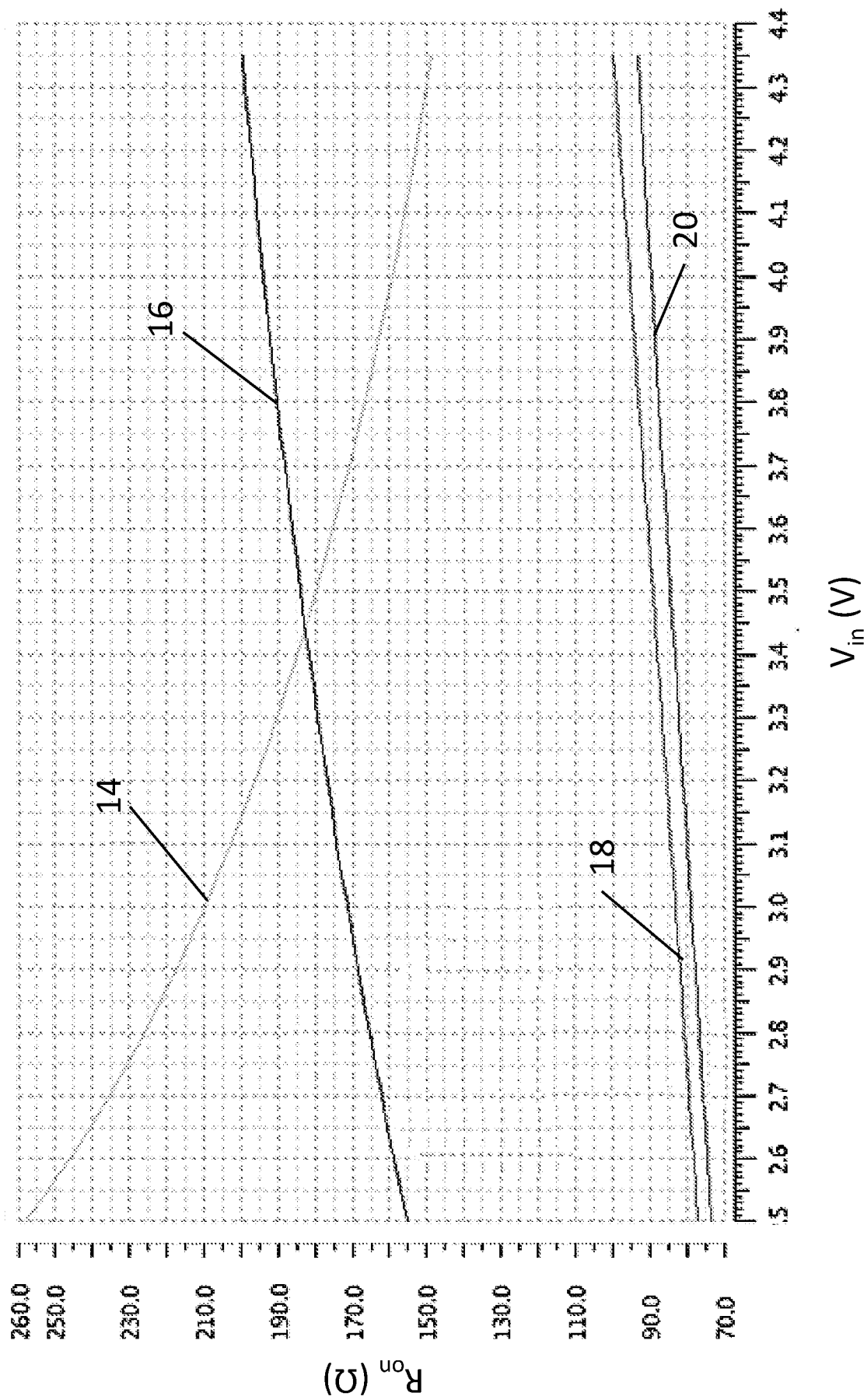


Fig. 3

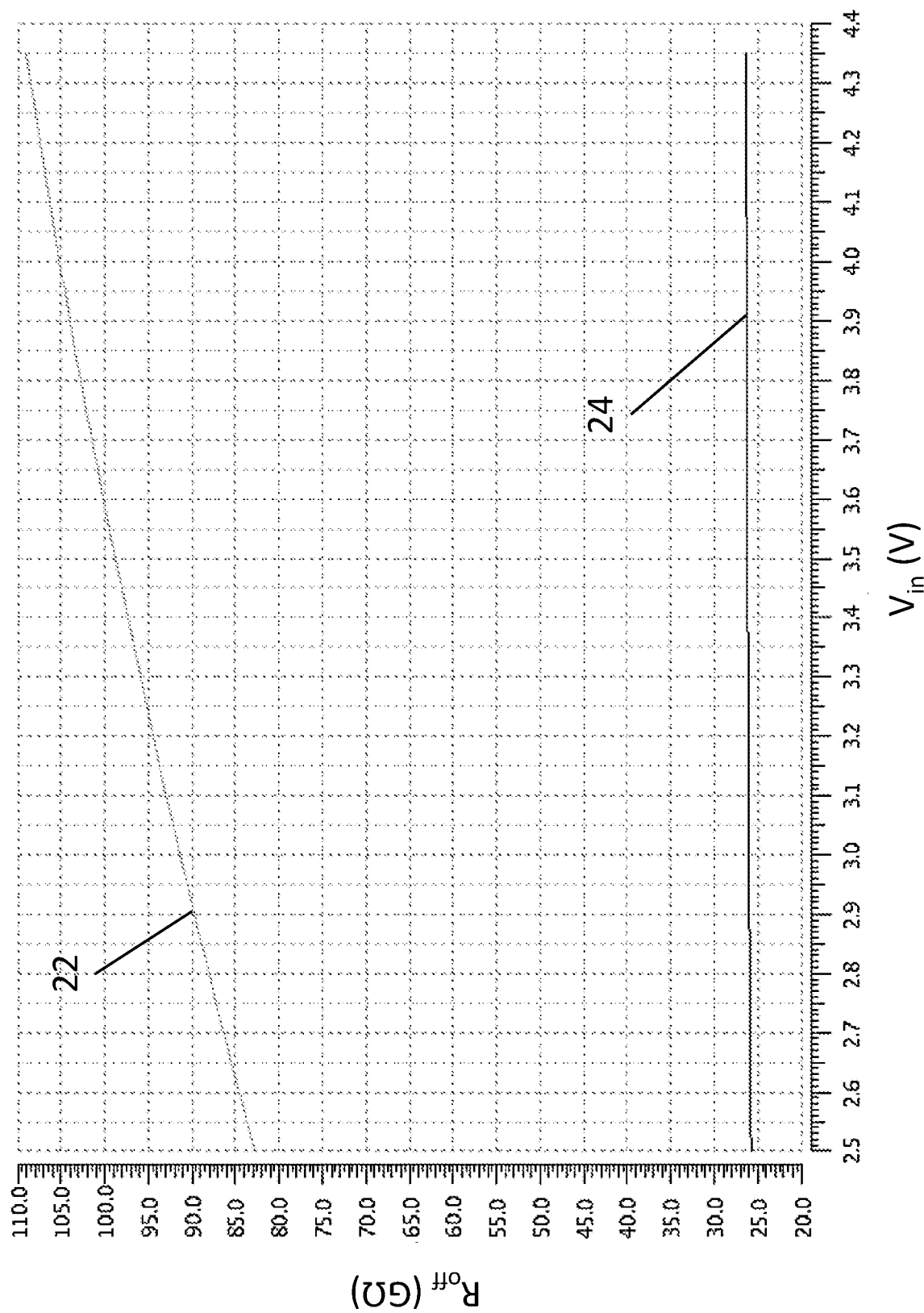


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2018/053239

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/0812
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 037 798 A (HEDBERG MATS [SE]) 14 March 2000 (2000-03-14) column 8, line 26 - column 9, line 6; figure 6B	1-16
Y	----- Mosfet Basics: "AN-9010", , 4 September 2013 (2013-09-04), XP055541448, Retrieved from the Internet: URL:http://www.onsemi.com/pub/Collateral/A N-9010.pdf.pdf [retrieved on 2019-01-14] pages 1-11 -----	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

16 January 2019

Date of mailing of the international search report

20/03/2019

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2018/053239

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-16

Transmission gate circuit with two field effect transistors and a control circuit, with certain specific relations between breakdown voltages

2. claims: 17, 18

Transmission gate circuit with two field effect transistors and a control circuit for use with a battery, wherein the transmission gate is controlled with specific voltage values based on the battery voltage.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2018/053239

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6037798	A	14-03-2000	NONE
