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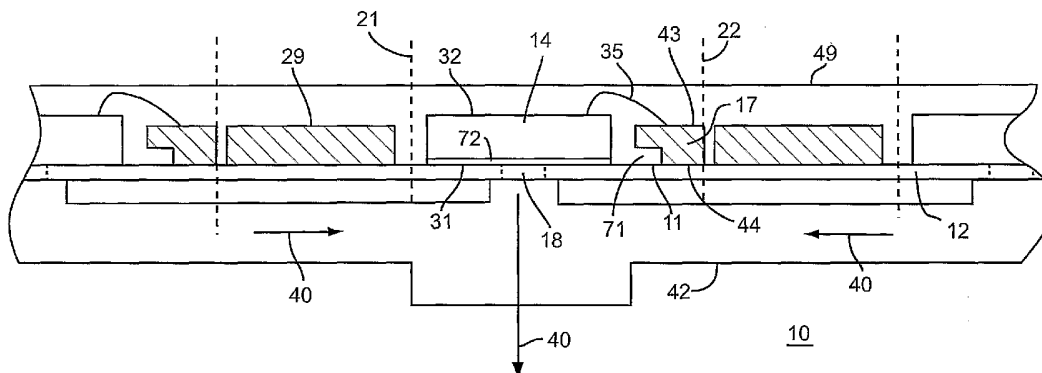
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MAKING A LOW PROFILE PACKAGED SEMICONDUCTOR DEVICE



(57) Abstract: A semiconductor device (10) is made by mounting the bottom surfaces (31, 44, 54) of a semiconductor die (14) and a lead (15, 17) on a tape (12) and over a hole (19) in the tape. A vacuum is drawn through the hole to secure the die in place when the lead's top surface (43) is wirebonded to a top surface (32) of the semiconductor die. A molding material (49) is formed to encapsulate the top surface of the semiconductor die and to expose its bottom surface.

METHOD OF MAKING A LOW PROFILE PACKAGED SEMICONDUCTOR DEVICE

Background of the Invention

5 **[0001]** The present invention relates in general to semiconductor devices and, more particularly, to semiconductor dice housed in low profile packages.

[0002] There is a continuing demand for electronic systems with a higher functionality and smaller physical
10 size. For example, successive generations of personal computers are specified to utilize motherboards of a decreasing while incorporating more features and operating at lower voltages but a higher power consumption. The power requirements often are met by using multiple local voltage
15 regulators located at several locations on each motherboard.

[0003] The multiple voltage regulators typically are implemented as switching regulators that include an integrated control circuit and, to accommodate the high current levels, multiple parallel-connected discrete power
20 switching transistors. A problem with this arrangement is that with each generation the multiple power switching transistors occupy larger portions of smaller motherboards, which reduces the area available for implementing other functions.

25 **[0004]** Some previous power transistors connect their semiconductor dice to package leads using wirebonds, but do not mount the dice on die attach flags. These devices have poor yields, and a resulting high cost, because the die is not adequately secured in position during the wirebond
30 process. If a die moves while a wirebond is being attached, the die could

[0005] Hence, there is a need for a packaged semiconductor device that has a small physical size and high

efficiency to alleviate the above mentioned problems.

5

Brief Description of the Drawings

[0006] FIG. 1 is an exploded isometric view of a semiconductor device during a first stage of fabrication;

FIG. 2 is a cross-sectional side view of the semiconductor device and a portion of an assembly apparatus at a second stage of fabrication;

FIG. 3 is an isometric view of the semiconductor device after completion of a singulation process;

FIG. 4 is a bottom view of the semiconductor device; and

FIG. 5 is a cross-sectional side view of a portion of an electrical system including the semiconductor device.

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Detailed Description of the Drawings

[0007] In the figures, elements having the same reference number have a similar structure and functionality. Similar elements associated with a particular reference number may be described in either the plural or general sense or in the singular or specific sense, depending on the context.

[0008] FIG. 1 is an exploded isometric view of a semiconductor device 10 being assembled on a mounting tape 12 at a first fabrication stage. Semiconductor device 10 is formed with a leadframe or leadframe matrix 16 and one or more semiconductor chips or dice 14. In one embodiment, semiconductor dice 14 are substantially identical semiconductor substrates on which standard semiconductor wafer processes are performed to produce a plurality of

power transistors.

[0009] Mounting tape 12 comprises a standard semiconductor package assembly tape having an adhesive surface 11 for holding mounted components in position during the assembly process. An array of holes 18 are punched or otherwise formed in tape 12 at predefined locations determined by the package size and other factors. Holes 18 may be formed *in situ* with a computer-controlled hole punch apparatus just prior to mounting package components, or may be purchased commercially in a pre-punched form from a tape manufacturer or vendor. Tape 12 preferably is formed with materials that can withstand the temperatures needed to complete the package assembly. For example, in one embodiment, the highest temperature occurs during the encapsulation process during which an epoxy-based or plastic mold compound is dispensed and cured at a temperature of about one hundred eighty degrees Celsius. In one embodiment, tape 12 is made of a polyester-backed acrylic adhesive and formed with holes 18 of a diameter of about one thousand five hundred micrometers. Alternatively, tape 12 may comprise silicone and/or acrylic adhesive with a polyester, polyimide or polytetrafluoroethylene (PTFE) backing. Tape 12 may also be formed with an adhesive material applied to a metal foil such as an aluminum foil.

[0010] Leadframe matrix 16 has an X-Y array of regions that define individual leadframes, including a leadframe defined by singulation along cut lines 21-24 and severed after assembly to form a plurality of packaged integrated circuits or transistors. In the embodiment of FIG. 1, leadframe matrix 16 is patterned such that, for example, leadframe 20 is formed with leads 15 and 17 and an opening 19. A region 29 between adjacent leadframes functions as a tie bar to maintain the position of leads 15 and 17 in

relation to opening 19 during assembly. In one embodiment, leadframe matrix 16 is stamped or etched from a sheet of rolled copper having a thickness in a range between about one hundred and five hundred micrometers and a typical
5 thickness of about two hundred micrometers. Leadframe matrix 16 is mounted on a region 27 of adhesive surface 11, with openings 19 aligned with regions 26 of mounting tape 12 that are generally centered around holes 18. Hence, leadframe matrix 16 is mounted directly on adhesive surface
10 11 so that holes 18 are exposed or visible through openings 19.

[0011] Openings 19 have a larger area than the area of semiconductor dice 14 to allow a standard pick-and-place apparatus (not shown) to mount semiconductor dice 14
15 directly on adhesive surface 11 within openings 19 and over holes 18. The size of openings 19 is selected taking into account the die size, the requirements of the pick-and-place apparatus and any alignment tolerance necessary for a saw or other singulation tool to avoid damaging dice 14 during the
20 subsequent singulation process.

[0012] FIG. 2 is a cross-sectional side view of semiconductor device 10 after a second fabrication stage, and showing tape 12 mounted on a portion of an assembly apparatus that includes a vacuum system 42.

25 **[0013]** A vacuum pump (not shown) pulls a vacuum in a direction indicated by arrows 40 through ducts of vacuum system 42 to produce a low pressure at holes 18 for securing the positions of semiconductor dice 14 and compensating for any elasticity or movement of tape 12 during subsequent
30 wirebonding. Once the vacuum is drawn, a wirebonding machine attaches bonding wires 35 from a top surface 43 of lead 17 to a top surface 32 of semiconductor die 14. Similar wire bonds are attached from lead 15 to top surface

32 as shown and described below.

[0014] After wirebonding, semiconductor device 10, with tape 12 attached, is placed on the floor of a molding chamber (not shown) into which is introduced a molding material 49 such as a plastic material or thermoset epoxy. Molding material 49 is formed as a continuous body that encapsulates top surfaces 32 of semiconductor dice 14, top surfaces 43 of leads 17 and the top surfaces of leads 15 (not shown in FIG. 2). Tape 12 is secured to surfaces of semiconductor device 10 so as to block molding material 49 from seeping through to reach holes 18, thereby preventing mold flash from forming on bottom surface 31 of semiconductor dice 14.

[0015] Bottom surface 31 of semiconductor die 14 is formed during wafer processing with a solderable layer 72 for mechanically and electrically attaching to an external surface. Bottom surfaces 31, bottom surfaces 44 of leads 17 and bottom surfaces 54 of leads 15 (shown in FIGs. 3-4) are attached to tape 12 during the encapsulation or molding process and, as a consequence, are masked by tape 12 to prevent their being covered by molding material 49. Hence, bottom surfaces 31, 44 and 54 are exposed for making external electrical and mechanical connections after tape 12 is removed. If necessary, semiconductor device 10 is subjected to a cleaning process to remove any residue of tape 12 or its adhesive material to ensure that bottom surfaces 31, 44 and 54 are fully exposed and free of material that could prevent or reduce electrical contact to external surfaces.

[0016] Note that leadframe matrix 16 is subjected to a half-etch or similar process to form mold locks 71 that prevent molding material 49 from separating from leads 15 and 17 during subsequent processing or while semiconductor

device 10 is being used or operated. In one embodiment, mold locks 71 have a generally rectangular reentrant shape as shown.

[0017] Leads 15 and 17, and in fact leadframe matrix 16, are made to a thickness less than the thickness of semiconductor dice 14. For example, in one embodiment, semiconductor dice 14 have a thickness of about two hundred micrometers, while leads 15 and 17 have a thickness of about one hundred twenty-five micrometers. This thickness difference allows bonding wires 35 to be formed with a small loop height to reduce the overall thickness or height of semiconductor device 10. In an embodiment in which semiconductor dice 14 have a thickness of two hundred micrometers, the loop height is about four hundred eighty micrometers from the peak of bonding wires 35-36 to top surface 32 of semiconductor die 14, and the overall height of semiconductor device 10 is about eight hundred micrometers.

[0018] FIG. 3 is an isometric view of semiconductor device 10 after removing tape 12 and sawing along cut lines 21-24 to complete the singulation process. In one embodiment, semiconductor die 14 is configured as a power transistor operating at a specified source-drain current greater than one ampere and housed in a singulated package 70 that includes leads 15 and 17, bonding wires 35 and 36 and molding material 49.

[0019] Semiconductor die 14 has a gate electrode coupled to a gate bonding pad 51 and a source electrode coupled to a source bonding pad 52, both formed on top surface 32 of semiconductor die 14. Solderable layer 72 is formed on bottom surface 31 during wafer processing to function as a drain terminal. In one embodiment, solderable layer 72 is formed with a titanium-nickel-silver alloy. Bottom surface

31 is exposed, i.e., not encapsulated by molding material 49, so solderable layer 72 allows bottom surface 31 to function as a package lead that can be attached by a solder reflow or other process for making external connections.

5 **[0020]** Where semiconductor device 10 comprises a vertical power transistor, multiple bonding wires 35 are attached in parallel between source bonding pad 52 and top surface 43 of lead 17 to reduce the on-resistance. The gate current is transient in nature and generally of a lower amplitude, so a
10 single bonding wire 36 attached between gate bonding pad 51 and lead 15 is generally adequate to ensure a high performance.

15 **[0021]** Note that bottom surface 31 of semiconductor die 14, bottom surface 44 of lead 17 and a bottom surface 54 of lead 15 are all coplanar and exposed from molding material 49 to facilitate external connectivity.

20 **[0022]** Tabs 55-56 project from leads 15 and 17, respectively, and are remnants of the tie bar of region 29, remaining on leads 15 and 17 as artifacts of the sawing or singulation process.

25 **[0023]** The exposure of bottom surface 31 of semiconductor die 14 and the reduced loop height of bonding wires 35-36 provide package 70 of semiconductor device 10 with a low profile. In one embodiment, semiconductor device 10 has an overall height of about eight hundred micrometers.

30 **[0024]** FIG. 4 is a bottom view of semiconductor device 10 showing bottom surface 31 of semiconductor die 14 as being exposed for making external electrical connections along with bottom surface 54 of lead 15 and bottom surface 44 of lead 17. Bottom surfaces 31, 44 and 54 are all coplanar.

35 **[0025]** FIG. 5 shows a cross-sectional side view of a portion of an electronic system, including semiconductor device 10 mounted on a motherboard 60.

[0026] Motherboard 60 is formed with a trace 61 to which is attached lead 17 and a trace 62 for attaching to bottom surface 31 of semiconductor die 14. In one embodiment, lead 17 and bottom surface 31 are attached to traces 61-62 by reflow soldering.

[0027] The exposure of bottom surface 31 of semiconductor die 14 results in a low thermal resistance since heat does not flow through a die attach pad and its associated metallurgical junctions as in other packaged devices. This benefit is particularly apparent in an embodiment in which a large portion of the power is generated throughout the bulk of semiconductor die 14, rather than at top surface 32.

[0028] Thermal resistance is further reduced by the low package profile of semiconductor device 10 because of the short distance from semiconductor die 14 to a top surface 65 of molding material 49. In some applications, it is advantageous to mount an external heat sink (not shown) to top surface 65 to further aid in dissipating power. Note also that trace 62 is formed to extend outwardly from semiconductor device 10. This arrangement exposes a portion of trace 62 to ambient air currents to further facilitate the removal of power P_D dissipated by semiconductor device 10.

[0029] Moreover, by mounting bottom surface 31 of semiconductor die 14 directly to trace 62, the electrical resistance is reduced since the distance from trace 62 to bottom surface 31 is virtually zero. Indeed, current flows from the bulk substrate of semiconductor die 14 through solderable layer 72 directly to trace 62. Hence, current flowing through semiconductor device 10 encounters no die attach flag and flows through fewer metallurgical junctions, which results in a lower on-resistance than is the case with other devices. The lower on-resistance provides a high

performance and efficiency by further reducing the dissipated power P_D .

[0030] By now it can be seen that the present invention provides a packaged semiconductor device with a low profile and a low electrical and thermal resistance. A lead has a first surface for wirebonding to a first surface of a semiconductor die and a second surface substantially coplanar with a second surface of the semiconductor die. A molding material encapsulates the first surface of the semiconductor die and exposes the second surface of the semiconductor die. The semiconductor die and lead are disposed on a mounting tape to maintain their position during the packaging assembly process. The semiconductor die is secured during package assembly by positioning over a hole in the mounting tape and applying a vacuum through the hole to obviate any movement or elasticity in the mounting tape while pressure is applied to the die by the wirebonding tool during the wirebonding process.

[0031] The present invention provides a packaged semiconductor device with a high reliability and low cost. Because the semiconductor die is exposed to function as a lead, there is no die attach pad and therefore no solder reflow die attach process is needed. Hence, the semiconductor device can be assembled in a wider variety of manufacturing locations and at a lower cost. Moreover, fewer dissimilar component materials and therefore fewer dissimilar temperature coefficients of expansion within the semiconductor device. Consequently, internal stresses are reduced and reliability enhanced. Finally, the semiconductor device can be formed with a smaller footprint because there is no need to align and mount the semiconductor die on a die attach pad that is made larger to avoid die overhang.

CLAIMS

What is claimed is:

1. A method of making a semiconductor device, comprising:
5 mounting a semiconductor die on a tape and over a hole in the tape;
drawing a vacuum through the hole to secure the semiconductor die; and
attaching a wirebond to a first surface of the
10 semiconductor die while drawing the vacuum.
2. The method of claim 1, further comprising:
disposing a lead on the tape; and
attaching the wirebond to the lead.
- 15 3. The method of claim 2, further comprising encapsulating the wirebond in a molding compound.
4. The method of claim 3, wherein encapsulating includes:
20 encapsulating a portion of the lead; and
encapsulating a portion of the semiconductor die.
5. The method of claim 4, wherein encapsulating a portion of the semiconductor die includes coating the semiconductor
25 die with an encapsulant so as to expose a second surface of the semiconductor die.
6. The method of claim 5, wherein encapsulating a portion of the lead includes coating the lead with an encapsulant so
30 as to expose a surface of the lead.
7. The method of claim 6, wherein mounting the semiconductor die includes mounting the second surface of

the semiconductor die to a surface of the tape.

8. The method of claim 7, wherein disposing the lead includes mounting the surface of the lead to the surface of the tape such that the second surface of the semiconductor die and the surface of the lead are coplanar.

9. A method of making a semiconductor device, comprising:
mounting a semiconductor die over a hole in a tape; and
drawing a vacuum through the hole while wirebonding the semiconductor die.

10. The method of claim 9, wherein mounting includes disposing a first surface of the semiconductor die on a surface of the tape.

11. The method of claim 10, further comprising:
disposing a lead on the surface of the tape; and
coupling a bonding wire from a second surface of the semiconductor die to the lead.

12. The method of claim 11, wherein disposing the lead includes placing a first surface of the lead on the surface of the tape in a plane with the first surface of the semiconductor die.

13. The method of claim 12, wherein coupling the bonding wire includes attaching the bonding wire to a second surface of the semiconductor die and a second surface of the lead.

14. The method of claim 9, further comprising encapsulating the bonding wire and the second surfaces of the semiconductor die and the lead with an encapsulant.

15. The method of claim 14, wherein encapsulating includes covering the first surfaces of the semiconductor die and the lead with the tape to block the encapsulant.

5

16. The method of claim 15, wherein encapsulating further includes coating the second surfaces of the semiconductor die and the lead with the encapsulant while exposing the first surfaces of the semiconductor die and the lead.

10

17. A method of packaging a semiconductor die, comprising drawing a vacuum through a hole in a tape to maintain a position of a semiconductor die while wirebonding the semiconductor die to a lead.

15

18. The method of claim 17, wherein the lead is provided in a leadframe, further comprising:

mounting the semiconductor die directly on a surface of the tape to cover the hole; and

20

mounting the leadframe on the surface. attach

19. The method of claim 18, wherein mounting the leadframe includes mounting the leadframe directly on the adhesive surface to expose the hole through an opening of the leadframe.

25

20. The method of claim 19, wherein mounting the semiconductor die includes mounting the semiconductor die within the opening of the leadframe.

30

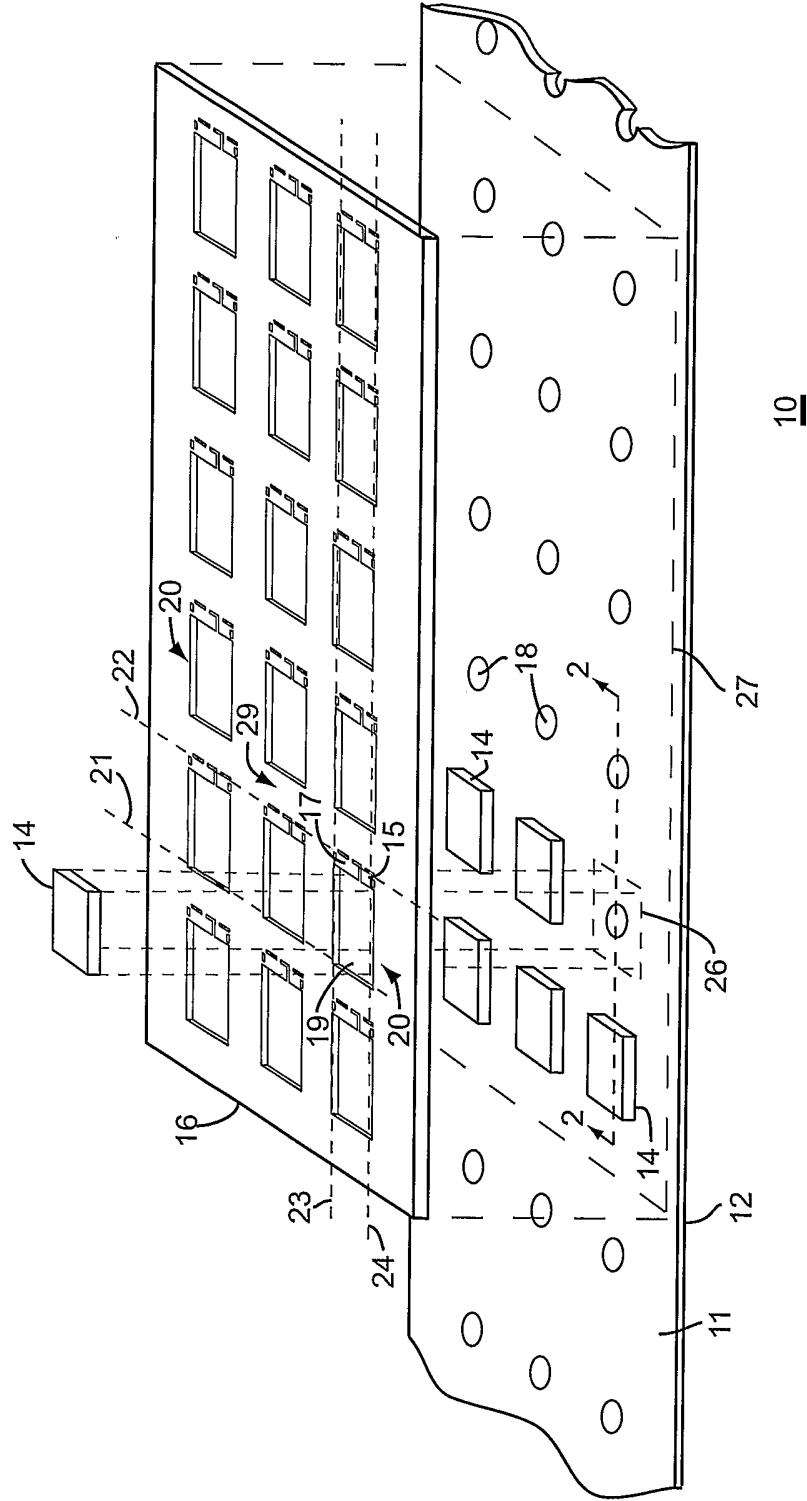


FIG. 1

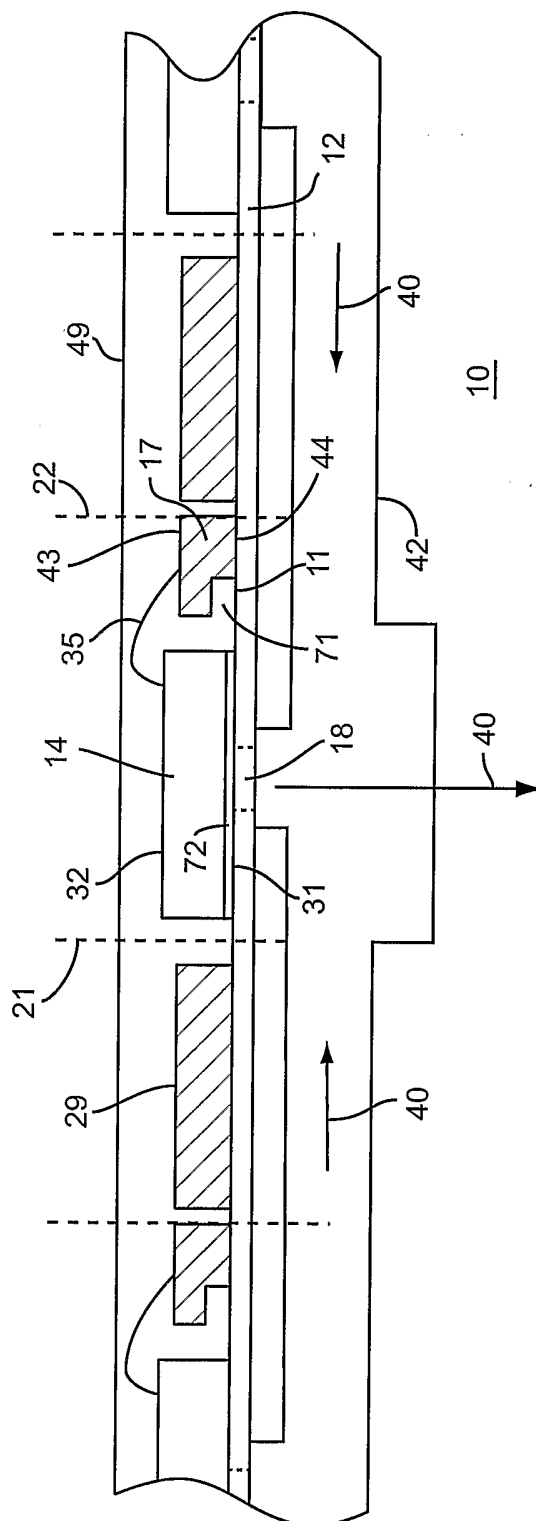


FIG. 2

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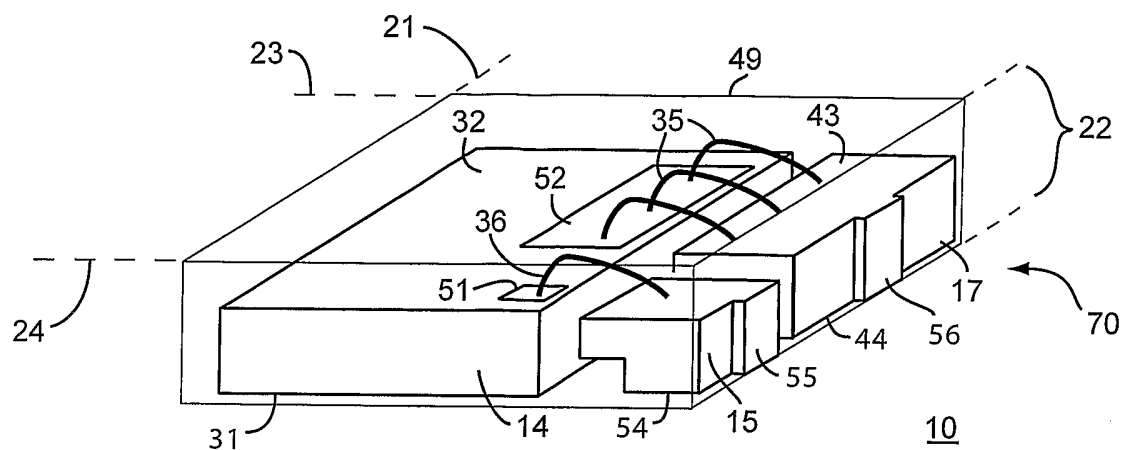


FIG. 3

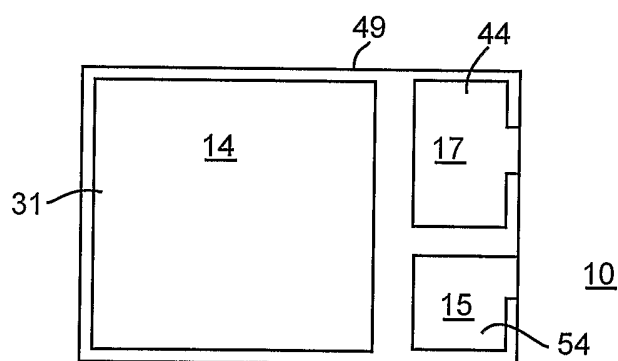


FIG. 4

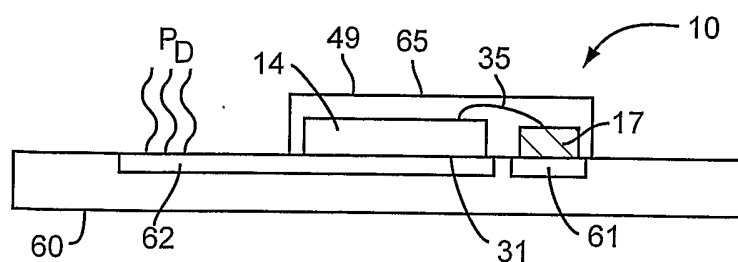


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 03/13027

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H01L21/68 H01L21/56 H01L21/607

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

WPI Data, EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 258 632 B1 (TAKEBE NAOTO) 10 July 2001 (2001-07-10) column 1, line 20-30 column 4, line 60 -column 5, line 16; figures 8A,8B	1,9,17
A	column 5, line 43-53; figures 11A-11C column 7, line 20-39; figures 16A-16C column 7, line 47-56; figures 17A,17B	1-20
A	US 2002/100163 A1 (KO SHARON MEI WAN ET AL) 1 August 2002 (2002-08-01) column 1, paragraph 2 paragraph '0003!; figure 1 paragraph '0020!; figure 6	1-20
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Internat Application No
PCT/US 03/13027

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 001 671 A (FJELSTAD JOSEPH) 14 December 1999 (1999-12-14) column 1, line 30-41 column 2, line 15-41 column 3, line 53 -column 4, line 4; figures 1A-1G column 4, line 32 -column 5, line 2 ---	1-20
A	US 6 069 408 A (WATANABE TAKANORI ET AL) 30 May 2000 (2000-05-30) column 12, line 1-38; figures 10,11 column 2, line 42-57 -----	1-20

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International Application No

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