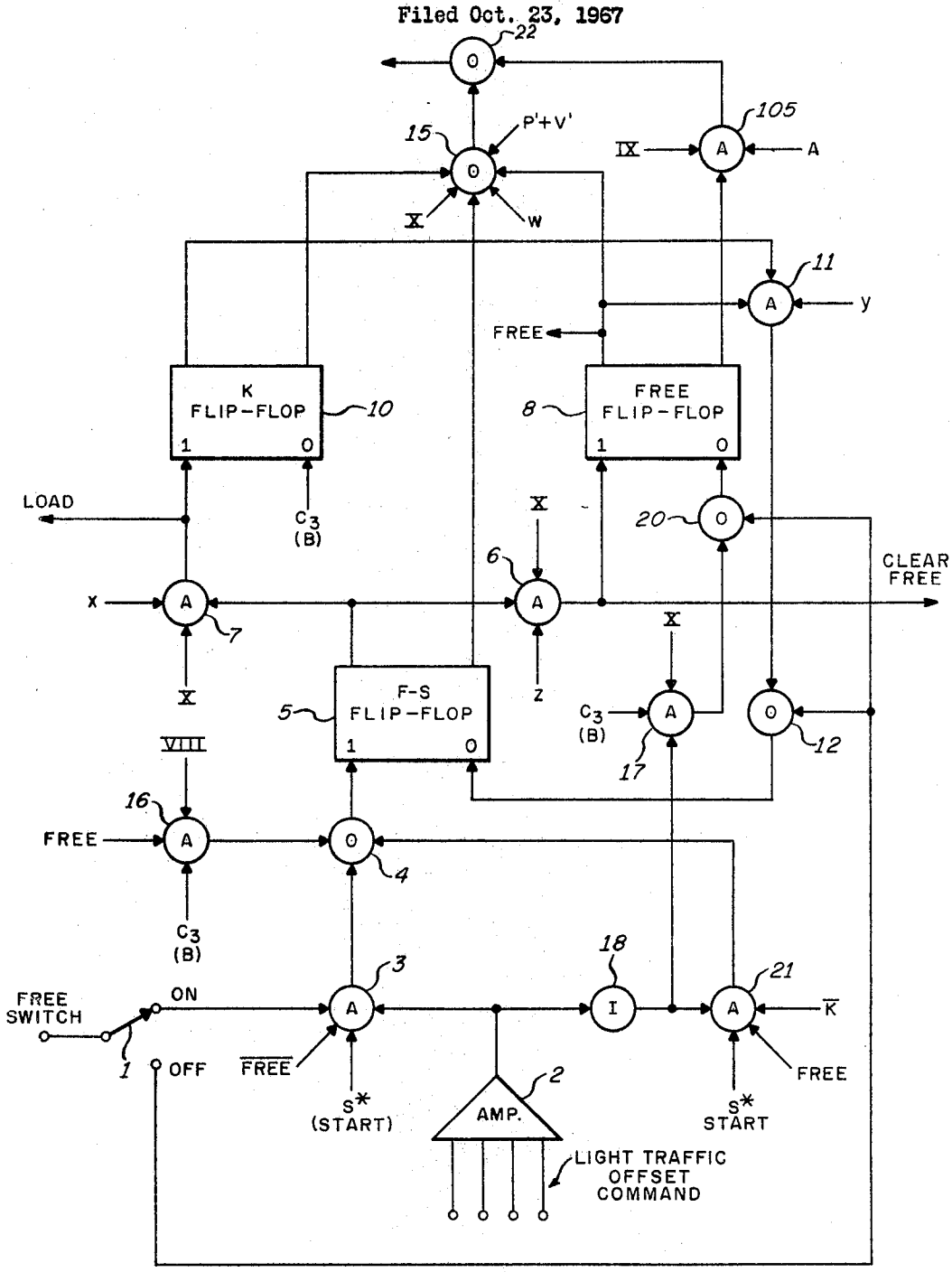
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APPARATUS FOR VEHICULAR TRAFFIC INTERSECTION CONTROLLERS

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APPARATUS FOR VEHICULAR TRAFFIC INTERSECTION CONTROLLERS

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ABSTRACT OF THE DISCLOSURE

Apparatus for traffic intersection controllers when the controller transfers to, operates in, or transfers from a non-coodinated or free mode of operation which assures that the major traffic phase is accorded with a minimum right-of-way interval for each non-coordinated cycle as well as during the transition period.

BACKGROUND OF THE INVENTION

Field of the invention

The present invention pertains to apparatus for traffic intersection controllers of the semi-actuated type for providing proper actuation during conditions of light traffic density as well as during transition periods.

Description of the prior art

In a coordinated traffic control system, the local intersection controllers in a section operate with the same background cycle and with a particular set of offset values depending on the density of traffic. When the traffic density changes, the central controller changes the set of offset values on which the controllers in the section operate. For a particular offset value, a controller in the section has a preset time during the background cycle at which to initiate its local cycle. Some controllers in the section are of the non-actuated variety; that is, they continuously effectuate a local cycle in accordance with the background cycle and the selected local offset values. Other controllers in the section are of the semi-actuated type; that is, they continuously display a green indication for the major traffic phase and a red indication for the itnersecting traffic phases until a local actuation is received from a vehicle or a pedestrian. The controller then waits for its coordinated preset time in the background cycle to initiate a local cycle. The semi-actuated controller initiates local cycles only when demanded and they are timed in accordance with the background cycle and the selected local offset value.

During conditions of light traffic density, it is often desirable to free the semi-actuated controller from the requirement to wait for a preset time in the background cycle to initiate its local cycle. It would be advantageous, under these circumstances, to initiate the cycle immediately upon receipt of an actuation. Thus, semi-actuated controllers are provided with a two-position switch for selecting the coordinated or the free condition for the local operation mode. When the switch is positioned to select the free mode, the controller operates in the coordinated mode until the central controller selects the light traffic offst values for the section. At this time, the controller commences to operate in the free mode. When the traffic density increases so as to cause the central controller to select other than the light traffic offset values, the controller reverts to the coordinated mode of operation.

When operating in a free mode, a semi-actuated controller times a local cycle in response to an actuation and thereafter remains in a rest interval until receipt of another actuation. During the rest interval, a green indication is displayed to the main traffic phase. Should traffic on the secondary phase be continuous, the controller would continually execute local cycles remaining in the rest interval only momentarily. Thus the right-of-way would be continuously accorded to the secondary phase and only momentarily to the main phase. Therefore, any vehicle arriving at the intersection on the major phase would have to wait until all of the vehicles on the secondary phase have cleared the intersection before proceeding.

To avoid this anomalous condition, when operating in the free mode, controllers at attaining the rest interval after executing a local cycle, insert an interval which accords the right-of-way to the major traffic phase for a preset duration before reverting to vehicle passage on the secondary phase. Thus, despite the traffic density on the secondary phases, the right-of-way will be given to the major phase once for each cycle executed when operating in the free mode.

When operating in either the coordinated or the non-coordinated mode, controllers operate properly. However, when executing the transition between modes, the transitional cycle may be severely distorted. For example, a controller operating in the free mode, when entering the dwell interval after executing a local cycle, begins to display the right-of-way signal to the major phase. If at this time, the command to revert to the coordinated mode is received and the signal to begin a coordinated local cycle is also received, the right-of-way for the major phase may be abruptly terminated. Vehicles waiting on the major phase and vehicles arriving on the secondary phase may, under these circumstances, enter the intersection simultaneously with potentially catastrophic results.

SUMMARY OF THE INVENTION

The present invention overcomes the problems explained above by providing in a semi-actuated intersection controller responsive to mode signals, the means for timing an interval including inhibiting means effective to inhibit initiation of a non-coordinated cycle until the interval is timed and initializing means for actuating the timing means at the coincidence of a non-coordinated mode command signal and the dwell interval of the controller cycle as well as control means for actuating the timing means once for each initiated non-coordinated cycle and means for inhibiting the termination of the non-coordinated mode when the timing means are activated.

BRIEF DESCRIPTION OF THE DRAWINGS

The single drawing is a schematic diagram of the apparatus incorporating the present invention applied to a semi-actuated traffic intersection controller.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will be described for purposes of example with respect to the semi-actuated type of traffic intersection controller of the character explained in U.S. patent application Ser. No. 453,072 now abandoned entitled Traffic Intersection and Other Signal Controllers Responsive to a Cyclic Pulse Train, filed May 4, 1965 in the name of John J. King which may be used in conjunction with a system of the type described in U.S. patent application Ser. No. 452,974 now abandoned entitled Control System for Controlling Vehicular Traffic Flow or Other Moving Elements, filed May 4, 1965 in the name of John J. King et al.

The present invention provides apparatus for use in a semi-actuated type of intersection controller responsive to command signals representative of various traffic densities at the local intersection which can transfer between system

modes predetermined and selectable parameters while maintaining synchronism with the individual intersection cycle. The system operation of the semi-actuated controller is such that it must be capable of operating interchangeably between three system modes, i.e., the coordinated mode, the free mode and the standby mode. Further, the central site may be capable of switching between two of these modes, such as the coordinated and free modes by means of communication command signals.

In the coordinated mode of operation, the local intersection cycle of a particular controller, i.e., the transferring of green time from one street to the other is determined by a combination of switch settings on the switch panel of the local controller and the communication information received from the central site, i.e., offset command, split command, background start and cycle length, as explained in detail in said patent applications S.N. 452,974 and 453,072. In the free mode, the local controller uses a combination of switch settings, different from those used in the coordinated mode, to determine the local intersection cycle. The controller also uses less communication information than in the coordinated mode, i.e., split command and cycle information. The controller is also more responsive to local intersection traffic in the free mode than in the coordinated mode; rather than being capable of responding to traffic calls for 10% of the cycle as in the coordinated mode, the controller can now respond at any point within the cycle.

In a particular controller, the conditions required for free mode operation are that the free switch be in the ON position, and that it be operating on a light traffic offset command. The free switch is usually set when the controller is installed at a particular intersection. The offset communication from the central site usually connects to numerous local intersection controllers. Then, when the central site changes to light traffic offset command, the individual intersection controllers are in different portions of their local intersection cycle. Thus, the transferring to the free mode can be random in its occurrence with respect to an individual local intersection cycle. Conversely, the same will be true when transferring out of the free mode.

Inconsistencies may occur during the transitional period because of the meshing of the two types of local intersection cycles which among other things can cause a disjointed local intersection cycle. Also in the transitional period, the major phase green time changes from a constant (switch settable) to a variable function of the local intersection traffic density that can under certain conditions reduce to zero.

The present invention overcomes the aforementioned problems by establishing two conditions for the controller's response during the transitional period. First, the transfer of operation takes place before the beginning of the next local intersection cycle, and second, the major phase green time during the transition is a minimum value settable through a controller panel switch. The circuit shown in the drawing satisfies these conditions.

Referring now to the drawing, the operation of the present invention will be explained first with respect to the transition of the controller to the free mode of operation. The free switch **1** is in the ON position as shown. The light traffic offset command is received from the central site on four communication lines connected to an AND gate **2**. The light traffic offset command enables the AND gate **2**. The next background start signal S* will guide the received signal through gating to set a transition memory cell in a manner to be explained. The S* signal is generated by the background start pulse as described in said U.S. patent application S.N. 453,072. An AND gate **3** is then enabled with all its input terminals energized since the free switch **1** is in the ON position, the controller is not yet in the free mode thereby providing a $\overline{\text{FREE}}$ signal, the S* signal is present and there is an output from the AND gate **2**. The output of the AND gate **3** enables an OR gate **4** which sets the transition memory cell FREE START (F.S.) flip-flop **5**. This is kept in the transition memory cell **5** until the local intersection cycle of the controller is finished. Then a minimum green period, as set on the "A MIN" switch (not shown) is timed out by the controller's interval counter (not shown), all as explained in said U.S. patent application S.N. 453,072. The "A MIN" switch determines the minimum major phase green time. At the end of the minimum green period timing, the mode memory cell FREE flip-flop **8** is set.

The controller contains an oscillator (not shown) which generates four clock time pulses, i.e., *w*, *x*, *y* and *z* clock times, each separated by 50 microseconds which are utilized in the present invention. The controller also has the interval counter mentioned above cooperative with a sequencing unit (not shown) but fully explained in said U.S. patent application S.N. 453,072 which provides sequential interval signals designated by Roman numerals such as I to X. At interval X, which represents the major phase green, and the next *z* clock time, an AND gate **6** is enabled by being responsive to the X and *z* signals and to the binary ONE output of the F.S. flip-flop **5**. The output of the AND gate **6** generates a clear free signal. This signal clears the interval counter to its initial or ZERO value and sets the mode memory cell FREE flip-flop **8**.

At the next *x* clock time, an AND gate **7** which is responsive to the interval X signal, the *x* signal and the binary ONE output of the F.S. flip-flop **5** is enabled. The output of the AND gate **7** sets a K flip-flop **10** and generates a load signal which loads the switch setting into the controller's interval counter. This load signal performs the same function as the insert data signal of said U.S. patent application S.N. 453,072. The time that the K flip-flop **10** remains set is equal to the interval counter counting period.

At the next *y* clock time, an AND gate **11** which is responsive to the binary ONE output of the K flip-flop **10**, the binary ONE output of the FREE flip-flop **8** and to the *y* signal is enabled. The AND gate **11** output resets the F.S. flip-flop **5** through an OR gate **12**.

When the "A MIN" period has been timed out by the interval counter, a C3 pulse is generated which resets the K flip-flop **10**. The controller now operates in the free operation.

A traffic call will immediately start the controller in its local cycle. If a call is received by the controller, the $P'+V'$ line will be enabled to provide a signal accordingly. The $P'+V'$ signal enables an AND gate **15** which is also responsive to the binary ZERO signals from the F.S. and K flip-flops **5** and **10**, respectively, as well as the interval X signal, the *w* signal and the binary ONE signal from the FREE flip-flop **8**. The output of the AND gate **15** generates the free start signal. The free start signal enables OR gate **22**, whose other input is the output of the AND gate **105** of said U.S. patent application Ser. No. 453,072. The AND gate **105** is responsive to a binary zero signal from the FREE flip-flop **8**, the IX interval signal, and the A signal. The functions performed by the output of the AND gate **105**, as discussed in said U.S. patent application Ser. No. 453,072, are now performed by the output of the OR gate #**22**; namely, starting the controller sequencing through its local cycle. Then at this time, the circuit has placed the controller in the free mode.

An AND gate **16** is utilized while operating in the free mode. The AND gate **16** is responsive to the C3, interval VIII and the binary ONE output of the FREE flip-flop **8**. When the AND gate **16** is enabled, the F.S. flip-flop **5** is set through the OR gate **4**. The operation as described above with respect to the *z* clock pulse is repeated to satisfy the operating requirements while in this mode.

The transition of the controller from the free mode will now be described. First, the offset command is changed on the input lines to the AND gate **2**. With the controller sequencing through its local cycle, the change in offset command will be stored in the transitional memory cell F.S. flip-flop **5** at the next background start.

However, if the "A MIN" period is timed out before the next background start, the controller will switch out of the mode at that time thus removing the need for storage in the transitional memory cell **5**. The AND gate **2** is disabled by the change in the offset command. With the controller timing the "A MIN" period, the interval X line is enabled. At the end of the period, a C3 signal is generated which enables an AND gate **17** that is responsive to the interval X signal, the C3 signal and the inverted output of the AND gate **2** via an inverting circuit **18**. The output of the AND gate **17** is connected through an OR gate **20** to reset the FREE flip-flop **8**. Thus, the controller is switched back to the coordinated mode.

When the next background start occurs before the previous step (not timing "A MIN" period), an AND gate **21** is enabled which sets the F.S. flip-flop **5** through the OR gate **4**. Then the same sequence for the F.S. flip-flop **5**, as described before, will be repeated except now at the C3 signal, the AND gate **17** will be enabled. This will switch the controller to the coordinated mode.

An advantage of the present invention lies in the fact that it incorporates both the functions required during the free mode and the conditions required during the transition between modes thereby minimizing the structure required to perform these functions.

We claim:

1. In a semi-actuated master controlled traffic intersection controller adapted to operate selectively in coordinated and non-coordinated modes,

means responsive to command signals from a master controller commanding operation in said non-coordinated mode,

timing means for timing an interval including inhibiting means effective to inhibit initation of a non-coordinated cycle until said interval is timed,

initializing means for actuating said timing means at the first occurring coincidence of said non-coordinated mode command signal and a signal indicating that the intersection controller is green in the major traffic phase,

control means for actuating said timing means once for each non-coordinated cycle initiated, and

means for inhibiting the termination of said non-coordinated mode when said timing means are activated.

2. In a controller of the character recited in claim **1** and further including

means for inserting said interval when transferring from non-coordinated to coordinated operation.

3. In a controller of the character recited in claim **1** wherein said means for inhibiting the termination of said non-coordinated mode when said timing means are activated includes

a non-coordinated mode memory flip-flop.

4. In a controller of the character recited in claim **1** in which said interval is the minimum right-of-way interval for the major traffic phase.

5. In a controller of the character recited in claim **1** in which the non-coordinated command signal is the coincidence between the actuated position of the free switch and the light traffic offset command from the master controller.

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