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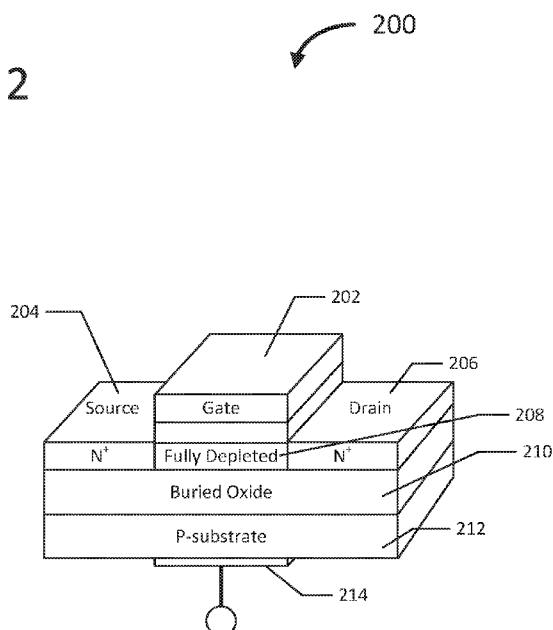
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(54) Title: POWER GATING CIRCUIT UTILIZING DOUBLE-GATE FULLY DEPLETED SILICON-ON-INSULATOR TRANSISTOR

FIG. 2



(57) Abstract: Combining the functionality of sleep transistors with logic devices in power-gating circuits by utilizing fully depleted silicon-on-insulator (FDSOI) transistors. In an embodiment, a back gate of a FDSOI transistor controls the threshold voltage to eliminate the need for standalone sleep transistors.

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POWER GATING CIRCUIT UTILIZING DOUBLE-GATE FULLY DEPLETED SILICON-ON-INSULATOR TRANSISTOR

FIELD

[0001] Aspects of the present invention generally relate to the field of power gating circuits, such as those utilized to manage power consumption and thermal stress in microprocessors and/or integrated circuits.

BACKGROUND

[0002] Power gating is a technique to manage leakage power during the standby mode in low-power and high-speed integrated circuits (ICs). Conventional power gating techniques utilize transistor-based switches (e.g., sleep transistors) to shut down part of the circuit block and put it in idle mode. Sleep transistors help ICs manage power and thermal effects efficiently. The total power consumption of the ICs is comprised of static, dynamic, and short-circuit effects. The dynamic behavior has an exponential effect on the power dissipation, and as a result, it leads to a higher temperature injection in the circuit node. In the static mode, temperature has an exponential effect on the leakage current. This interdependence of power and thermal impacts makes an efficient power gating circuit a very critical requirement for integrated circuits and systems.

[0003] Conventional sleep transistor based power gating techniques utilize one of the three approaches as shown in FIGS. 1A-1C. The first approach, illustrated by FIG. 1A, employs high threshold voltage (high- V_t) transistors between the supply lines and the circuit to create virtual V_{dd} and V_{ss} nodes at every cell that needs to be shut down or placed in a sleep mode. The high- V_t sleep transistors are implemented in the form of a “header switch” and a “footer switch” to isolate the virtual supply nodes from the actual supply lines, as shown in FIG. 1A. The second approach, illustrated by FIG. 1B, utilizes only a “header switch” by connecting a high- V_t transistor between the actual power rail and the virtual V_{dd} node. And the third approach, illustrated by FIG. 1C, utilizes only a “footer” switch.

[0004] All of the above approaches are used to lower subthreshold current leakage. Other conventional techniques include a reconfigurable sleep transistor technique, a negative bias temperature instability (NBTI) aware sleep transistor design, and a sleep transistor

inserted as part of a 3T DRAM cell to reduce leakage power. In all of these conventional approaches, low- V_t transistors are used inside the logic circuits to ensure higher performance during the active mode of the circuit. High- V_t sleep transistors are placed between the logic circuits and the supplies to reduce leakage power during the standby period. These sleep transistors used as “header” and/or “footer” switches impose extra area, delay, and power overheads. Additionally, the design complexity involved with the implementation of transistors with different threshold voltages in the same circuit makes these design techniques less appealing. Moreover, the additional wiring required for the virtual nodes introduces unwanted resistor, inductor, capacitor (RLC) issues and IR-drops causing voltage variations.

SUMMARY

[0005] Aspects of the invention relate to power-gating circuits that combine the functionality of sleep transistors with logic devices by utilizing fully depleted silicon-on-transistor (FDSOI) devices. Beneficially, the FDSOI transistor-based power-gating circuit described herein eliminates the requirement of employing a separate set of sleep transistors to place the circuit in the sleep/idle mode. Eliminating the standalone sleep transistors reduces the overall complexity and overheads of integrated circuits and simplifies power gating techniques. Moreover, aspects of the present disclosure improve the overall power efficiency and reduce thermal effects. In the circuit design described herein, the flexibility to control the threshold voltage (V_t) of a double-gate FDSOI device via the back gate is utilized to eliminate the need for using a separate set of sleep transistors.

[0006] A system embodying aspects of the invention includes a back gate controller and a fully depleted silicon-on-insulator (FDSOI) transistor. The double-gate FDSOI transistor includes a front gate and a back gate. The back gate controller is configured to induce a bias in the back gate of the FDSOI transistor to dynamically set a threshold voltage value of the FDSOI transistor. In a sleep state, the FDSOI transistor is set to a high threshold voltage value and in an active state, the FDSOI transistor is set to a low threshold voltage value.

[0007] Other objects and features will be in part apparent and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A-1C illustrate conventional sleep transistor circuits.

[0009] FIG. 2 illustrates an exemplary double-gate silicon-on-insulator (SOI) metal-oxide semiconductor field-effect transistor (MOSFET) according to an embodiment.

[0010] FIG. 3 illustrates an exemplary variation of threshold voltage with back gate bias according to an embodiment.

[0011] FIG. 4 illustrates an exemplary propagation delay incurred by a header switch transistor in a two-input NAND gate SOI FET design at a high threshold voltage according to an embodiment.

[0012] FIG. 5 illustrates an exemplary propagation delay incurred by a header switch transistor in a two-input NAND gate SOI FET design at a low threshold voltage according to an embodiment.

[0013] FIG. 6 illustrates an exemplary two-input NAND gate in which the same set of transistors perform both sleep and logic functions according to an embodiment.

[0014] FIG. 7 illustrates an exemplary variation of leakage current with back gate voltage according to an embodiment.

[0015] FIG. 8 illustrates an exemplary relation between leakage current and threshold voltage according to an embodiment.

[0016] FIG. 9 illustrates an exemplary relation between threshold voltage and standby power according to an embodiment.

[0017] FIG. 10 illustrates an exemplary relation between back gate voltage and standby power according to an embodiment.

[0018] FIG. 11A illustrates an exemplary threshold voltage relative to back gate bias according to an embodiment.

[0019] FIG. 11B illustrates exemplary drain currents with respect to drain voltage and back gate bias according to an embodiment.

[0020] FIG. 11C illustrates an exemplary leakage current relative to back gate voltage according to an embodiment.

[0021] FIG. 11D illustrates an exemplary leakage current relative to threshold voltage according to an embodiment.

[0022] FIG. 11E illustrates an exemplary threshold voltage relative to static power according to an embodiment.

[0023] FIG. 11F illustrates an exemplary back gate voltage relative to static power according to an embodiment.

[0024] Corresponding reference characters indicate corresponding parts throughout the drawings.

DETAILED DESCRIPTION

[0025] In conventional complementary metal-oxide semiconductor (CMOS) sleep transistor design, logic gates or blocks are connected to the power supplies through sleep transistors. These sleep transistors are controlled by signals generated by a central gate controller or distributed control logics. But centralized sleep transistor designs suffer from large interconnect resistances between distant blocks. Such resistance has to be compensated by an extra-large sleep transistor area. In the distributed and cluster-based designs of sleep transistors (as opposed to the centralized control approach), additional wiring is required. In accordance with an aspect of the present disclosure, the additional sleep transistors are completely eliminated, which provides 100% savings of the area overheads of the sleep transistors.

[0026] The additional wiring and the placement of additional sleep transistors (FIGS. 1A-1C) between the functional blocks and the power supplies result in a delay penalty in the conventional designs. In the absence of a sleep transistor, the propagation delay (τ_{pd}) of a logic gate depends on the supply and threshold voltages. This dependency can be expressed by the Alpha Power law model as depicted in Equation (1), where C_L is the load capacitance and α is the velocity saturation index, which is process specific. For simplicity, α is typically assumed to be 1 in short-channel devices.

$$T_{pd} = \frac{C_L V_{dd}}{(V_{dd} - V_{tL})^\alpha} \quad (1)$$

[0027] When a sleep transistor is present, a source drain voltage (V_{sd}) drop occurs causing the propagation delay to increase as shown in Equation (2).

$$T_{pd-MT} = \frac{C_L V_{dd}}{(V_{dd} - V_{sd} - V_{tL})^\alpha} \quad (2)$$

[0028] The performance loss (PL) due to the increase in propagation delay related to the sleep transistors is depicted by Equation (3).

$$PL = 1 - \frac{5 T_{pd}}{T_{pd-MT}} \quad (3)$$

[0029] The delay overhead depicted by Equation (3) is absent in power gating circuits in accordance with an aspect of the disclosure because of the elimination of sleep transistors.

[0030] FIG. 2 illustrates a double-gate fully depleted silicon-on-insulator (FDSOI) transistor 200 adapted to perform both the functions of sleep transistors and logic devices, in accordance with an aspect of the disclosure. The FDSOI transistor 200 includes a front gate 202, a source 204, a drain 206, a body (i.e., fully depleted layer) 208, a buried oxide layer 210, a substrate layer 212, and a back gate 214. As illustrated, the back gate 214 is provided under the substrate layer 212. In an embodiment, FDSOI transistor 200 comprises a metal-oxide semiconductor field-effect transistor (MOSFET).

[0031] The FDSOI transistor 200 includes two gates (e.g., front gate 202 and back gate 214) that control the charges in the silicon channels. In an aspect, FDSOI transistor 200 differs from conventional approaches by the addition of a conductive under layer (e.g., back gate 214) beneath the SOI device. As depicted in FIG. 2, the body region of this SOI MOSFET is floating as opposed to a bulk MOSFET device, in which the body is inherently connected to the substrate. From a functional point of view, the FDSOI transistor 200 can be viewed as two MOSFETs (e.g., front and back MOSFETs) that share the same body, drain, and source regions. Although embodiments described herein utilize a fully depleted (FD) channel region (e.g., body) SOI MOSFET structure, one of ordinary skill in the art will understand that a partially depleted (PD) channel region is within the scope of the present disclosure. An exemplary advantage of FDSOI transistor 200 includes enhanced control of the back-gate on the channel. In an aspect of the PDSOI, the back gate or the substrate has very minor influence on the front surface and channel potential. In an aspect of FDSOI devices, the silicon film thickness is generally less than or equal to about half of the depletion width of the bulk device. Electrical parameters, including threshold voltage and drain current of the SOI devices, are influenced by the film thickness.

[0032] Since fully depleted SOI MOSFET threshold voltages are sensitive to the variations in SOI silicon film thickness, thin films are required in order to have enhanced control over the performance of a device. In addition, thinner SOI film thickness is required for the minimization of short-channel effects and elimination of the current kinks in the SOI MOSFETs.

The surface potentials of FDSOI at the front and back interfaces are strongly coupled to each other and capacitively coupled to the front-gate and the substrate through the front-gate oxide and buried oxide, respectively.

[0033] The threshold voltage of a double-gate FDSOI can be modeled as in Equation (4) and Equation (5), where V_t^f and V_{BG} are the front threshold and back gate voltages, respectively, V_{FB}^f and V_{FB}^b are the front gate and back gate flatband voltages, respectively, C_{ox} , C_{BOX} , and C_{si} are front and back gate oxide, and the buried oxide capacitance and depleted silicon film capacitances. Q_b is the area charge density in the depleted silicon film.

$$V_t^f = V_{FB}^f + 2\phi_B - \frac{Q_b}{2C_{ox}} - \left(V_{BG} - V_{FB}^b - 2\phi_B + \frac{Q_b}{2C_{BOX}} \right) \cdot \frac{C_{si}C_{BOX}}{C_{ox}(C_{si}+C_{BOX})} \quad (4)$$

$$Q_b = -qN_A T_{si} \text{ or } +qN_D T_{si} \quad (5)$$

[0034] FIG. 3 shows the dependence of the threshold voltage on the back gate of the device for both n-type silicon on insulator (NSOI) (302) and p-type silicon on insulator (PSOI) (304) devices. In an embodiment, FDSOI transistor 200 controls subthreshold leakage by lowering the subthreshold swing (S) of the transistor. The FDSOI provides a lower value of S (e.g., between 65-80 mV/dec) and it can even be further improved by reducing η (DIBL or drain induced barrier) using the thin film (T_{si}) design. The achievable values of S in the conventional bulk MOSFET are between 90-120 mV/dec. The subthreshold swing S of FDSOI device is given by Equation (6), where $C_{it1,2}$ is interface-trap capacitance in the wafer process, which can dynamically be charged or discharged. In this device, the threshold voltage values can be controlled by applying a bias voltage at the back gate.

$$S_1^{dep} = 2.3 \frac{KT}{q} \left(1 + \frac{C_{it1}}{C_{ox1}} + \frac{C_{ox2}+C_{it2}}{C_{si}+C_{ox2}+C_{it2}} + \frac{C_{si}}{C_{ox1}} \right) \quad (6)$$

[0035] FIG. 4 illustrates a propagation delay incurred by a header switch (e.g., transistor) in a two-input NAND gate SOI FET design at high- V_t in accordance with an embodiment of the disclosure. As illustrated, FIG. 4 depicts the output voltage (V) of a two-input NAND gate with header switch (402) with a solid line and without a header switch or back gate controlled design (404) with a dashed line. At a high threshold voltage setting, the proposed approach shows a 177.6 picosecond propagation delay improvement.

[0036] FIG. 5 illustrates a propagation delay incurred by a header switch (e.g., transistor) in a two-input NAND gate SOI FET design at low- V_t in accordance with an embodiment of the disclosure. As illustrated, the output voltage of a circuit in accordance with the present disclosure (502) shown with a solid line can push the threshold voltage to a low setting and allow it to turn on quicker than one with a header switch (504) shown with a dashed line. An improvement of about 500 picoseconds is exhibited via dynamic threshold control. Additionally, the slope of the new circuit is much steeper, this is especially important for the transient response of the circuit in active mode. Details regarding dynamic control of the threshold voltage via the back gate are further described herein.

[0037] For faster operation in the active mode, a lower threshold voltage for the logic transistors is desired to provide a higher gate drive. For power savings in the standby mode, a higher threshold voltage in the sleep transistors is desired because higher threshold voltage leads to exponential reduction of the subthreshold current, which is the primary source of standby power. Since the same set of transistors perform both the functions (of logic and sleep transistors) in accordance with an aspect of the disclosure, the ability to dynamically set lower and higher values of threshold voltage in the same transistors is required. This can be done in a double-gate SOI device. The flexibility of the double-gate SOI devices provides the ability to dynamically set the threshold voltage to an appropriate level for both active (e.g., a first value or level) and standby (e.g., a second value or level) modes. In an embodiment, the threshold voltage of the double-gate SOI device is set to a first value that corresponds to an active mode. The double-gate SOI operates at the first threshold voltage value while in the active mode. The threshold voltage of the double-gate SOI can be dynamically adjusted to a second value that corresponds to a sleep mode. The double-gate SOI then operates at the second threshold voltage value during the sleep mode. In one form, the threshold voltage is initially at a value (e.g., a third value) that is higher than the first value. In this form, the setting of the threshold voltage comprises reducing the threshold from the third value to the first value in order to achieve faster operation of the double-gate SOI device while in the active mode. In another form, the dynamic adjustment of the threshold voltage comprises dynamically increasing the threshold voltage from the first value to the second value to achieve power savings of the double-gate SOI device in the sleep mode. Moreover, utilizing a SOI device beneficially results in enhanced performance (e.g., high speed, low power consumption,

radiation-hardness, etc.), higher scalability, improved noise immunity, lower parasitic capacitances, and higher yield.

[0038] FIG. 6 illustrates an exemplary two-input NAND gate 600 in accordance with an aspect of the disclosure, in which the same set of transistors are utilized for sleep and logic functions by replacing conventional bulk MOSFET transistors by a double-gate FDSOI transistor. The front gates of all of the transistors of FIG. 6 are connected to appropriate voltage supplies, while the back gates are connected to a centralized back gate controller (BCR). In another embodiment, the double-gate FDSOI is managed by distributed control logic components in the same manner conventional sleep transistors are connected and controlled. Advantageously, the illustrated two-input NAND gate in accordance with an aspect of the disclosure does not need the additional sleep transistor because the back-gate MOSFET within the double-gate FDSOI device structure will perform this function. Different levels of I_{on} current can be specified based on the effective bias at the back gates of the transistors. In the active mode, higher I_{on} current can be set for faster operation. In the standby mode, the transistors can be set to low-current and low-power mode dynamically. In an embodiment, the high and low current values are relative to the application. For example, a microampere current may be a low (e.g., off) current in some applications and a very high current in other applications (e.g., low-power applications, etc.). In another embodiment, the high and low current values are relative to the size of the device and technology node (e.g., see FIGS. 7 and 8).

[0039] The subthreshold leakage current in a MOSFET device can be modeled as in Equations (7)-(9). These equations are slightly modified to represent the back gate bias voltage.

$$I_{leakage} = I_0 e^{\frac{V_{GS} - V_{TH} - \eta V_{DS} + \gamma V_{BS}}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}} \right) \quad (7)$$

$$I_{leakage} = I_0 e^{\frac{V_{GS} - V_{TH} - \eta V_{DS} + \gamma V_{BS}}{s}} \left(1 - e^{\frac{-V_{DS}}{V_T}} \right) \quad (8)$$

$$I_0 = \mu C_{ox} \frac{W}{L} V_T^2 e^{1.8} \text{ and } V_T = \frac{KT}{q} \quad (9)$$

[0040] Here V_{GS} , V_{DS} , and V_{BS} are the gate to source, drain to source, and bulk to source voltages, respectively, and μ denotes the carrier mobility. C_{ox} is the gate oxide capacitance, W and L denote the channel width and length of the SOI MOSFET, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, V_T

is the thermal voltage, V_{THf} is the threshold voltage at the front gate (as a function of the bias voltage), γ is the body effect coefficient, η denotes the drain induced barrier lowering coefficient, n is the subthreshold swing coefficient, and S is the subthreshold swing (as in Equation 6).

[0041] For the two-input NAND sleep transistor circuit 600 in accordance with an aspect of the disclosure, various Hspice simulations were performed and the results are presented in FIGS. 7-10. FIG. 7 shows the variation of the leakage current with the back gate voltage. The correlation between the threshold voltage and leakage current is shown in FIG. 8. As depicted by FIGS. 7 and 8, by setting a proper value of the threshold voltage through the back-gate, an acceptable level of leakage current can be set for the standby mode. The subthreshold leakage current is the dominant source of static or standby power dissipation. FIGS. 9 and 10 show the change in standby power with the change of the threshold voltage and back gate bias, respectively. Therefore, by properly adjusting the back gate bias it is possible to control the standby power dissipation in the circuit 600 depicted in FIG. 6 for a two-input NAND gate.

[0042] Before implementing the design on Hspice, the sleep transistor design in accordance with an aspect of the present disclosure was first simulated and verified on MATLAB. The equations provided above from (4) to (9) are used to base the foundation for the design approach. The simulation results for the preliminary analysis are presented in FIG. 11. The input voltages as well as some of the device parameters are not the same with the Hspice design. Also, some of the equations were simplified to facilitate the coding. Plot (a) of FIG. 11, shows threshold dependency of NSOI by varying the back gate voltage. FDSOI can be viewed and modeled as two FETs with two gates that control the charges in the silicon channels (plot (b) of FIG. 11). This allows the designer to accurately modulate the I_{on} current to increase and I_{off} current to decrease dynamically. Plots (c) and (d) of FIG. 11 are very critical, especially to sleep transistor design. The figures show the flexibility of FDSOI to the back bias voltage in determining the leakage current. Plots (e) and (f) of FIG. 11 illustrate the correlation between high and low threshold voltage and their role when it comes to static power dissipation.

[0043] In one form, aspects of the disclosure provide an approach to mitigate static power consumption using double-gate FDSOI transistors. In an embodiment, sleep transistor characteristics are controlled via back-gate bias. This approach simplifies design complexity,

reduces chip area, improves power dissipation, and lowers thermal effects in the circuit.

Beneficially, transistors in accordance with the present disclosure reduce performance loss due to propagation delay caused by additional transistors between the low- V_t logic blocks and voltage supply line. The approach described herein incorporates the sleep transistor design as part of the circuit design and avoids the standalone complex design technique. Moreover, aspects of the present disclosure provide a dynamically controlled V_t for circuits that need to be switched between a sleep state and an active state.

[0044] A system embodying aspects of the invention includes a back gate controller and a fully depleted silicon-on-insulator (FDSOI) transistor (200). The double-gate FDSOI transistor includes a front gate (202) and a back gate (214). The back gate controller is configured to induce a bias in the back gate of the FDSOI transistor to dynamically set a threshold voltage value of the FDSOI transistor. In a sleep state, the FDSOI transistor is set to a high threshold voltage value and in an active state, the FDSOI transistor is set to a low threshold voltage value.

[0045] In one form, the back gate is arranged beneath the FDSOI transistor. In another form, the system further includes a source (204), a drain (206), a fully depleted layer (208), a buried oxide layer (210), and a substrate layer (212). In yet another form, the fully depleted layer is arranged between the buried oxide layer and the front gate, the buried oxide layer is arranged between the fully depleted layer and the substrate layer, and the substrate layer is arranged between the buried oxide layer and the back gate. In another form, the substrate layer is a silicon thin film. In yet another form, a body region (e.g., fully depleted layer) is floating. In another form, the back gate controller is configured to set a high I_{on} current for the active state and a low I_{on} current for the sleep state. In yet another form, the FDSOI transistor is a metal-oxide semiconductor field-effect transistor (MOSFET) that is configured to perform logic operations on input voltages when the FDSOI MOSFET is in the active state and the back gate is configured to switch the FDSOI MOSFET between the active state and an idle state.

[0046] A method embodying aspects of the invention includes setting a threshold voltage of a logic transistor (200) at a first value that corresponds to an active mode. The logic transistor is operated at the first threshold voltage value during the active mode. The method further includes dynamically adjusting the threshold voltage of the logic transistor to a second

value that corresponds to a sleep mode. The logic transistor is then operated at the second threshold voltage value during the sleep mode.

[0047] In one form, setting the threshold voltage value comprises reducing the threshold voltage from a third value that is higher than the first value. The threshold voltage is reduced from the third value to the first value to achieve faster operation of the logic transistor in the active mode. In another form, the dynamic adjustment of the threshold voltage comprises dynamically increasing the threshold voltage from the first value to the second value to achieve power savings of the logic transistor in the sleep mode. In yet another form, the logic transistor is a double-gate fully depleted silicon-on-insulator (FDSOI) transistor. In another form, the FDSOI transistor is a MOSFET.

[0048] A logic circuit embodying aspects of the invention includes an integrated power gating circuit. The power gating circuit includes a transistor (200) that has a plurality of threshold voltage values. The transistor is configured to perform logic operations on input voltages at a first threshold value when in an active state and configured to switch from the active state to an idle state. The idle state has a second threshold value that is different than the first threshold value.

[0049] In one form, the transistor includes a back gate (214) that is configured to switch the transistor from the active state to the idle state. In another form, the back gate is arranged beneath the transistor. In yet another form, the transistor includes a front gate (202) arranged on top of the transistor such that the front gate and the back gate comprise opposite sides of the transistor. In another form, the transistor is a double-gate fully depleted silicon-on-insulator (FDSOI) transistor. In yet another form, the FDSOI transistor is a MOSFET.

[0050] When introducing elements of aspects of the invention or the embodiments thereof, the articles “a”, “an”, “the” and “said” are intended to mean that there are one or more of the elements. The terms “comprising”, “including”, and “having” are intended to be inclusive and mean that there may be additional elements other than the listed elements.

[0051] Having described aspects of the invention in detail, it will be apparent that modifications and variations are possible without departing from the scope of aspects of the invention as defined in the appended claims. As various changes could be made in the above constructions, products, and methods without departing from the scope of aspects of the

invention, it is intended that all matter contained in the above description and shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

WHAT IS CLAIMED IS:

1. A power-gating circuit, comprising:
 - a back gate controller; and
 - a double gate fully depleted silicon-on-insulator (FDSOI) transistor, the FDSOI transistor having a front gate and a back gate,
 - wherein the back gate controller is configured to induce a bias in the back gate of the FDSOI transistor to dynamically set a threshold voltage value of the FDSOI transistor, wherein the FDSOI transistor is set to a high threshold voltage value in a sleep state thereof, and
 - wherein the FDSOI transistor is set to a low threshold voltage value in an active state thereof.
2. The power-gating circuit of claim 1, wherein the back gate is arranged beneath the FDSOI transistor.
3. The power-gating circuit of claim 1, further comprising:
 - a source;
 - a drain;
 - a fully depleted layer;
 - a buried oxide layer; and
 - a substrate layer.
4. The power-gating circuit of claim 2, wherein the fully depleted layer is arranged between the buried oxide layer and the front gate, wherein the buried oxide layer is arranged between the fully depleted layer and the substrate layer, and wherein the substrate layer is arranged between the buried oxide layer and the back gate.
5. The power-gating circuit of claim 2, wherein the substrate layer comprises a silicon thin film.
6. The power-gating circuit of claim 1, wherein a body region of the FDSOI transistor is floating.

7. The power-gating circuit of claim 1, wherein the back gate controller is configured to set a high I_{on} current for the active state, and wherein the back gate controller is configured to set a low I_{on} current for the sleep state.
8. The power-gating circuit of claim 1, wherein the FDSOI transistor comprises a metal-oxide semiconductor field-effect transistor (MOSFET), the FDSOI MOSFET configured to perform logic operations on input voltages when the FDSOI MOSFET is in the active state and the back gate configured to switch the FDSOI MOSFET between the active state and an idle state.
9. A method comprising:
- setting a threshold voltage of a logic transistor at a first value, the first threshold voltage value corresponding to an active mode;
 - operating the logic transistor at the first threshold voltage value during the active mode;
 - dynamically adjusting the threshold voltage of the logic transistor to a second value, the second threshold voltage value corresponding to a sleep mode; and
 - operating the logic transistor at the second threshold voltage value during the sleep mode.
10. The method of claim 9, wherein said setting the threshold voltage value comprises reducing the threshold voltage from a third value to the first value to achieve faster operation of the logic transistor in the active mode.
11. The method of claim 9, wherein said dynamically adjusting the threshold voltage comprises dynamically increasing the threshold voltage from the first value to the second value to achieve power savings of the logic transistor in the sleep mode.
12. The method of claim 9, wherein the logic transistor comprises a double-gate fully depleted silicon-on-insulator (FDSOI) transistor.

13. The method of claim 12, wherein the FDSOI transistor comprises a FDSOI metal-oxide semiconductor field-effect transistor (MOSFET).

14. A logic circuit comprising an integrated power gating circuit, the power gating circuit comprising a transistor having a plurality of threshold voltage values, the transistor configured to perform logic operations on input voltages at a first threshold value when in an active state and configured to switch from the active state to an idle state having a second threshold value different than the first threshold value.

15. The logic circuit of claim 14, wherein the transistor includes a back gate, and wherein the back gate is configured to switch the transistor from the active state to the idle state.

16. The logic circuit of claim 15, wherein the back gate is arranged beneath the transistor.

17. The logic circuit of claim 16, wherein the transistor includes a front gate arranged on top of the transistor such that the front gate and the back gate comprise opposite sides of the transistor.

18. The logic circuit of claim 15, wherein the transistor is a double-gate fully depleted silicon-on-insulator (FDSOI) transistor.

19. The logic circuit of claim 18, wherein the FDSOI transistor comprises a FDSOI metal-oxide semiconductor field-effect transistor (MOSFET).

PRIOR ART

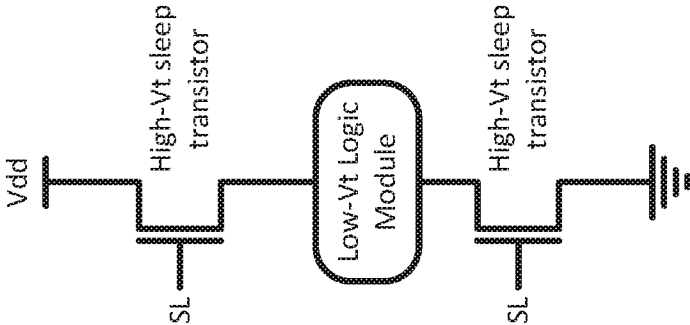


FIG. 1A

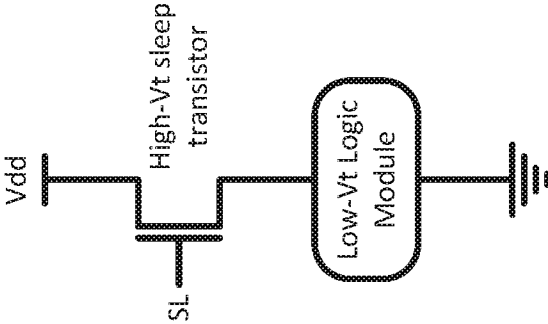


FIG. 1B

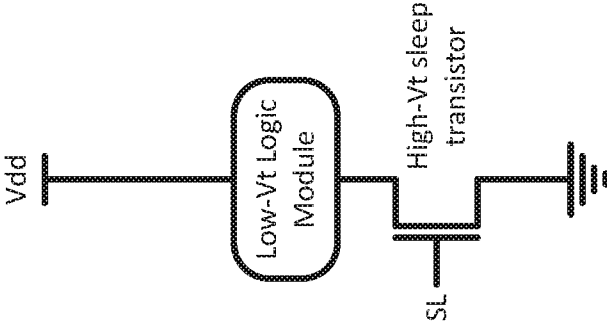


FIG. 1C

FIG. 2

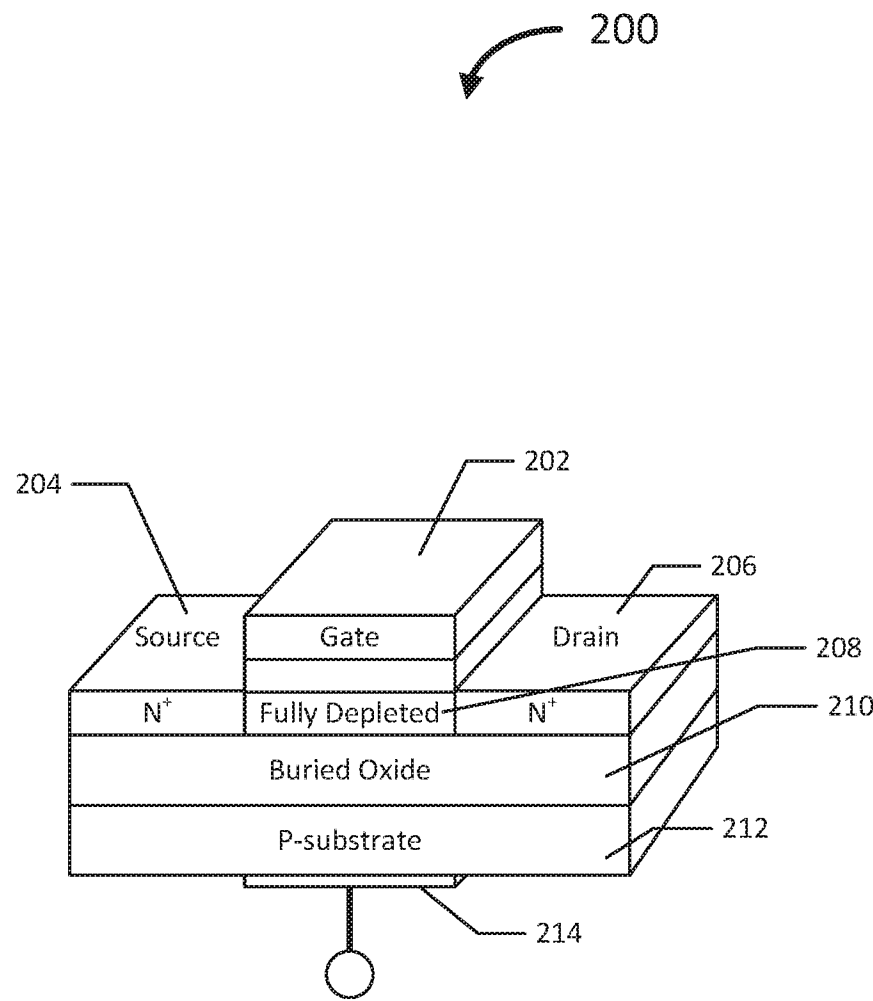


FIG. 3

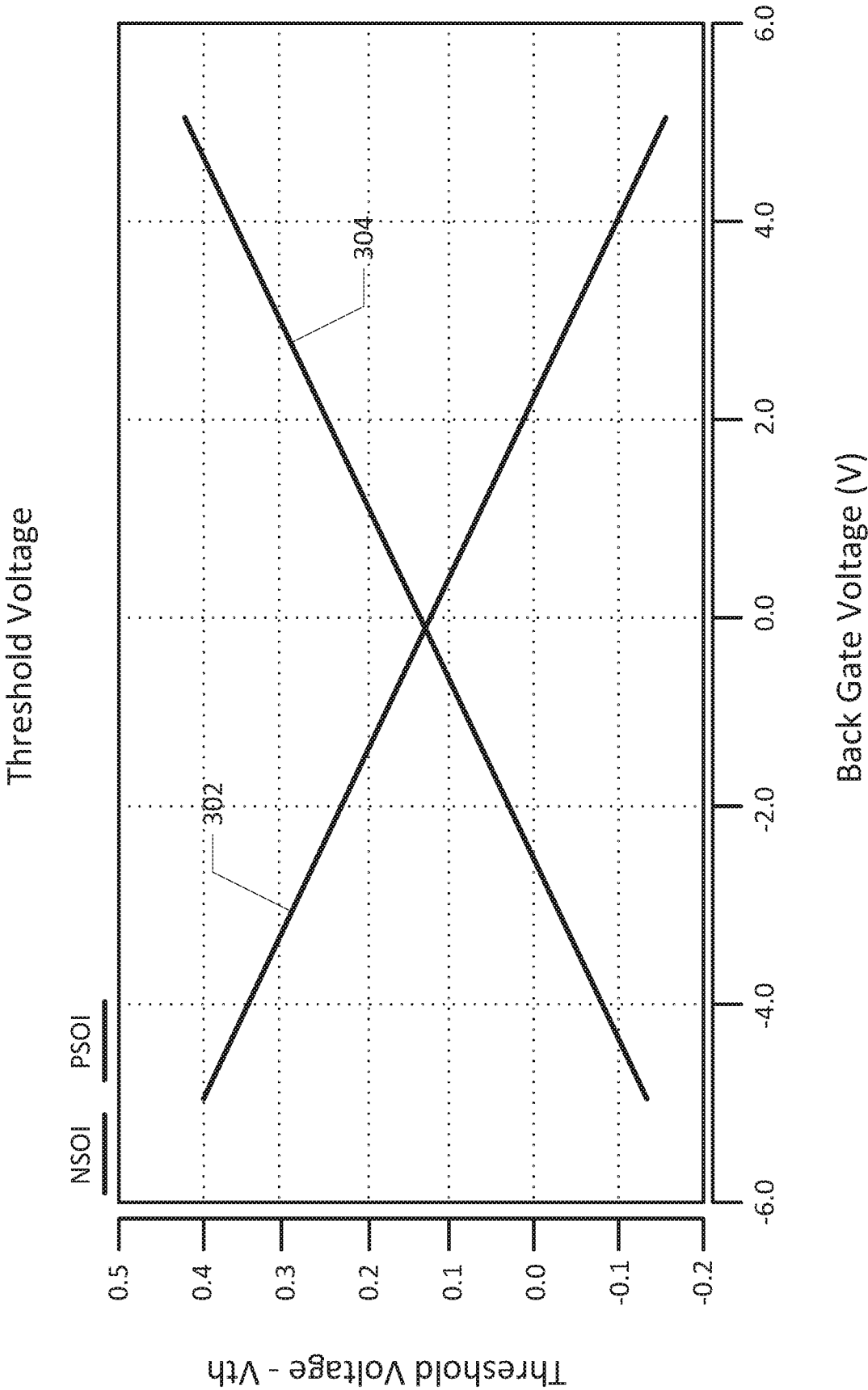


FIG. 4

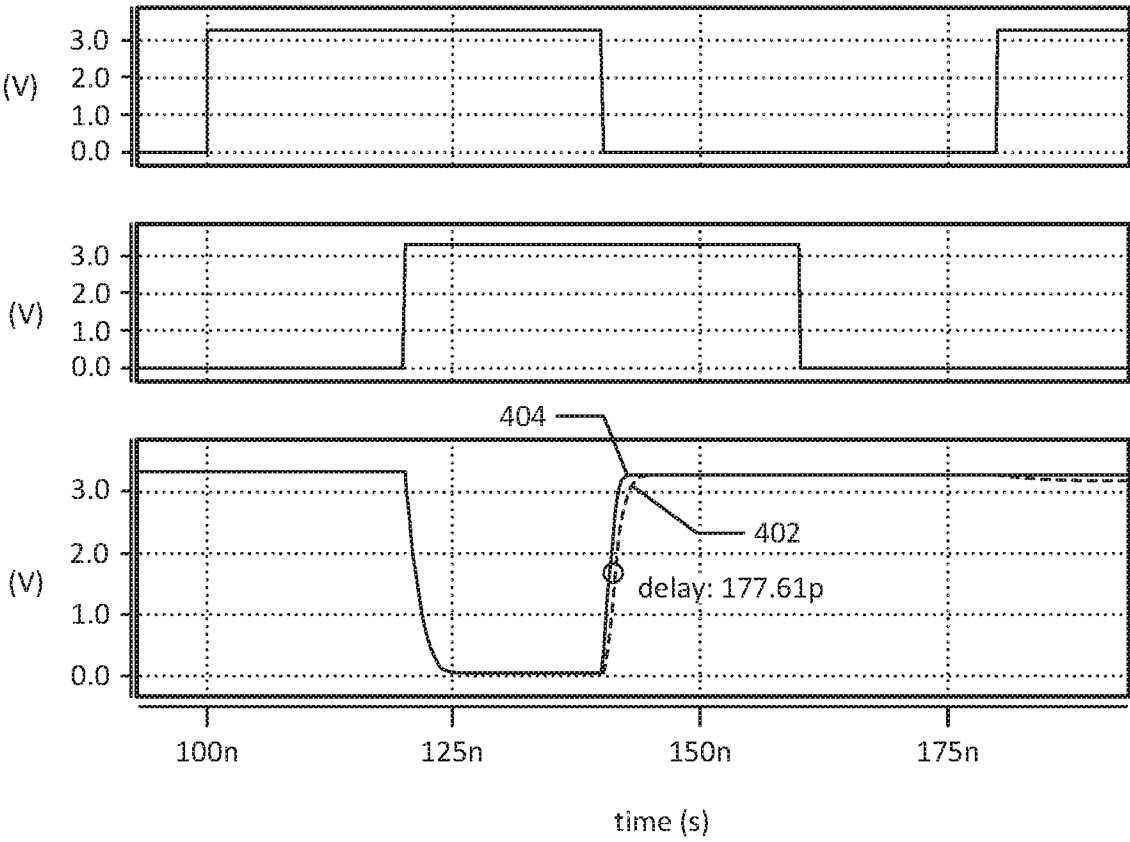


FIG. 5

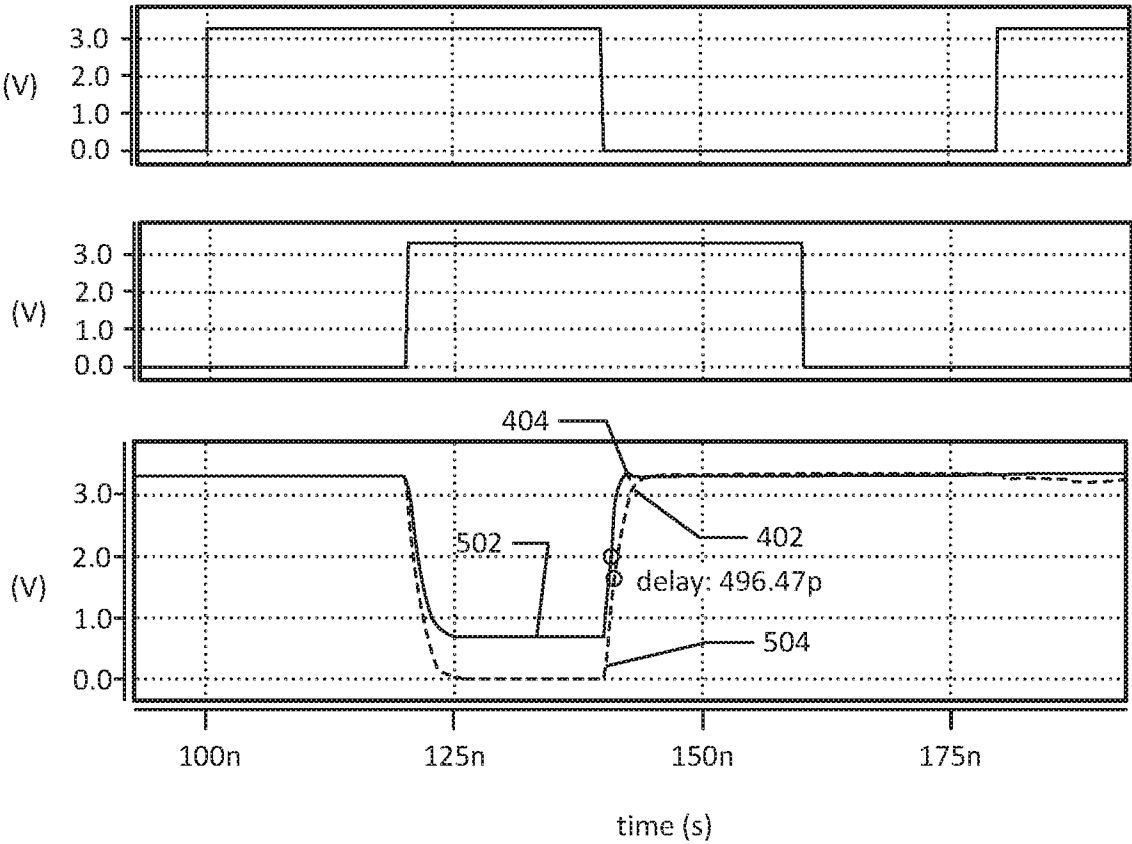


FIG. 6

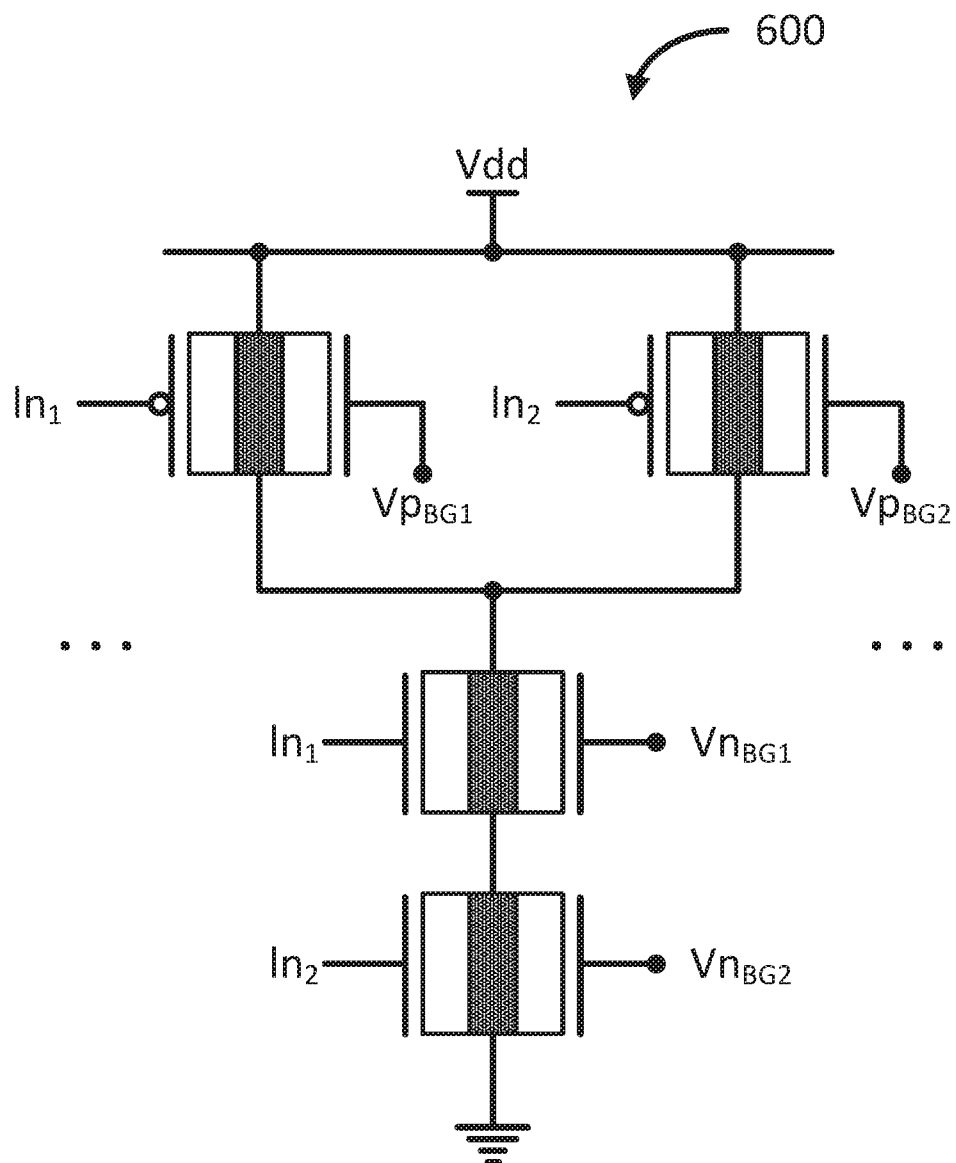


FIG. 7

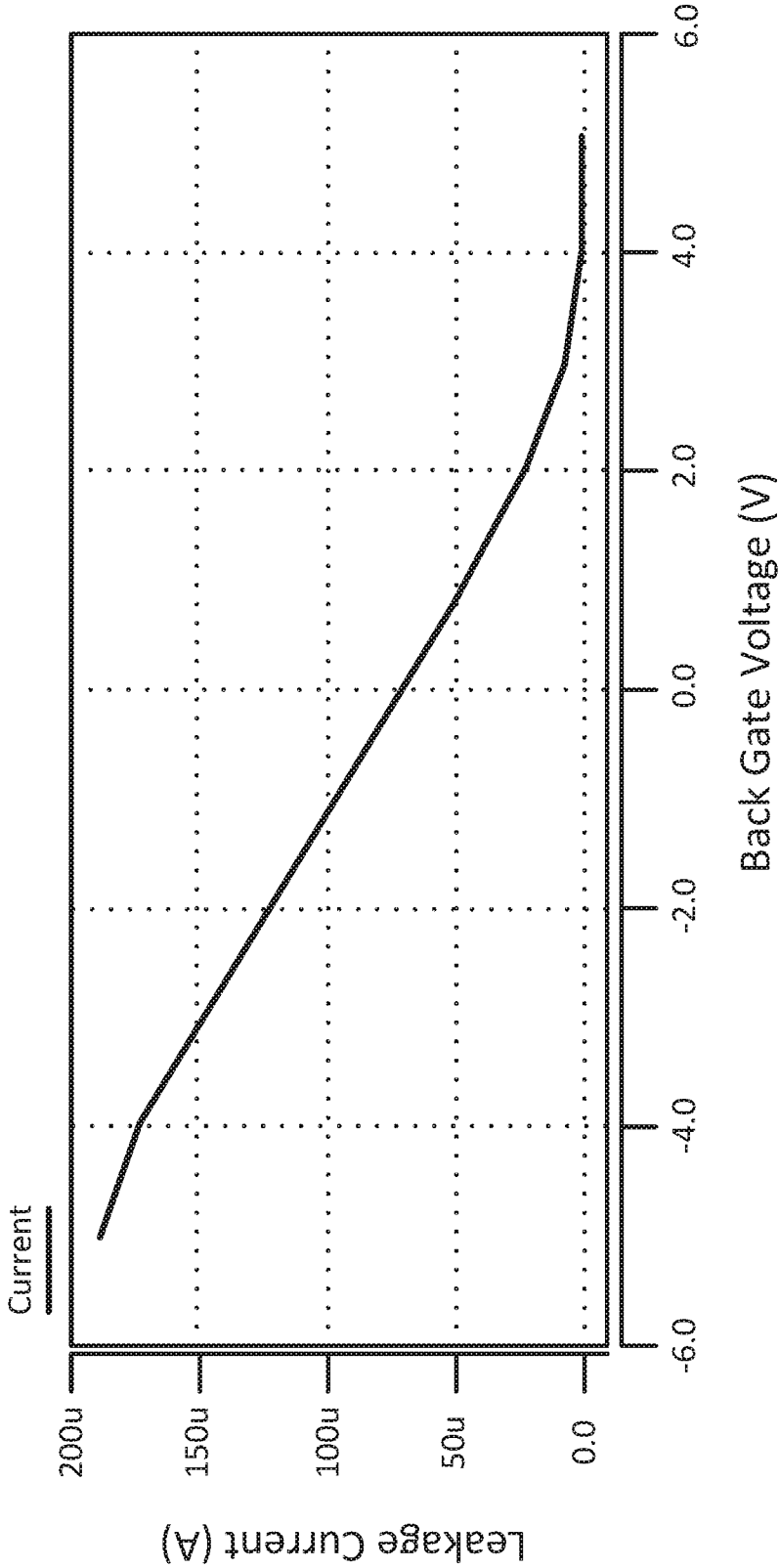


FIG. 8

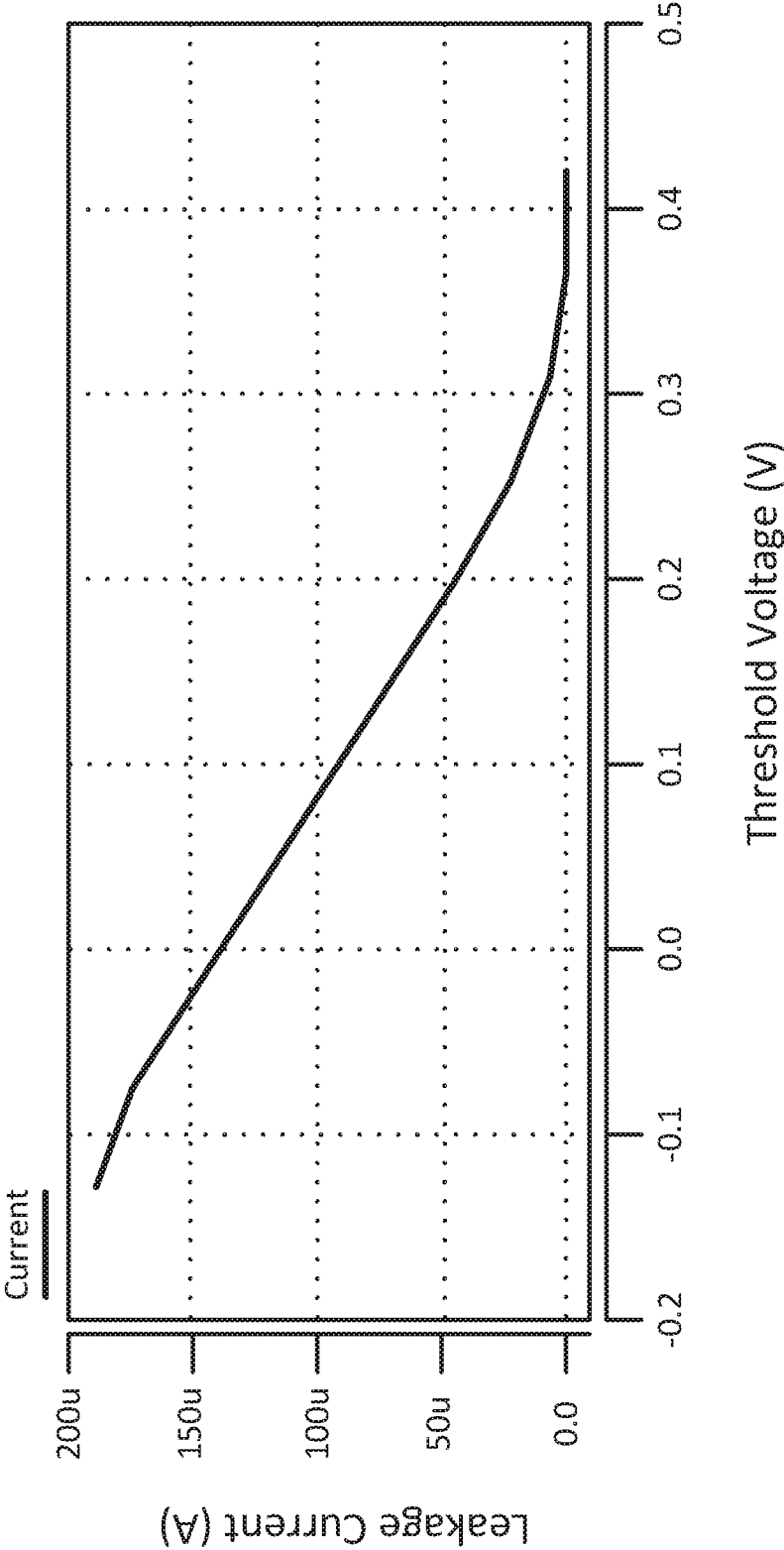


FIG. 9

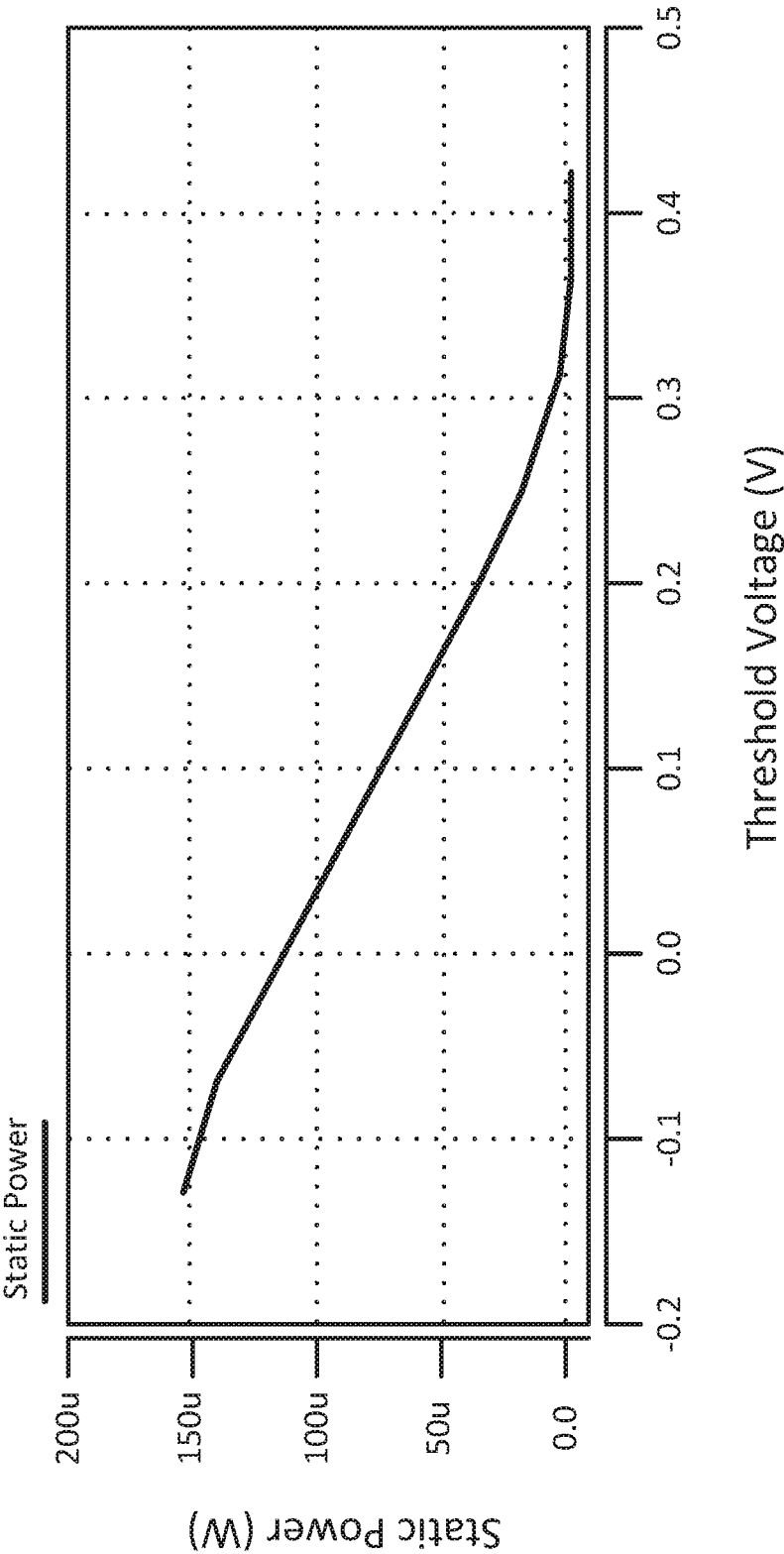
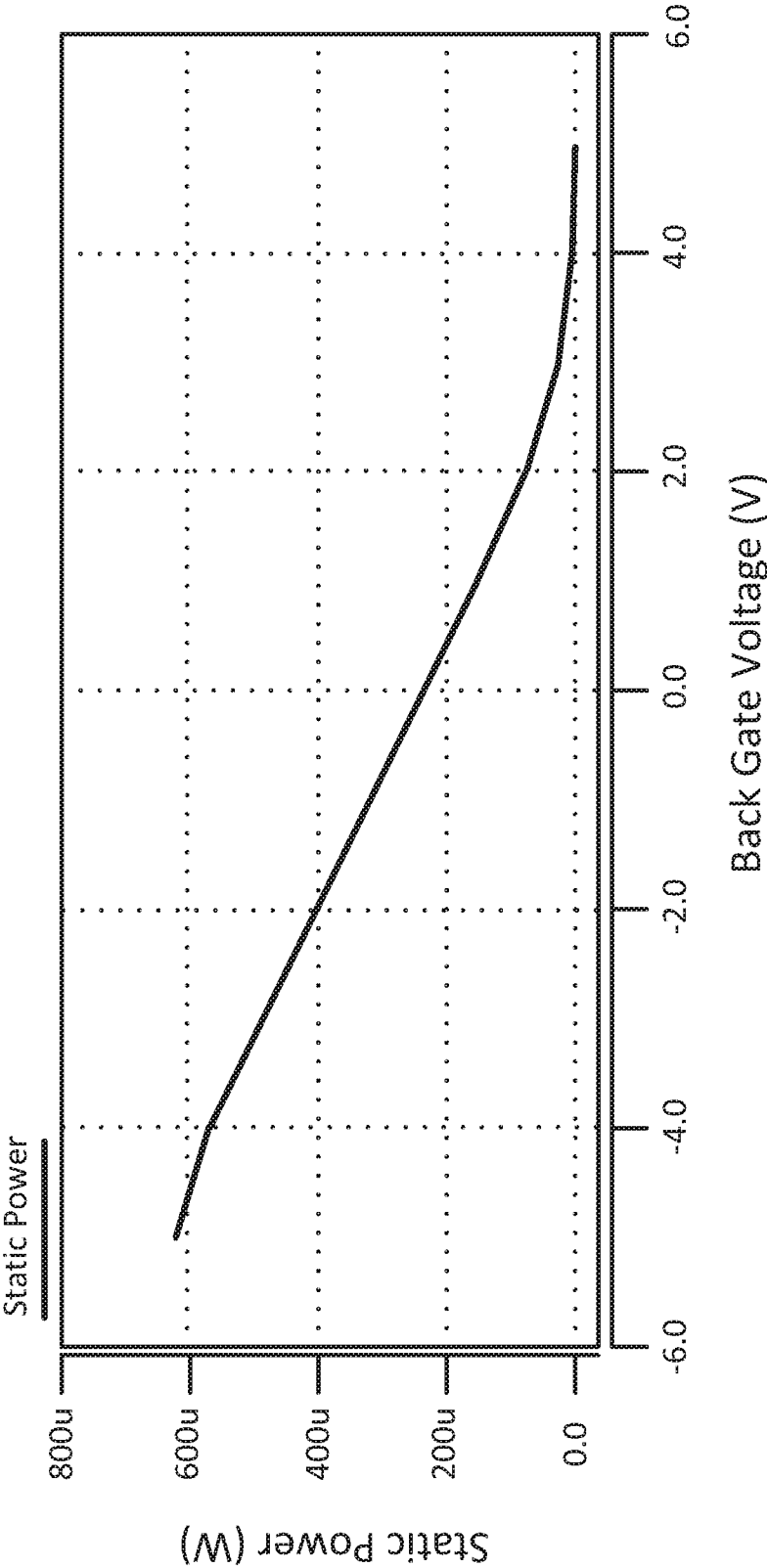


FIG. 10



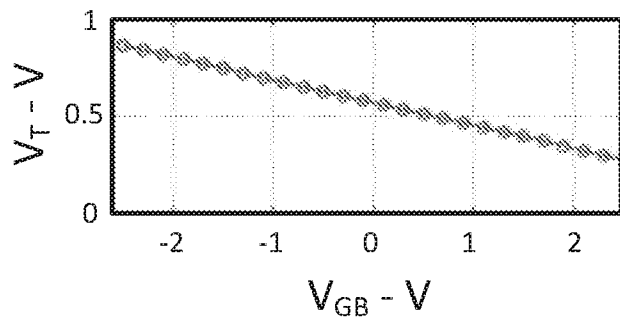


FIG. 11A

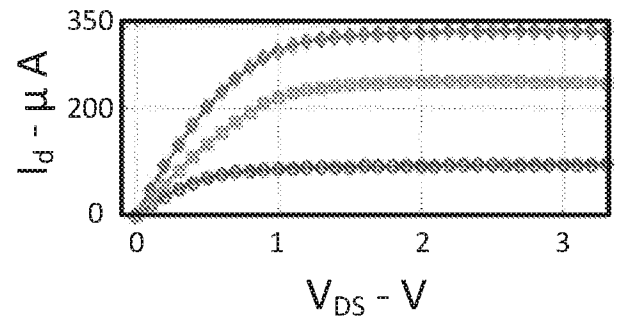


FIG. 11B

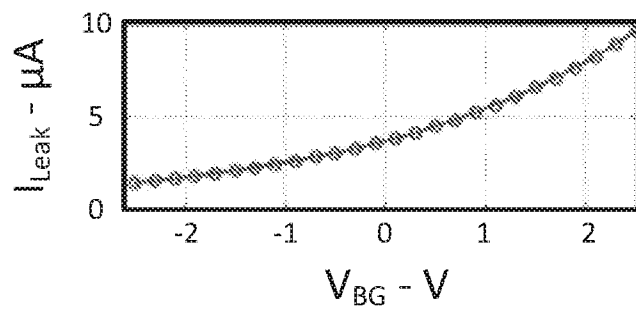


FIG. 11C

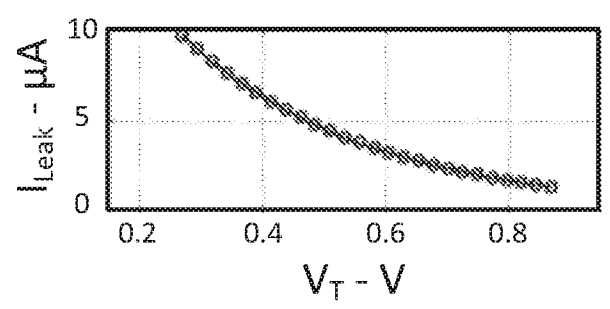


FIG. 11D

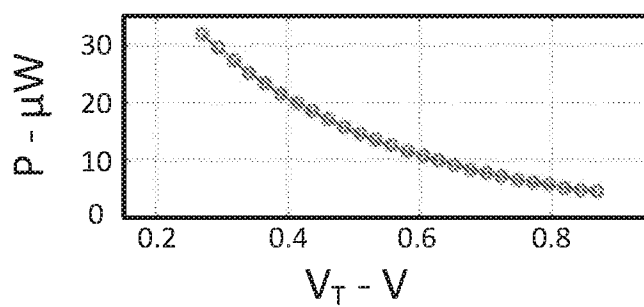


FIG. 11E

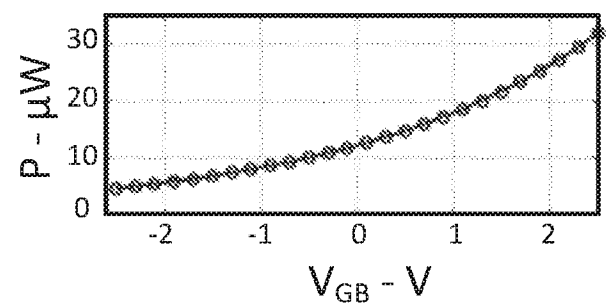


FIG. 11F

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 17/62459

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H03K 3/01, H03K 19/003, H03K 19/00, H01L 27/02 (2018.01)

CPC - H03K 19/018585, H01L 27/0218, H01L 29/66772, H01L 21/84, H03K 19/0027, H03K 19/00384, H01L 27/1203, H01L 29/78648

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y --- A	US 5,821,769 A (DOUSEKI) 13 October 1998 (13.10.1998), abstract; Fig 9A, 9B; col 14-27; col 7, ln 25-30; col 16, ln 10-27; col 16, ln 52-64	1, 3, 6, 8, 9, 11-15, 18, 19 ----- 2, 16, 17 ----- 4, 5, 7, 10
Y --- A	US 2005/0037582 A1 (DENNARD et al.) 17 February 2005 (17.02.2005), para [0002], [0008], [0034], [0045]; Fig 4	2, 16, 17 ----- 4, 5
Y --- A	US 5,164,805 A (LEE) 17 November 1992 (17.11.1992), Fig 1; col 2, ln 44-46; col 4, ln 39-47	17 ----- 4
A	US 2003/0067321 A1 (TURNER) 10 April 2003 (10.04.2003), entire document	1-19
A	US 2016/0079127 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 17 March 2016 (17.03.2016), entire document	1-19
A	US 2011/0133776 A1 (MAZURE et al.) 09 June 2011 (09.06.2011), entire document	1-19
A	US 2008/0239789 A1 (SHINO et al.) 02 October 2008 (02.10.2008), entire document	1-19

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 January 2018

Date of mailing of the international search report

05 MAR 2018

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

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