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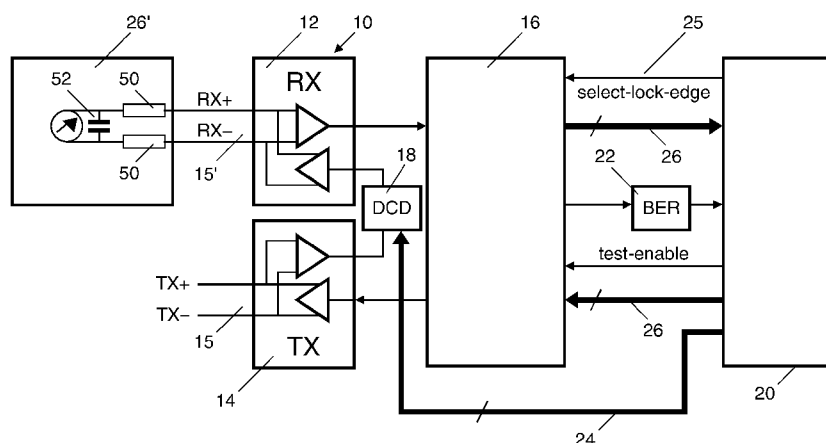


FIG. 1C

(57) Abstract: This invention relates to an apparatus, method, a computer program product, and a system of testing a data transmission and reception system, the method comprising sending a test signal (110) from a transmitter (14,14') of the system to a receiver (12,12') of the system, and analyzing the received signal (130), wherein the method comprises varying a duty cycle relationship between the test signal and a 5 timing signal (120) used by the receiver (12,12') of the system, and analyzing the effect of the duty cycle variation.

Testing of a Transmission and Reception System

FIELD OF THE INVENTION

This invention relates to a method, a computer program product, a device, and a system for the testing of a transmission and reception system, e.g. to verify reliability of data transfer within equipment using the system. For example, without any limitations, the transmission and reception system will typically be for providing data to, and receiving data from, a high-speed data bus which provides communication between different parts of an integrated circuit (IC) or between different ICs.

10 BACKGROUND OF THE INVENTION

Serial communication transceivers (transmitter/receiver devices) are widely used for data transfer between ICs, circuit boards and systems. The interfaces can operate at data rates above the capabilities of test equipment used in production, and this presents difficulties for the hardware testing. The high-speed interfaces need to correctly reconstruct received bits from the received signal in the presence of a certain level of distortion, particularly jitter.

Considerable design effort is required to achieve the high data rates and guarantee operation under relevant process, voltage and temperature variations. As a consequence, small production flaws can cause the interface to be out of its specification limits.

Existing production test methods aimed at detecting structural faults may not be capable of detecting all relevant production faults in the circuitry for high speed interfaces. It is possible to design test equipment specifically for a particular system to measure the jitter generation at the transmitter and jitter tolerance at the receiver. However, this is an expensive and time consuming approach and may not be viable.

A widely used alternative for specification-based testing in production is the use of a so-called “loop-back test”, by which a known transmitter output is supplied to a receiver, and analysis of the received signal can be used to test the complete system characteristics. The loop-back test is typically supported by
5 embedded pattern generation and bit error counters, in order to decrease test equipment requirements.

A disadvantage of this method is that the range of defects that can be detected is limited for both the transmitter and receiver, particularly as the receiver is designed to tolerate certain amounts of jitter and attenuation from
10 the transmitter.

Phase locked loops are typically used for the generation of internal clock signals from an external system clock signal. In synchronous systems, the accuracy of different internal clock signals, with respect to the master system clock signal, is one factor which influences the performance of the transmission and
15 reception of data between different parts of the system which are operated by different internal clocks. There will typically be a phase shift between the system clock signal and the master clock signal, and the way this phase difference varies over time (the time derivative of phase difference) is defined as the timing jitter.

Bit errors occur when interpreting received data if a recovered clock
20 edge samples a neighbouring bit in the bit stream, and if this neighbouring bit has an opposite value. Due to jitter, the moment of the data transitions vary around their ideal moment. Jitter has different physical root-causes; some root-causes like thermal noise result in a Gaussian distributed probability (Random Jitter, RJ) while other root-causes like cross-talk cause deterministic jitter (DJ) and have other types of
25 distributions. Since the RJ is unbounded there is always a probability of a bit error. In normal conditions, the design margin guarantees that the probability of a bit error is low, for example a probability (i.e. Bit Error Ratio) of 10^{-12} is often used in specifications.

One known method to improve the detection capability of a loop-back
30 test is to insert jitter into the high-speed signal. Jitter can be inserted using a voltage-controlled variable delay element, generally driven by a sine wave. The jitter can be inserted on-chip or off-chip. The level of inserted jitter has to be known accurately to

make this method suitable for production test. Off-chip implementation requires specific equipment as well as probing and routing of high-speed signals.

On-chip jitter insertion often suffers from poor reliability under process, voltage and temperature variations.

- 5 An example of a self-test circuit for testing the PLL phase and jitter is described in EP 0 889 411, and this uses the introduction of known delays, and comparison measurements are used to derive a measure of average maximum jitter.

SUMMARY OF THE INVENTION

- 10 According to a first aspect of the present invention, a method is described, a method of testing a data transmission and reception system is described, the method comprising sending a test signal from a transmitter of the system to a receiver of the system, and analyzing the received signal, wherein the method comprises varying a duty cycle relationship between the test signal and a timing
15 signal used by the receiver of the system, and analyzing the effect of the duty cycle variation.

- According to a second aspect of the present invention, an apparatus for testing a data transmission and reception system is described, comprising a test unit configured to generate a test signal for transmission; a duty cycle control unit
20 configured to vary a duty cycle relationship between the test signal and the timing signal used by the receiver of the system; and an analyzing unit configured to analyze a received signal which comprises the transmitted signal after the effect of duty cycle variation, said analyzing comprising analyzing the effect of the duty cycle variation.

- According to a third aspect of the present invention, a data
25 transmission and reception system is described, comprising: a transmitter; a receiver; and a testing apparatus as explained above.

 According to a fourth aspect of the present invention, a computer-readable storage medium encoded with instructions is described that, when executed by a computer, perform:

- 30 - sending a test signal from a transmitter of a data transmission and reception system to a receiver of the system, and analyzing the received signal, and varying a duty cycle relationship between the test signal and a timing signal used by the receiver of the system, and analyzing the effect of the duty cycle variation.

According to a fifth aspect of the present invention, a computer program is described, the computer program comprising sending a test signal from a transmitter of a data transmission and reception system to a receiver of the system, and analyzing the received signal, and varying a duty cycle relationship between the test signal and a timing signal used by the receiver of the system, and analyzing the effect of the duty cycle variation.

Varying the duty cycle relationship between the test signal and the timing signal of the receiver may be performed by shifting the falling edges and/or shifting the rising edges of the test signal on the time axis, so that the duty cycle of the test signal is varied. Furthermore, varying the duty cycle relationship between the test signal and the timing signal of the receiver may be performed by shifting the falling edges and/or shifting the rising edges of the timing signal on the time axis, so that the duty cycle of the timing signal is varied. Of course, a combination of varying the duty cycle of the test signal and varying the duty cycle of the timing signal may also be performed. The timing signal may represent the clock recovered in the receiver which is used for sampling the received signal.

For instance, the transmitted test signal may represent a signal, wherein data bits with '1' are transmitted with a high voltage level and data bits with '0' are transmitted with a low voltage level. Then, varying the duty cycle may be achieved by shifting arising edge and the succeeding falling edge (i.e. the successor on the time-axes) of the transmitted test signal together in order to decrease the duty cycle, or by shifting a rising edge and the succeeding falling edge of the transmitted test signal apart from each other in order to increase the duty cycle.

Or, for instance, varying the duty cycle may be achieved by shifting the falling edges of the transmitted test signal in negative time direction in order to decrease the duty cycle, or by shifting the falling edges of the transmitted test signal in positive time direction in order to increase the duty cycle, thereby not shifting the rising edges.

Or, as another example, varying the duty cycle may be achieved by shifting the rising edges of the transmitted test signal in positive time direction in order to decrease the duty cycle, or by shifting the rising edges of the transmitted test signal in negative time direction in order to increase the duty cycle, thereby not shifting the falling edges.

Of course, any other well-suited method of varying the duty cycle may be applied.

The test signal may be considered as a loop-backed signal with inserted duty cycle distortion (DCD), which is looped-back from the output of the transmitter and may be connected to receiver input pins.

Varying the duty cycle relationship may be considered as a kind of degradation of the test signal with respect to the timing signal.

Varying the duty cycle relationship provides duty cycle distortion (DCD), and this can be considered as a form of embedded jitter insertion. This type of jitter can be measured relatively easily, for example with a low-pass filtered DC measurement. Furthermore, for instance, the DCD may be measured back, so that the required accuracy of induced DCD is low, which may allow an on-chip implementation of DCD to be relatively simple.

In particular, the method does not require any alteration to the transmitter or receiver functional operation and may be implemented with low use of IC area and with simple test equipment.

The data transmission and reception system may represent any kind of data transmission and reception system, e.g. a Universal Serial Bus (USB) transmission and reception system, or a High Definition Multimedia Interface (HDMI). Thus, the data transmission and reception system may be configured to transmit and receive high speed data, e.g. with data rates higher than 1 Mbit/s. It has to be noted, that the present invention is not restricted to high speed data transmission and reception system.

For instance, the data transmission and reception system may be implemented on an IC. Furthermore, as an example, the apparatus for testing the data transmission and reception system may be implemented on the same IC. Thus, the apparatus may be configured to perform a built-in self-test (BIST) mechanism within the IC in order to verify the data transmission from the transmitter to the receiver of the data transmission system.

The duty cycle control unit may be considered as a kind of cable emulator, simulating cable effects by means of varying the duty cycle as mentioned above. The duty cycle control unit is configured to be controllable, i.e. the duty cycle

variation can be modified, so that the duty cycle control unit may be considered to represent a programmable cable emulator.

Furthermore, as another exemplary alternative, the duty cycle control unit may be placed on a separate test board. In case the duty cycle control unit is placed separate from the IC, no on-chip hardware is needed to stress the test signal.

For instance, for some High Speed I/O interfaces (e.g. PCI Express), the transmitter and receiver pads are separated, so that a dedicated loopback path may be inserted for test purposes. However, in other bi-directional interfaces (e.g. USB2.0 or USB3.0) the transmitter and receiver pads can be shared, in which case the transmitter output and receiver input are the same. In these cases, there is no loopback path provided for test purposes. The invention can still however be implemented, by adding the duty cycle control unit in the functional path. This requires a bypass possibility for the functional signal, which can be implemented by alteration of the transmitter or receiver functional operation.

According to an embodiment of the present invention, varying a duty cycle relationship comprises varying the duty cycle of the test signal.

Thus, as an example, a duty cycling varying unit configured to vary the duty cycle of the test signal may be used. For instance, in case said data transmission and reception system is implemented on an IC, this duty cycling varying unit may also be implemented on the same IC, but the duty cycling varying unit may also be placed as a separated unit from the IC.

According to an embodiment of the present invention, the duty cycle of the test signal is varied in the path between the transmitter output and the receiver input.

Thus, the duty cycling varying unit may be placed in this path between the transmitter output and the receiver unit.

However there are other ways of varying the duty cycle relationship, for example varying a duty cycle of a clock recovered in the receiver which is used for sampling the received test signal.

According to an embodiment of the present invention, the varying the duty cycle comprises splitting the transmitter output into two branches, and delaying

the signal of one branch by a programmable amount of time, and combining the signals of the two branches.

For instance, the two branches may be combined by means of an AND gate, so that the duty cycle of the combined signal is decreased.

5 Furthermore, for instance, the two branches may be combined by means of an OR gate, so that the duty cycle of the combined signal is increased.

According to an embodiment of the present invention, the signals in the two branches are combined using parallel AND and OR gates, and the method further comprises selecting an increased or decreased duty cycle using a multiplexer.

10 The AND gate output gives a decreased duty cycle while the OR gate gives an increased duty cycle. The programmable load and multiplexer control can be provided by a shift register arrangement.

According to an embodiment of the present invention, the delaying the signal of one branch comprises adding a programmable amount of load.

15 For instance, the one branch for delaying the signal comprises at least one buffer, and adding the programmable amount of load to one of the at least one buffer causes a delay of the signal in this branch. Furthermore, the other branch may also comprise at least one buffer. For instance, both branches may comprise the same number of buffers, so that both branches introduces the same time delay when the
20 programmable amount of load is zero. Thus, by means of adding the programmable amount of load, a defined delay to the signal in the one path can be added with respect to the signal in the other path. It has to be understood, that the above-mentioned buffers may also represent drivers.

According to an embodiment of the present invention, the delaying the
25 signal of one branch comprises using a programmable drive strength.

For instance, the one branch for delaying the signal represents the first branch and the other branch represents the second branch.

The first branch may comprise a driver, wherein the drive strength of the driver can be programmed. Thus, according to the programmed drive strength, the
30 delay of the signal in the first branch can be varied.

According to an embodiment of the present invention, the varying a duty cycle relationship comprises varying a duty cycle of a clock which is used for sampling the received test signal.

Thus, the duty of cycle of the timing signal of the receiver may be varied in order to vary the duty cycle relationship.

For instance, assuming that the receiver is implemented on an IC, the actual amount of inserted DCD can be measured internally (on-chip), or off-chip on
5 the Rx pins.

According to an embodiment of the present invention, the test signal provided to the receiver is low-pass filtered, and a dc voltage of the low-passed filtered signal is measured, wherein the dc voltage represents the duty cycle.

For instance, a low-pass filter connected to a dc voltage meter may be
10 used for determining the duty cycle. This low-pass filter and the dc voltage meter may be considered to represent a duty cycle measurement unit. Furthermore, this duty cycle measurement unit may be configured to be switched on/off. When being switched off, then low-pass filter may have no influence to the test signal provided to the input of the receiver. Instead of the dc voltage meter (DVM), an other suited
15 measurement unit like a Parametric Unit (PMU) may be used.

For instance, the signal can be low-pass filtered by connecting resistors to the two differential Rx pins and a capacitor between the two resistor's other terminals. After a multiple of (e.g. 7, but any other well-suited multiple may also applied) the RC time constant, a stable measurement of the DC voltage can be made.
20 Assuming a test pattern for the test signal having the same numbers of '0' and '1, e.g. like a ...010101... pattern, a 0V level is expected in the case of a 50% duty cycle. Under presence of DCD the resulting DC level will differ proportionally to the amount of DCD (which may have units of time, such as picoseconds).

The difference with the DC value when no DCD is inserted may be of
25 particular interest. This relative measurement can be made with good accuracy in a production test, limited for example by the PMU or DVM resolution, for example 250 micro-Volts for a typical test equipment PMU.

According to an embodiment of the present invention, the test signal provided to the receiver is sampled and the number of sampled '1's and/or '0's is
30 counted, where the ratio of counted '1's to the total number of samples represents the duty cycle.

According to an embodiment of the present invention, the analysis comprises bit error ratio measurement.

The combination of insertion of various amounts of DCD and bit-error ratio measurements allows a small number of measurements to be taken, in a sufficiently short time that is suitable for production testing. The measurement results can be used to calculate relevant jitter properties like random jitter (RJ), deterministic jitter (DJ) and total jitter (TJ). Total jitter is a known combination of the DJ and RJ characteristics of the transceiver under test, using statistical methods.

According to an embodiment of the present invention, the analyzing the received signal comprises providing a pass or fail indication based on the duty cycle variation and a measured receiver error rate.

For instance, assuming that the duty cycle control unit is implemented on a chip, the actual amount of inserted DCD may vary from chip to chip due to spread in process parameters, so that the measured inserted DCD and corresponding BER may be processed to determine a pass/fail condition.

According to an embodiment of the present invention, the analyzing the received signal comprises calculating the jitter from the duty cycle variation and a measured receiver error rate.

For instance, a statistical evaluation can be used to extract the relevant jitter levels from the measured DCD and corresponding BER.

According to an embodiment of the present invention, a clock recovery from received data is performed in the receiver and the recovered clock is used to interpret the received data.

For instance, phase lock loop (PLL) may be used for clock recovery. The receiver may use a clock-and-data recovery (CDR) circuit having a PLL which locks to the received signal. Depending on the PLL implementation, locking may be done on one or both edges.

The recovered CDR clock is typically used to sample the received high speed data on both rising and falling edges. With the CDR locking on one edge of the received signal, the DCD causes the opposite data edge to be displaced with respect to its normal position. This results in an increased probability of bit errors on those edges. For instance, a bit-error counter in the receiver allows this probability to be measured.

According to an embodiment of the present invention, clock recovery is performed from the rising or falling edges of the received data, and the effect of

duty cycle variation for a recovered clock using the rising edges of the received data and for a recovered clock using the falling edges of the received data is analyzed.

For instance, assuming that a PLL is used, the clock recovery is performed by PLLs that lock on one edge, and then jitter on rising and falling edges can be measured separately. This may increase the diagnostic possibilities needed to find rootcauses of detected faults. For instance, the edge used by the PLL to lock can be made selectable, to enable detection of faults related to both edges.

According to an embodiment of the present invention, clock recovery is performed from rising and falling edges of the received data.

Thus, the PLL may lock on both edges, and the inserted DCD will affect both edges.

The invention may be used for detecting production faults in the transmitter or receiver hardware, which can cause increased jitter generation and/or decreased jitter tolerance, as these result in higher BER of the loopbacked signal.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE FIGURES

In the Figures show:

Fig. 1a a schematic block diagram of a first exemplary embodiment of an apparatus according to the present invention;

Fig. 1b a schematic flowchart of a first exemplary embodiment of a method according to the present invention;

Fig. 1c a schematic block diagram of a second exemplary embodiment of an apparatus according to the present invention;

Fig. 2 a schematic block diagram of an exemplary embodiment of a duty cycle control unit according to the present invention;

Fig. 3 a schematic block diagram of an exemplary embodiment of a switch in the exemplary embodiment of a duty cycle control unit;

Fig. 4 a schematic timing diagram for illustrating the operation the duty cycle control unit;

- Fig. 5 a schematic block diagram of an exemplary embodiment of a measurement unit;
- Fig. 6 a schematic simulation of low-pass filtered clock signals;
- Fig. 7 a schematic timing of a first exemplary duty cycle variation;
- Fig. 8 a schematic timing of a second exemplary duty cycle variation;
- Fig. 9 a schematic timing of a third exemplary duty cycle variation;
- Fig. 10 a schematic block diagram of a first exemplary embodiment of a circuit configured to switch between PLL lock edges;
- Fig. 11 a schematic block diagram of a second exemplary embodiment of a circuit configured to switch between PLL lock edges;
- Fig. 12 a schematic flowchart of a second exemplary embodiment of a method according to the present invention;
- Fig. 13 a schematic flowchart of a second exemplary embodiment of a method according to the present invention;
- Fig. 14a a first schematic flow diagram exemplarily illustrating the effect of duty cycle distortion; and
- Fig. 14b a second schematic flow diagram exemplarily illustrating the effect of duty cycle distortion.

DETAILED DESCRIPTION OF THE EMBODIMENTS

In the following detailed description, exemplary embodiments will be described.

Fig. 1a depicts a schematic block diagram of a first exemplary embodiment of an apparatus 100' according to the present invention. This apparatus 100' will be described in combination with the schematic flowchart of a first exemplary embodiment of a method according to the present invention depicted in Fig. 1b.

The apparatus 100' is configured for testing a data transmission and reception system 12', 14', 16'. The apparatus 100' comprises a test unit 20' configured to generate a test signal for transmission; a duty cycle control unit 18' configured to

vary a duty cycle relationship between the test signal and the timing signal used by the receiver 12' of the system; and an analyzing unit (not depicted in Fig. 1a) configured to analyze a received signal which comprises the transmitted signal after the effect of duty cycle variation, said analyzing comprising analyzing the effect of the duty cycle variation.

The data transmission and reception system comprises a receiver 12', a transmitter 14' and a control unit 16', wherein the receiver 12' and the transmitter 14' may represent a transceiver 10'. For instance, reference sign 15 represents a communications bus for transmitting data from the transmitter 14', and reference sign 15' represents a communications bus for receiving data at the receiver 12'. The data transmission and reception system may represent any kind of data transmission and reception system, e.g. a Universal Serial Bus (USB) transmission and reception system, or a High Definition Multimedia Interface (HDMI). Thus, the data transmission and reception system may be configured to transmit and receive high speed data, e.g. with data rates higher than 1 Mbit/s. It has to be noted that the present invention is not restricted to high speed data transmission and reception system. For instance, the data transmission and reception system may be implemented on an IC.

The test unit 20' is connected to the control unit 16' of the data transmission and reception system, and the test unit 20' is configured to provide a test signal to the control unit 16', so that this test signal is send via the transmitter 14'. The test signal may represent a random test signal pattern, a or predefined test signal pattern, or a combination of both. Furthermore, the test unit 20' is connected to the duty cycle control unit 18.

The output of the transmitter 14' is looped-back to the input of the receiver 10' via the duty cycle control unit 18'.

Varying the duty cycle relationship between the test signal transmitted from the transmitter 14' and the timing signal of the receiver 12' may be performed by shifting the falling edges and/or shifting the rising edges of the test signal on the time axis, so that the duty cycle of the transmitted test signal is varied. Furthermore, varying the duty cycle relationship between the test signal and the timing signal of the receiver may be performed by shifting the falling edges and/or shifting the rising edges of the timing signal on the time axis, so that the duty cycle of the timing signal is varied. Of course, a combination of varying the duty cycle of the test signal and

varying the duty cycle of the timing signal may also be performed. Varying the duty cycle according to the present invention will be exemplarily explained in the sequel with respect to Figs. 4, 7, 8 and 10.

5 The timing signal may represent the clock recovered in the receiver 12' which is used for sampling the received signal.

The test signal is send from the transmitter 14' of the system to the receiver 12' of the system, as indicated by step 110 in Fig. 1d. A duty cycle relationship between the test signal and a timing signal used by the receiver 12' is varied by means of the duty cycle control unit 18', as indicated by step 120 in Fig. 1b.

10 The test signal received at the input of receiver 12' may be considered as a loop-backed signal with inserted duty cycle distortion (DCD). Varying the duty cycle relationship may be considered as a kind of degradation of the test signal with respect to the timing signal. The received signal is analyzed (Fig. 1b: step 130), wherein the effect of the duty cycle variation is analyzed. This analyzing may be performed by means of the analyzing unit, wherein this analyzing unit may be implemented in the test unit 20, or at any other location. For instance, the analyzing unit may determine a bit error ratio (BER) of the received signal, wherein the BER depends on the variation of duty cycle relationship.

15 For instance, the apparatus 100' may comprise a measurement unit (not depicted in Fig. 1a) configured to measure the duty cycle introduced by the duty cycle control unit 18'.

Varying the duty cycle relationship may be considered as a kind of degradation of the test signal with respect to the timing signal, wherein varying the duty cycle relationship provides duty cycle distortion (DCD), and this can be considered as a form of embedded jitter insertion.

25 This type of jitter can be measured relatively easily, for example with a low-pass filtered DC measurement, i.e. the optional measurement unit may comprise said low-pass filtered DC measured which is connectable to the input of the receiver 12'. Furthermore, for instance, the DCD may be measured back, so that the required accuracy of induced DCD is low, which may allow an on-chip implementation of DCD to be relatively simple.

30 Thus, the invention may be considered to be based on the addition of duty-cycle distortion (DCD) to displace the position of data edges with respect to the

recovered clock edges in a controlled and measurable way. The probability of bit errors, measured as a BER, will then be higher. For instance, from the measured edge displacement and corresponding BER the standard deviation of the random jitter (RJ) can be calculated, as well as the peak-to-peak level of the deterministic jitter (DJ).

5 In particular, the present invention does not require any alteration to the transmitter or receiver functional operation and may be implemented with low use of IC area and with simple test equipment.

 The invention relates to the testing of a transmission and reception system. The invention may applied to a system in which a Clock and Data Recovery (CDR) circuit is used in the receiver to derive clock timing information and perform
10 data recovery from a received data stream.

 There are many different architectures suitable for CDR circuits. For instance, three main architectures can be classified as an over-sampling architecture, a tracking architecture and a phase-interpolation architecture.

15 In an over-sampling architecture, multiple samples are taken for each bit period. An algorithm decides which bit is best suited to use. For very high speed signals, it becomes impractical to build clocks that allow data oversampling.

 In a tracking architecture, a phase locked loop is used that locks on the received data. With a phase interpolation architecture, which is essentially an
20 alternative form of tracking, the transmit clock is used and phase aligned with the incoming data, so only the phase is tracked. This is usually done by a loop that selects the phase that is closest to the data transition.

 In the sequel, exemplary embodiments of the invention will be given based on a tracking architecture using a PLL, although it will be apparent that the
25 invention can also be applied to other architectures.

 As mentioned above, the invention may be considered to be based on the addition of duty-cycle distortion (DCD) to displace the position of data edges with respect to the recovered clock edges in a controlled and measurable way.

 When locking occurs on either the rising or falling edge of the received
30 bitstream, the introduced DCD will essentially displace the opposite data edges with respect to the recovered clock edges, covering faults related to these edges. To cover faults related to the other edges, a test procedure is required that allows to select the edge on which the CDR PLL locks.

Fig. 1c depicts a schematic block diagram of a second exemplary embodiment of an apparatus according to the present invention using DCD insertion. This second exemplary embodiment of an apparatus according to the present invention is based on the first exemplary embodiment of the apparatus 100' depicted in Fig. 1a. Thus, the explanations and advantages mentioned above with respect to the first exemplary apparatus 100' also hold for the second exemplary apparatus depicted in Fig. 1c.

The data transmission and reception system comprises a transceiver 10 having a receiver 12 and a transmitter 14, and these interface between a communications bus 15, 15' and a serial circuit 16. A loopback path is defined between the output of the transmitter 14 and the input of the receiver 12, and this path comprises a duty cycle distortion (DCD) element 18, which may corresponds to the duty cycle control unit 18' depicted in Fig. 1c. The DCD element 18 is controlled by a test register 20 which also performs analysis of the signals received by the circuit 16 using the receiver 12. In the example shown, this analysis involved bit error ratio (BER) measurement, implemented by BER unit 22. The control of the DCD element is shown as 24. Thus, compared to the first exemplary apparatus 100, the test register 20 may correspond to the test unit 20', receiver 12 may correspond to receiver 12', transmitter 14 may correspond to transmitter 14', and circuit 16 may correspond to the control unit 16'.

Fig. 1c also shows that the signal to which DCD has been applied is also supplied to an optional measurement circuit 26', which may be on or off-chip, and this enables measurement of the applied DCD before the signal has passed through the receiver.

Fig. 1c also shows that the test register 20 may have a control output "select lock edge". As will be described below, this may or may not be required, depending on the manner in which clock recovery is carried out.

Fig. 1c also shows data communications paths 26 between the test register 20 and the circuitry 16. Figure 1b also shows an optional "test_enable" control signal which enables selection of different test modes, for example the loopback mode, a pattern generation mode, and an error compare mode. For instance and with out any limitations, the implementation of the invention may be considered as five operations:

- DCD insertion;
- DCD measurement;
- Selection of lock edge (if required);
- BER measurement; and
- 5 - Jitter analysis.

The optional jitter analysis is not shown in Figure 1c, and this analysis can be implemented as software on the test equipment.

The insertion of Duty Cycle Distortion can be implemented in several different ways. One possibility is to use the intrinsic difference in fall and rise time of
 10 circuit elements. For example, a standard multiplexer with two inputs A and B in a given CMOS process has a difference between fall and rise time of the order of 20ps. A chain of multiplexers can be configured, where each multiplexer output connects to input A of the next multiplexer, and input B connects to the original signal. Each multiplexer adds then a DCD of 20 ps to the signal; and the total DCD can be
 15 programmed by selecting the number of multiplexers in the signal path. In this implementation of DCD the original exemplary signal is used to drive all multiplexer inputs B, which requires a large buffer for this signal.

Fig. 2 depicts a schematic block diagram of an exemplary embodiment of a duty cycle control unit, i.e. a duty cycle distortion element which may be used for
 20 the DCD element 18 depicted in Fig. 1c or for the duty cycle control unit 18' depicted in Fig. 1a.

Fig. 2 shows an $n+1$ bit programmable DCD element. In the DCD element 18 of Fig. 2, the high-speed signal from the transmitter is used in two branches, "TXdelayed" (branch 30) and "TXbuf" (branch 32). Each branch comprises
 25 first and second buffers 30a,30b and 32a,32b. The signal propagates with a certain delay through these branches.

For the branch 30 "TXdelayed", the delay can be increased by selectively adding load to the first buffer 30a. As alternative, the drive strength of the buffer can be made programmable, if needed in combination with programmable load.

30 Load-selection bits "DCD delay[0..n]" are programmed by shifting control bits into a test register 20. The values of the loads are then chosen as a binary coded (1,2,4 .. $2n$) multiple of a capacitance value $x1$. A linear array of switches $S0 - S_n$ couple the capacitors to the output of the buffer 30a, 20 where $n+1$ is the number

of switches used. The control bits “DCD delay[0..n]” control the switches S0 to Sn, and when a switch is closed the capacitance is added to the load seen by the buffer.

For instance, each switch S0 – Sn can be implemented as a transmission gate as shown in Fig. 3.

5 The two branches TXdelayed and TXbuf in Figure 2 are used as inputs to an AND gate 40 as well as an OR gate 42 in parallel. The output of the AND gate “TXand” provides a signal with reduced duty cycle; and the OR gate output “TXor” provides a signal with increased duty-cycle.

10 Fig. 4 depicts a schematic timing diagram for illustrating the operation of the duty cycle unit of Fig. 2. In this timing diagram, the signals TXdelayed 30' and TXbuf 32' in the two branches are illustrated, and the outputs 40', 42' from the AND and OR gates 40, 42 for a given relative delay between the two branches are depicted. The difference in duty cycle between the signals TXand 40' and TXor 42' can clearly be seen.

15 The increased duty-signal 42' or decreased duty-cycle signal 40' may be selected by a multiplexer 44 (shown in Figure 2). The multiplexer control signal “DC_decrease_increase” is provided by the test register 20.

20 The buffers 30a, 30b, 32a, 32b, AND/OR gates 40, 42 and multiplexer 44 potentially add to the DCD, so that the DCD is not dependent solely on the capacitive load added. This is not critical since the DCD may also be measured at the receiver pins by the optional circuitry 26' shown in Fig. 1b.

25 However, any DCD added by these circuits will be present as a DCD offset. An unbalanced offset could create the risk that the duty cycle cannot be increased or decreased sufficiently to produce a significant amount of bit errors in limited time.

30 For this reason, buffers are added in both branches 30, 32, as shown, to make the default delay through both branches approximately equal. At least one buffer in the TXbuf branch 32 is needed to physically separate the two branches. To allow the range of programmable DCD decrease and increase to be as equal as possible, the nominal delay in both branches should be equal.

 The duty-cycle distortion can be measured at the circuitry 26' (of Fig. 1b) in various ways, for example using an oscilloscope. For production test it is preferred to have low requirements to equipment. One piece of equipment that is

generally available in a test system is a Parametric Measurement Unit (PMU). A PMU can be used to measure DC voltage and currents. In testers equipped with a Digital Voltmeter (DVM) the DVM can also be used.

With the addition of a low-pass filter the PMU or DVM can also be used to measure the duty cycle of a bit-stream. One exemplary implementation is to add a lowpass filter on the tester-to-device interface board, as depicted in Fig. 5, which illustrates a schematic block diagram of an exemplary embodiment of a measurement unit. For example two resistors 50 connecting to the receiver pins 48 and a capacitor 52 connected to the other two terminals of the resistors, as shown schematically in Fig. 1c and in more detail in Fig. 5, may be used, wherein the resistor-capacitor arrangement functions as a low pass filter, and of course other filter configurations can be used. For instance, each of the resistors 50 may have a value of 50 Ohm, and the capacitor 52 may have a capacitance of 10 nF, but of course any other suited values may also be applied for the resistors 50 and the capacitor 52.

Inside the receiver, the clock is generated by means of clock generators 54 and 56.

The DC value of the output voltage V_{out} measured between the two terminals of the capacitor is an RC charge curve, as exemplarily represented in Figure 6. Fig. 6 depicts a schematic simulation of low-pass filtered clock signals, wherein the clock generators 54 and 56 are exemplarily configured (without any limitations) to operate at 400 mV, 2500 MHz and 50 ps rise. The x-axis of Fig. 6 depicts the measured voltage and the y-axis represents the time-axis.

The time constant is derived from the sum of the two resistors (i.e., in case of the exemplary values mentioned above, the time constant would be $2 \cdot 50 = 100$ Ohm for the resistors used in Fig. 5). The circuit in Fig. 5 is of course only one example, and in other interface implementations voltage levels may be different, for example due to external DC biasing or an external load to a reference voltage.

Fig. 6 shows a simulation of low-pass filtered clock signals with 50% duty cycle (plot 60) and 49.5% duty cycle (plot 62). The reduced duty cycle corresponds to DCD of 2 ps. The resulting DC value is an average of the time 'high' minus the time 'low' of the high-speed signal. The 50% duty-cycle clock signal will approach a DC level of 0V at V_{out} .

For instance, the DC output voltage on the positive leg will be:

$$V_{outDC,positive\ leg} = V_{min} + (1 - e^{-\frac{t}{RC}})^{19} * (duty_cycle) * (V_{max} - V_{min})$$

With V_{max} and V_{min} being the 'high' respectively 'low' voltage.
Similarly, the DC output on the negative leg is:

5

$$V_{outDC,negative\ leg} = V_{max} - (1 - e^{-\frac{t}{RC}}) * (duty_cycle) * (V_{max} - V_{min})$$

The resulting DC output voltage V_{out} over the capacitor terminals is
the difference:

10

$$\begin{aligned} V_{outDC} &= V_{outDC,positive\ leg} - V_{outDC,negative\ leg} \\ &= V_{min} - V_{max} + 2 * (1 - e^{-\frac{t}{RC}}) * (duty_cycle) * (V_{max} - V_{min}) \end{aligned}$$

For the example of Figure 6, the signal with 49.5% duty cycle, for
15 $V_{max}=400mV$ and $V_{min}=0V$ will approach:

$$V_{outDC} = -0.4 + 2 * (1 - 0) * 0.495 * 0.4 = -4\ mV.$$

The output voltage can also be measured between one of the two
20 capacitor terminals and a reference voltage (e.g. ground).

As an example, the low-pass filter can be implemented on-chip, with
on-chip switches connecting the low-pass filter to the high-speed signal. The output
signal V_{out} has to be made observable at IC pins, for example using an analog test
bus (for example IEEE 1149.4).

25 The DC voltage measurement is directly affected by voltage amplitude
as well as the duty-cycle. For instance, the output voltage levels are measured in a
separate dedicated test, and these measured levels are used to determine the duty cycle
in combination with the low-pass filtered DC test.

As mentioned above, there are several options of selecting how to
30 implement the lock edge for clock recovery. For instance, one option is the use of a
PLL which locks on both edges, and another option is the use of a PLL which locks
on one edge.

The use of PLLs that lock on both edges within the clock and data recovery (CDR) circuit results in both data edges being displaced with respect to their ideal location as a result of the introduction of DCD. Thus, both edges contribute to an increased BER.

5 Fig. 7 depicts a schematic timing diagram of a first exemplary duty cycle variation with a recovered clock at the full data rate. Of course, a different clock rate versus data rate is possible. Most commonly, full rate and half rate CDRs are used. For a full rate CDR, 1 clock cycle corresponds to 1 bit, and the rising edge is used for clock recovery, and the falling edge is used for data recovery. For a half rate
10 CDR, 1 clock cycle corresponds to 2 bits, and both the rising and falling edges are used for clock recovery. A 90 degree phase shifted clock is used for data recovery, and recovered clock has half the frequency of the data rate. Full data rate clock recovery is shown by way of example.

The example signals in Figure 7 are for a “10101” pattern; for other
15 patterns the displaced edge positions will differ according the transitions.

The top plot 70, of the input data, shows a 50% duty cycle. The next two plots 72, 74 show the transitions between 1 and 0 shifted to provide decreased and increased duty cycle respectively. In this example, varying the duty cycle is achieved by shifting the a rising edge and the succeeding falling edge (i.e. the
20 successor on the time-axes) of the input data together in order to decrease the duty cycle (signal 72), or by shifting a rising edge and the succeeding falling edge of the input data apart from each other in order to increase the duty cycle (signal 74). The transitions move symmetrically about the center of the eye diagram. When the duty cycle is either decreased or increased, the probability of having an error in sampling
25 any other bit increases.

The plot 76 shows the recovered clock, in which the clock 1 to 0 transition has been timed with the center of the detected input data eye. This 1 to 0 clock transition is used to recover the data as represented by arrow 79.

The use of PLLs that lock on one edge results in the data edge on
30 which the CDR PLL will lock to be fixed. The data edges opposite to the edges on which the PLL locks are the displaced edges and faults related to these edges will contribute to the BER. Figure 8 again shows a recovered clock at the full data rate, and the different plots in Figure 8 correspond to those in Fig.7.

The example signals in Fig. 8 are again for a “10101” pattern, and the displaced edges 80 are those associated with the falling edges of the data. Thus, in this example, varying the duty cycle is achieved by shifting the falling edges of the input data in negative time direction in order to decrease the duty cycle (signal 72’), or by shifting the falling edges of the input data in positive time direction in order to increase the duty cycle (signal 74’), thereby not shifting the rising edges.

If the duty cycle is decreased, and locking occurs on rising edges (as in the second plot of Figure 8), the probability increases of having an error in sampling the last high bit before a transition to low.

When the duty cycle is increased (the third plot in Figure 8), the probability increases of having an error in sampling the next low bit just after a transition to low increases.

From the above, it can be seen that under presence of inserted DCD, the jitter related to the edge on which the PLL locks will not increase the BER, only jitter related to the next transition will increase the BER.

Potential faults related to the data edges on which the PLL locks are then not detected.

To overcome this possible drawback, the edge on which the PLL locks can be made to be switchable.

Fig. 9 shows the same plots as Figure 8, but with the CDR signals locking on falling edges, so that the displaced edges 90 are those associated with the rising edges of the data.

In this case, if the duty cycle is decreased (second plot in Figure 9), the probability of having errors related to the rising edges increase. Similarly, if the duty cycle is decreased, the probability of having errors related to the falling edges increases (third plot in Figure 9). Thus, in this example, varying the duty cycle is achieved by shifting the rising edges of the input data in positive time direction in order to decrease the duty cycle (signal 72’’), or by shifting the rising edges of the input data in negative time direction in order to increase the duty cycle (signal 74’’), thereby not shifting the falling edges.

In this way, by making the locking edge selectable, all rising and falling transitions contributing to BER can separately be tested. This is the purpose of the control signal 25 in Fig. 1b.

Fig. 10 shows one way to implement a selectable lock edge, in which the data on which the PLL locks is inverted.

An inverter 100' is used to provide inverted data, and the original data and the inverted data are provided to a multiplexer 102 which selects one of the data signals based on a control input "Select_lock_edge" 25. The control signal
5 "select_lock_edge" can be provided by the test register 20.

As a second example, shown in Figure 11, an XOR gate 110 can be used with the "Select_lock_edge" control signal and the data ("data_in") as inputs.

As a third exemplary alternative, if the signals used are differential
10 signals, the differential polarity can simply be reversed to achieve inversion.

As outlined above, the aim of the analysis to be carried out may be to perform jitter measurement and tests. Jitter is one of the main causes of bit errors in a serial transceiver. A high speed signal with increased DCD will be more susceptible to jitter and cause more bit errors.

15 One way to use the programmable DCD is to increase DCD until a first bit error is observed. Since jitter is partly of a stochastic nature it is unpredictable when a bit error will occur. Therefore, it is preferred to count the number of bit errors, expressed as a bit-error ratio representing the number of received erroneous bits as ratio of the total number of received bits.

20 Bit error counters are well known the art, and conventional devices can be used to implement the unit 22 shown in Fig. 1b.

To perform the jitter analysis based on the obtained bit error ratio measurements, the test equipment records one or more DCD levels with the corresponding bit error ratios.

25 A widely used method to analyse the performance of a receiver is to plot the BER versus eye-opening. The log-linear plot of BER versus eyeopening typically resembles the shape of a bathtub and is often referred to a bathtub curve.

From the bathtub curve, the level of random and deterministic jitter can be estimated using curve-fit techniques. For this, one or more measurement results
30 with level of inserted DCD level and corresponding BER are needed.

These jitter calculations also take into account how the clock recovery has been implemented, particularly whether the PLL lock is done on one or both edges.

An example is a relative simple method using two bathtub curve points is an estimate curve fit method described in IEEE Std 802.3ae-2002, Section 48B.3.1.3.1 “Approximate curve fitting for BERT scan”, pp 510-511. This method estimates the random jitter σ , deterministic jitter, peak-to-peak level and total jitter peak-to-peak level. With this method the quantiles of two BER levels are plotted against the eye-opening. The slope of the straight line drawn between these points corresponds to the random jitter (RJ) level, the point where the quantile (BER)=0 line is crossed indicates the peak-to-peak level of deterministic jitter (DJ). The RJ and DJ are combined in TJ according to

$$TJ = DJ + 13.8 * RJ.$$

As an example of the usage of the invention for production testing, the following exemplary steps can be implemented to complete a jitter test; applied to a PLL that locks on one edge. “Nr_observations” is a pre-determined number of DCD-BER points used in the jitter analysis:

- (i) Select loop-back test mode (step 210)
- (ii) Program DCD delay=0, DC_increase_decrease='0',
select_lock_edge='0' (step 220)
- (iii) Start transmitting patterns (step 230)
- (iv) Measure and store DCD and BER (step 121)
- (v) Increase DCD delay (step 122)
- (vi) Repeat steps (iv)-(v) another “nr_observations-1” times (step 123)
- (vii) Program DCD delay=0, DC_increase_decrease='0',
select_lock_edge='1' (step 240)
- (viii) Repeat steps (iv) – (vi)
- (ix) Program DCD delay=0, DC_increase_decrease='1',
select_lock_edge='0' (step 250)
- (x) Repeat steps (iv) – (vi)
- (xi) Program DCD delay=0, DC_increase_decrease='1',
select_lock_edge='1' (step 260)
- (xii) Repeat steps (iv) – (vi)

- (xiii) Perform jitter analysis: calculate RJ, DJ and TJ (step 270)
- (xiv) Decide pass or fail (step 280)
- (xv) Stop transmitting patterns (step 290)

5 This exemplary method is shown in Figure 12. The method implements a test mode in which a number N of BER measurements are taken for incrementally increasing DCD delay values. The N measurements correspond to the value “nr_observations”. This is performed by the sub-routine shown as 120. This sub-routine is performed for each lock edge and for increasing duty cycles and for
10 decreasing duty cycles. Thus, four separate sets of data are obtained, and the sub-routine is called four times as shown.

In case of a PLL that locks on both edges the signal “select_lock_edge” is not used. The test sequence in that case is:

- 15 (i) Select loop-back test mode (step 210)
- (ii) Program DCD delay=0, DC_increase_decrease='0' (step 220)
- (iii) Start transmitting patterns (step 230)
- (iv) Measure and store DCD and BER (step 131)
- (v) Increase DCD delay (step 132)
- 20 (vi) Repeat steps (iv) – (v) another “nr_observations-1” times (step 133)
- (vii) Program DCD delay=0, DC_increase_decrease='1' (240')
- (viii) Repeat steps (iv) – (vi)
- (ix) Perform jitter analysis: calculate RJ, DJ and TJ (step 270)
- (x) Decide pass or fail (step 280)
- 25 (xi) Stop transmitting patterns (step 290)

This exemplary method is shown in Figure 13. The method implements a test mode in which a number N of BER measurements are again taken for incrementally increasing DCD delay values. This is performed by the subroutine
30 shown as 130. and it is performed for increasing duty cycles and for decreasing duty cycles. Thus, two separate sets of data are obtained, and the sub-routine is called twice as shown.

For instance, the invention can be applied for production testing of high speed interfaces. Examples of serial interfaces are Serial ATA, PCI Express, DVI, HDMI and USB 2.0. The invention can also be used for parallel types of interfaces such as Double Data Rate memory interfaces.

5 The examples shown generally use single polarity signals. However, the use of differential signals in circuits of the invention is also possible.

 The examples described above relate to serial communications systems in which a receiver recovers a clock and data from a serial bitstream. The invention can also be applied to applications of the invention in which a receiver has an
10 externally provided clock. Also, it is possible to apply the DCD to the transmit clock instead of the data. This has the disadvantage of altering the functional circuit. Other applications may be to make a measurable delay between two sample times, where both sample times respond to different transitions of a clock for which duty cycle is altered and measured. Such a measurable delay might be applied for example in
15 delay-fault testing of digital circuits.

 There may thus be considered to be two types of duty cycle distortion, and these may be considered as data DCD and clock DCD. With data DCD, with DCD inserted after the transmitter, a data "1" is made wider (for example) than a data "0". As a result, the common mode voltage increases, and the cross points in the eye
20 diagram are not centered, but are shifted towards the high or lower rails, as shown in Figure 14a. With clock DCD, with DCD inserted before the transmitter and applied to the transmit clock, the common mode voltage is half way between the voltage rails, and the eye diagram transitions shift in time, as shown in Figure 14b. The CDR can latch onto rising or falling edges or both.

25 The use of DCD to provide a measurable affect on the probability of bit errors can be used in other examples of loopback test, in order to increase the sensitivity of the loopback test.

 In the example above, the DCD is inserted in a path between the transmitter and receiver. For some High Speed I/O interfaces (such as PCI Express),
30 the transmitter and receiver pads are separated and a dedicated loopback path is inserted for test purposes. However, in other bi-directional interfaces (such as USB2.0 or USB3.0) the transmitter and receiver pads can be shared, in which case the transmitter output and receiver input are the same. In these cases, there is no loopback

path provided for test purposes. The invention can still however be implemented, by adding DCD in the functional path. This requires a bypass possibility for the functional signal, which can be implemented by alteration of the transmitter or receiver functional operation.

5 In the example above, DCD is measured using a filter and DC measurement technique. DCD can also be measured with other methods, onchip and/or off-chip. For example, random sampling of the signal can be used, dividing the counted number of '1's by the total number of sampled bits.

 Various other modifications will be apparent to those skilled in the art.

10 The invention has been described above by means of exemplary embodiments. It should be noted that there are alternative ways and variations which are obvious to a skilled person in the art and can be implemented without deviating from the scope and spirit of the appended claims.

CLAIMS:

1. A method of testing a data transmission and reception system, the method comprising sending a test signal (110) from a transmitter (14,14') of the system to a receiver (12,12') of the system, and analyzing the received signal (130), wherein the method comprises varying a duty cycle relationship between the test
5 signal and a timing signal (120) used by the receiver of the system, and analyzing the effect of the duty cycle variation.
2. A method as claimed in claim 1, wherein varying a duty cycle relationship comprises varying the duty cycle of the test signal.
10
3. A method as claimed in claim 2, wherein the duty cycle of the test signal is varied in the path between the transmitter output and the receiver input.
4. A method as claimed in one of the preceding claims, wherein varying
15 the duty cycle comprises splitting the transmitter output into two branches (30,32), and delaying the signal of one branch by a programmable amount of time, and combining the signals of the two branches.
5. A method as claimed in claim 4, wherein the signals in the two
20 branches are combined using parallel AND (40) and OR (42) gates, and the method further comprises selecting an increased or decreased duty cycle using a multiplexer (44).
6. A method as claimed in claim 4 or 5, wherein delaying the signal of
25 one branch (30, 32) comprises adding a programmable amount of load.
7. A method as claimed in claim 4 or 5, wherein delaying the signal of one branch (30, 32) comprises using a programmable drive strength.

8. A method as claimed in claim 1, wherein varying a duty cycle relationship comprises varying a duty cycle of a clock which is used for sampling the received test signal.
- 5 9. A method as claimed in one of the preceding claims, wherein the method further comprises low-pass filtering the signal provided to the receiver, and measuring a dc voltage which represents the duty cycle.
- 10 10. A method as claimed in one of the preceding claims, wherein the method further comprises sampling the signal provided to the receiver, counting the number of sampled '1's and/or '0's, where the ratio of counted '1's to the total number of samples represents the duty cycle.
- 15 11. A method as claimed in one of preceding claims, wherein the analysis comprises bit error ratio measurement (121).
- 20 12. A method as claimed in one of the preceding claims, wherein analyzing the received signal comprises providing a pass or fail indication (280) based on the duty cycle variation and a measured receiver error rate.
- 25 13. A method as claimed one of the preceding claims, wherein analyzing the received signal comprises calculating the jitter from the duty cycle variation and a measured receiver error rate.
- 30 14. A method as claimed in one of the preceding claims, wherein the method further comprises performing clock recovery from received data in the receiver and using the recovered clock to interpret the received data.
15. A method as claimed in claim 14, wherein the method comprises performing clock recovery from rising and falling edges of the received data.
16. A method as claimed in claim 14, wherein the method comprises performing clock recovery from the rising or falling edges of the received data, and

wherein the method further comprises analyzing the effect of duty cycle variation for a recovered clock using the rising edges of the received data and for a recovered clock using the falling edges of the received data.

- 5 17. An apparatus for testing a data transmission and reception system, comprising:
- a test unit (20,20') configured to generate a test signal for transmission;
 - a duty cycle control unit (18,18') configured to vary a duty cycle relationship between the test signal and the timing signal used by the receiver (12,12')

10 of the system; and

 - an analyzing unit (22) configured to analyze a received signal which comprises the transmitted signal after the effect of duty cycle variation, said analyzing comprising analyzing the effect of the duty cycle variation.
- 15 18. An apparatus as claimed in claim 17, wherein the duty cycle control unit (18,18') comprises a duty cycle varying unit configured to vary the duty cycle of the transmitted test signal.
19. An apparatus as claimed in claim 17 or 18, wherein the analyzing unit
- 20 comprises a bit error ratio measurement circuit (22).
20. An apparatus as claimed in one of claim 17, 18 and 19, wherein duty cycle varying unit comprises:
- a splitter for splitting a transmitter output into two branches (30,32), a

25 delay element for delaying the signal of one branch (30) by a programmable amount of time; and

 - a combiner (40,42,44) for combining the signals of the two branches.
21. An apparatus as claimed in claim 20, wherein the combiner comprises
- 30 parallel AND (40) and OR (42) gates, and a multiplexer (44) for selecting the output of one of the gates.

22. An apparatus as claimed in claim 20 or 21, wherein the delay element comprises a variable load.

23. An apparatus as claimed in one of claims 17 to 22, further comprising a
5 determining unit (26') configured to determine the duty cycle variation.

24. An apparatus as claimed in claim 23, wherein the determining unit (26) comprises a low-pass filter (50,52) and a measuring unit configured to measure a dc voltage which represents the duty cycle.

10

25. An apparatus as claimed in one of claims 17 to 24, further comprising a recovery unit configured to recover a clock signal from the received signal.

26. An apparatus as claimed in claim 25, wherein the recovery unit is
15 configured to use the rising or falling edges of the received data, and wherein the apparatus further comprises a selection unit (25) configured to select the rising or falling edges for clock recovery.

27. A data transmission and reception system, comprising:
20 - a transmitter (14,14');
- a receiver (12,12'); and
- a testing apparatus (18,18',20,20',22) as claimed in one of claims 16 to 26.

25 28. A computer program comprising computer program code adapted to perform all of the steps of one of claim 1 to 16 when said program is run on a computer.

29. A computer program as claimed in claim 28 embodied on a computer
30 readable medium

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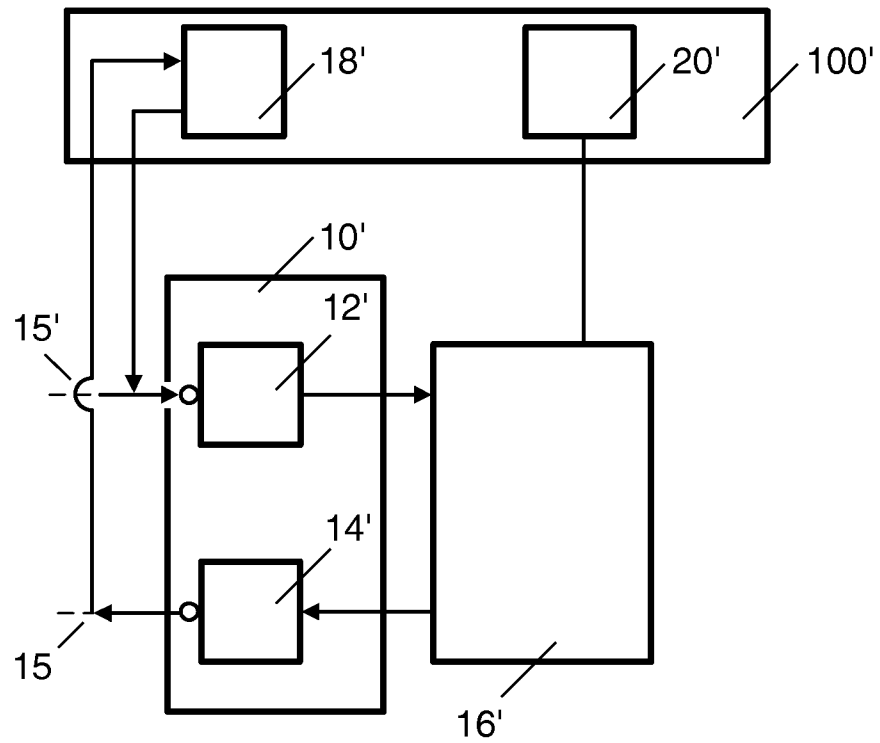


FIG. 1A

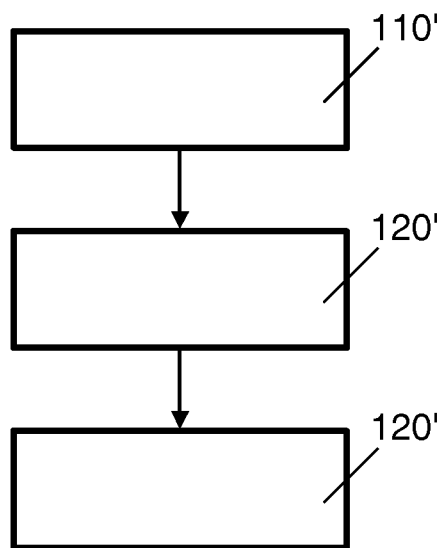


FIG. 1B

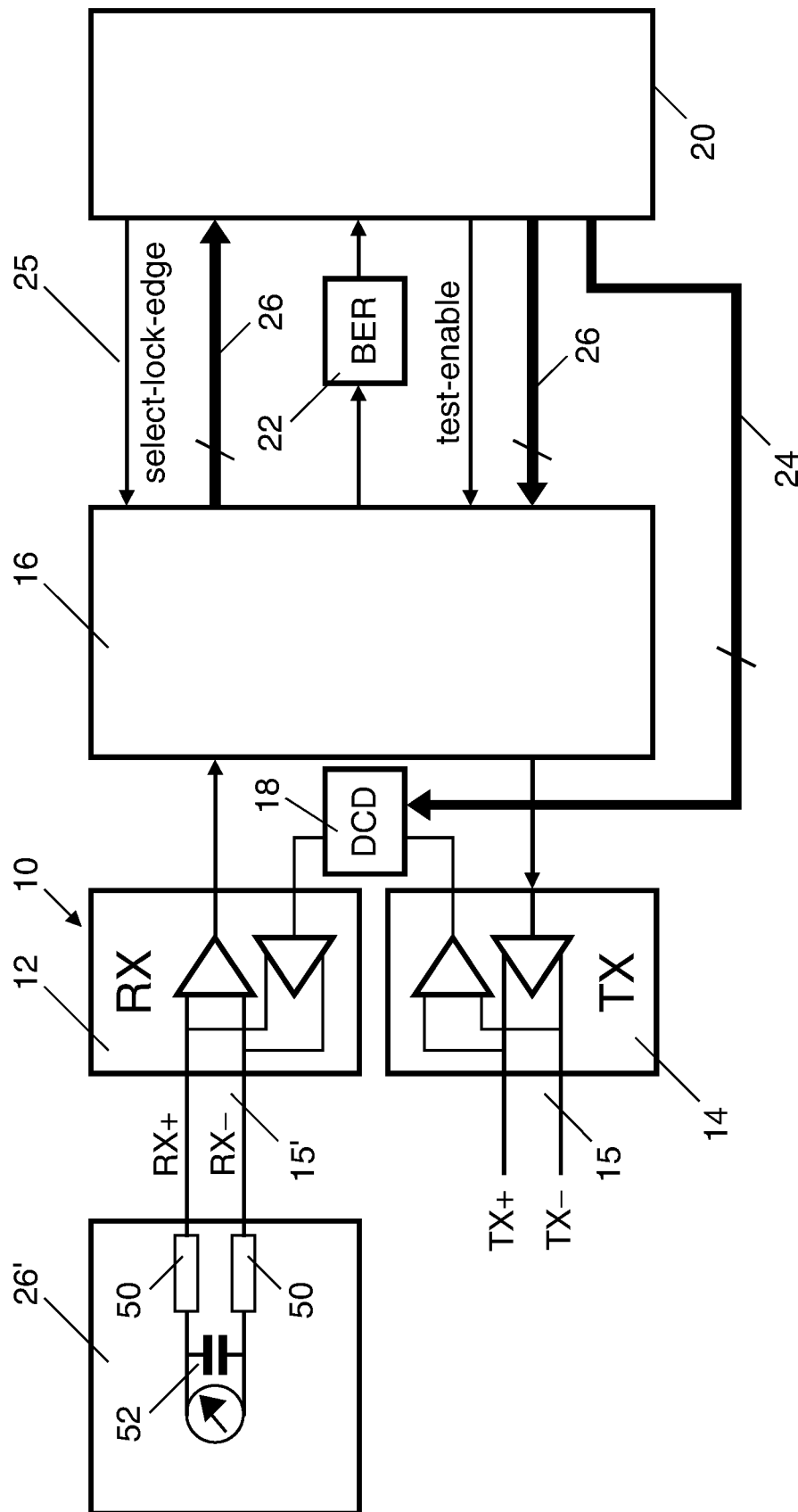


FIG. 1C

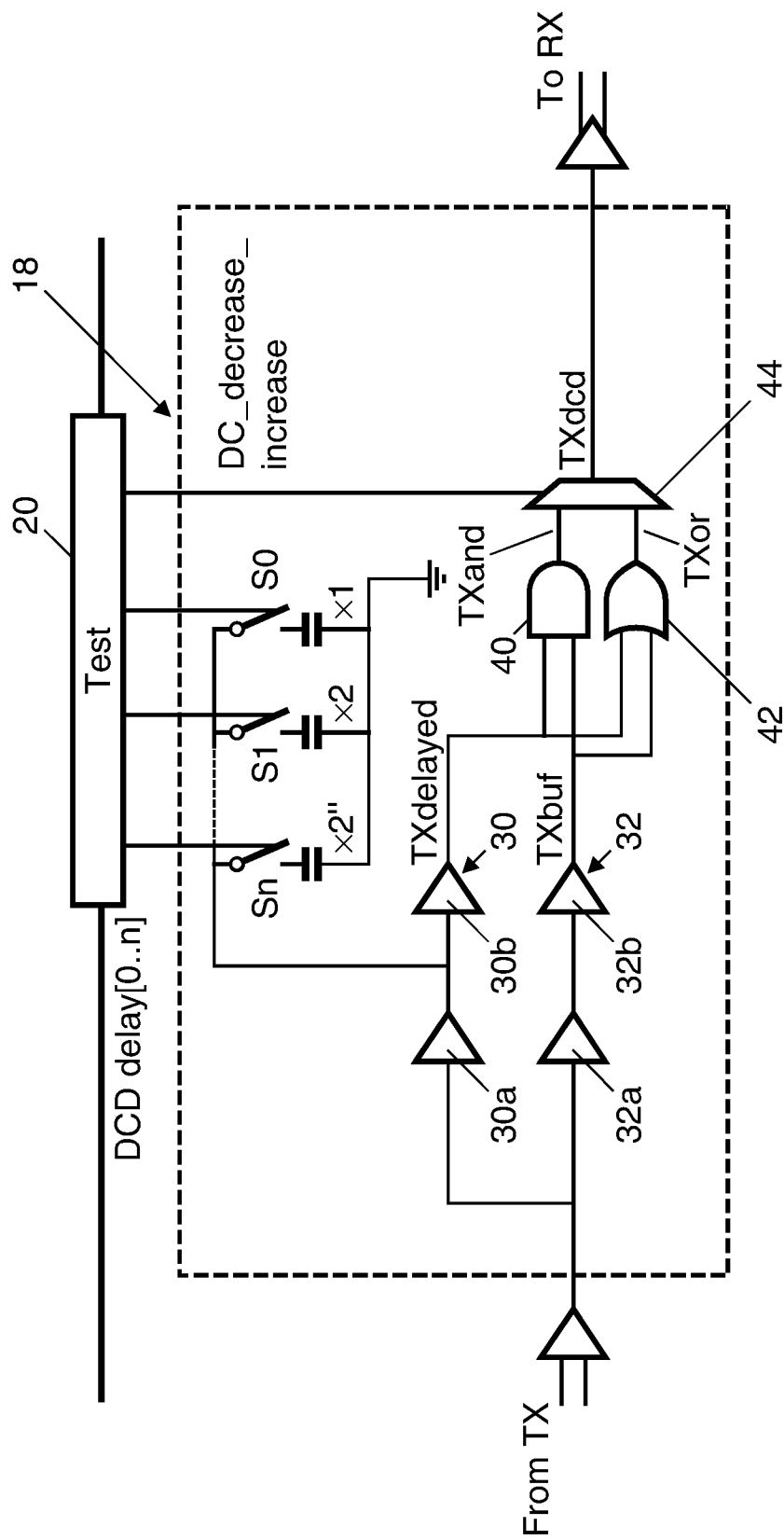


FIG. 2

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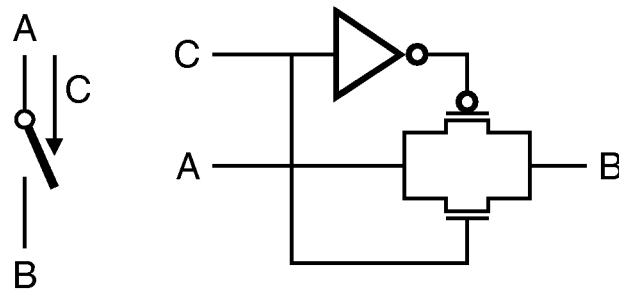


FIG. 3

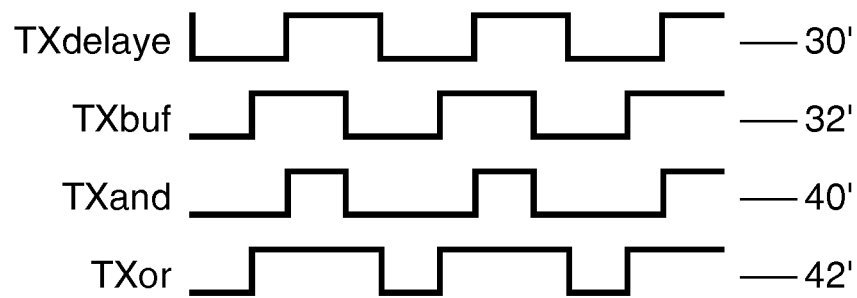


FIG. 4

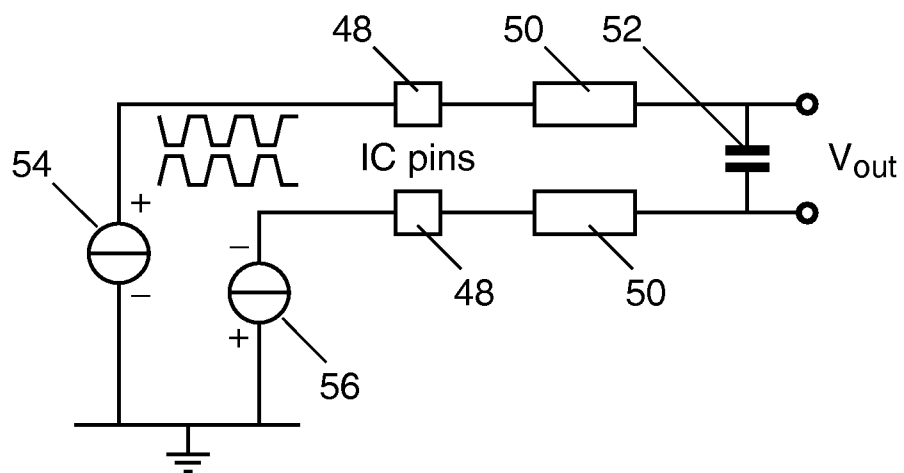


FIG. 5

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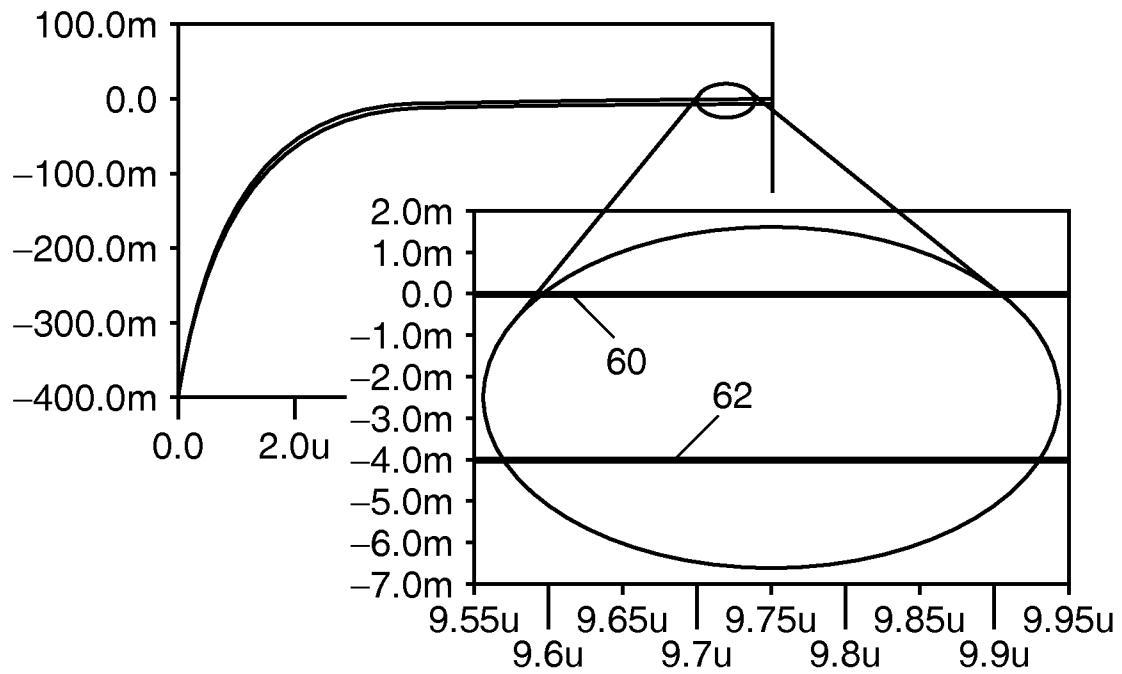


FIG. 6

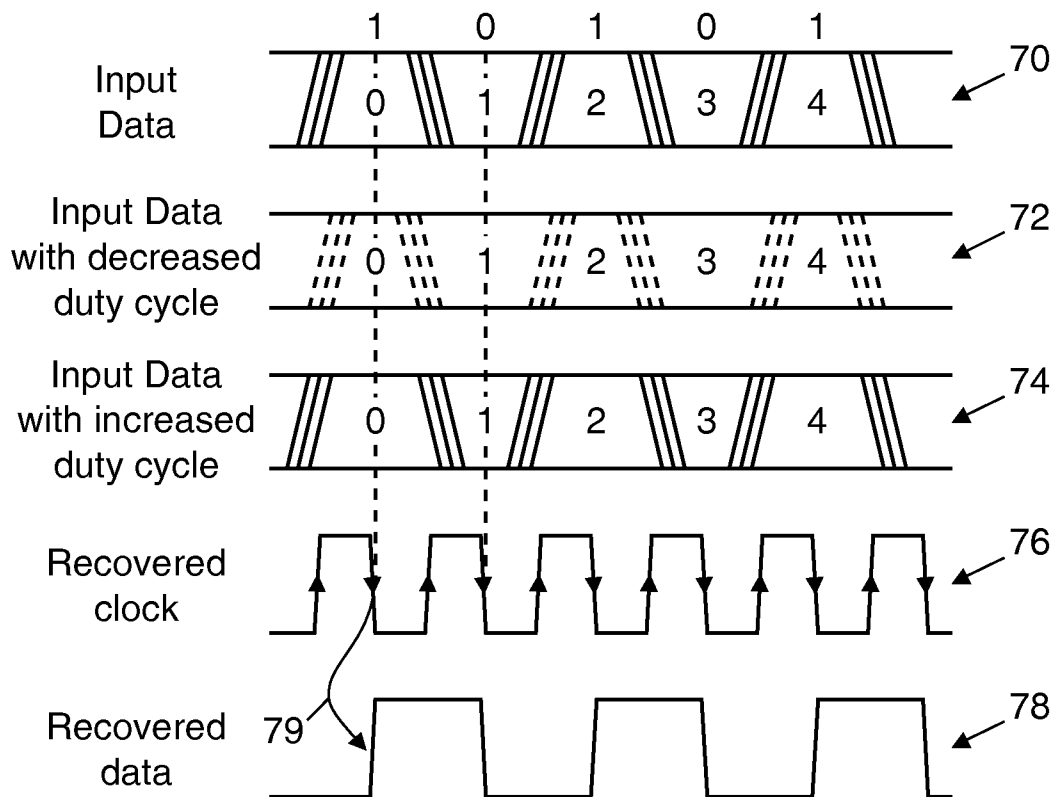


FIG. 7

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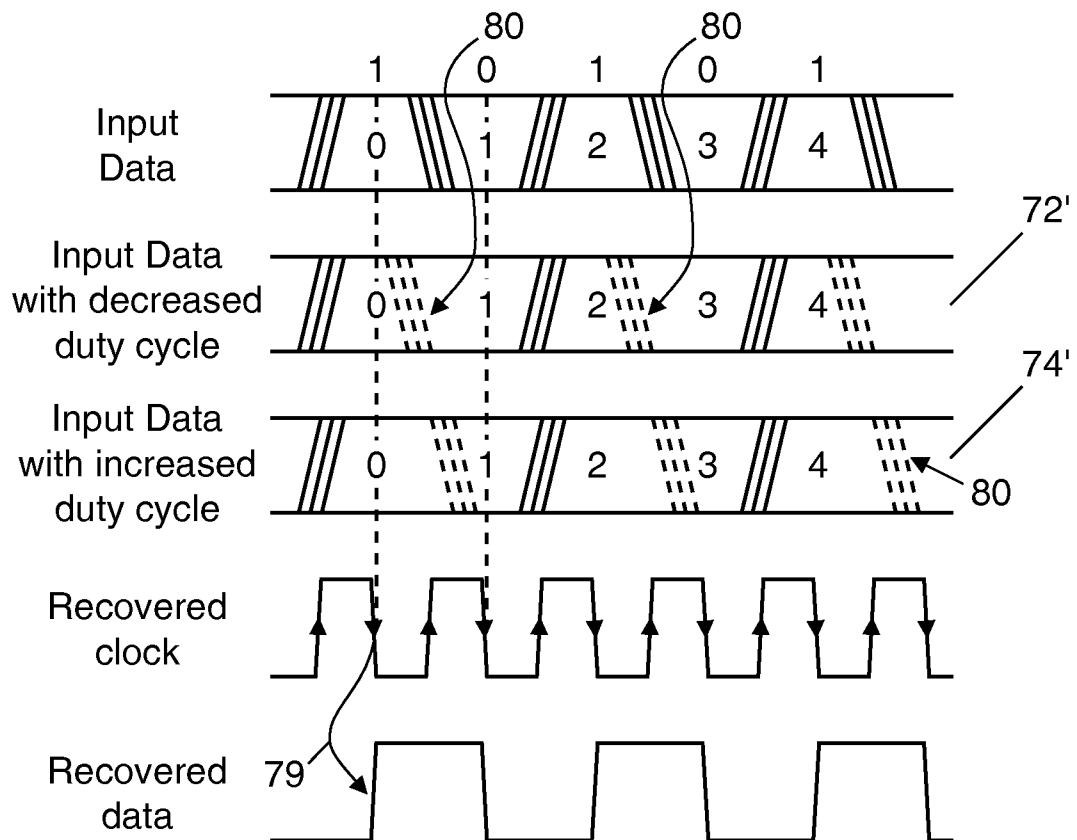


FIG. 8

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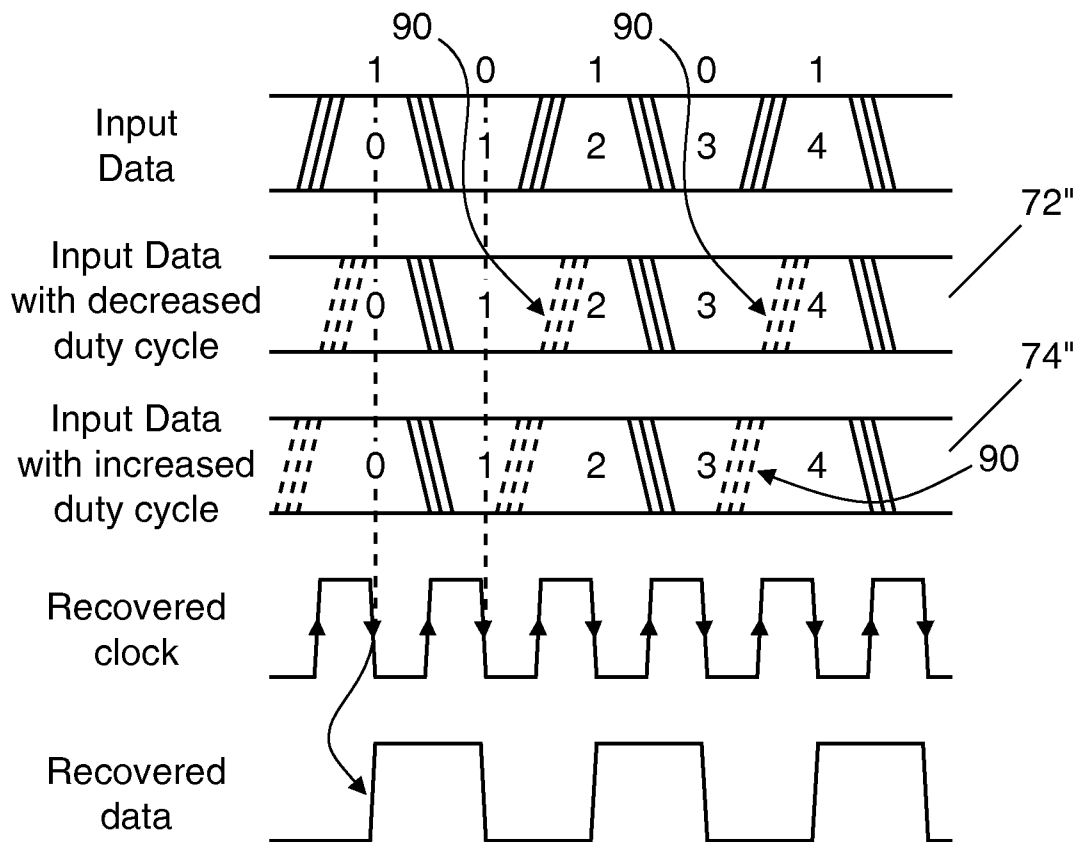


FIG. 9

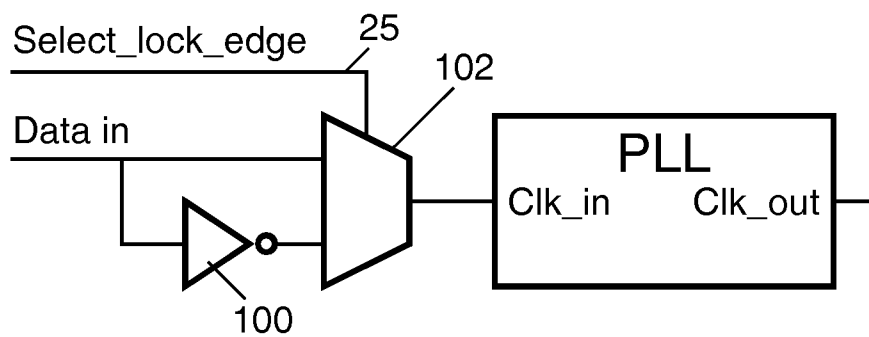


FIG. 10

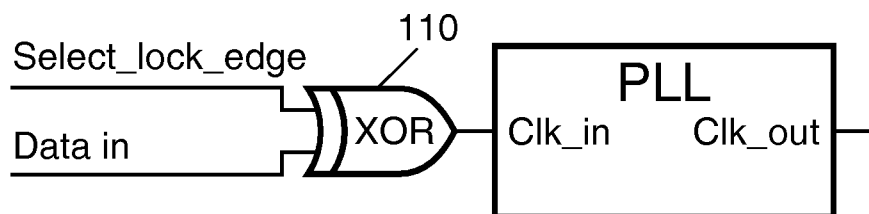


FIG. 11

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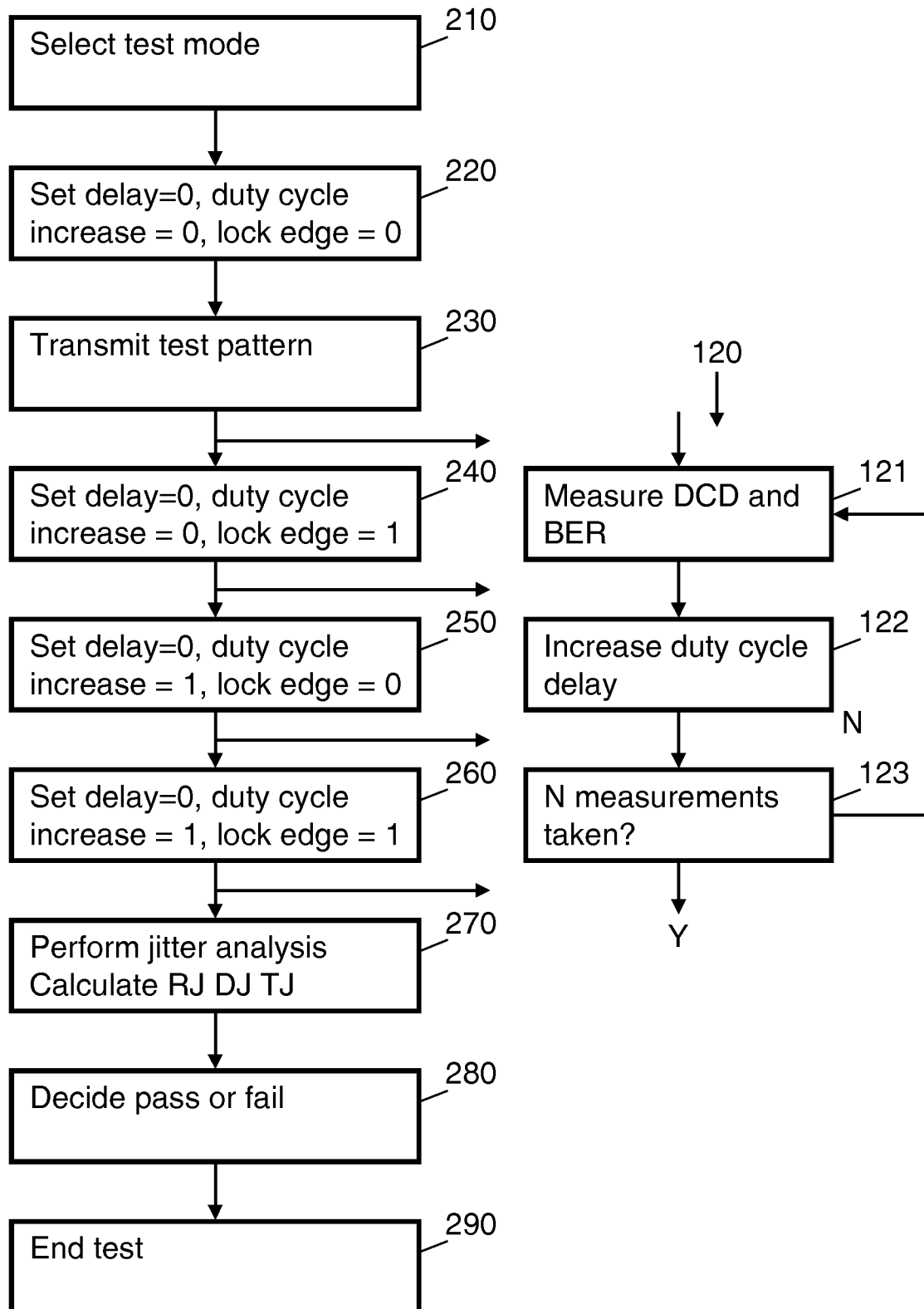


FIG. 12

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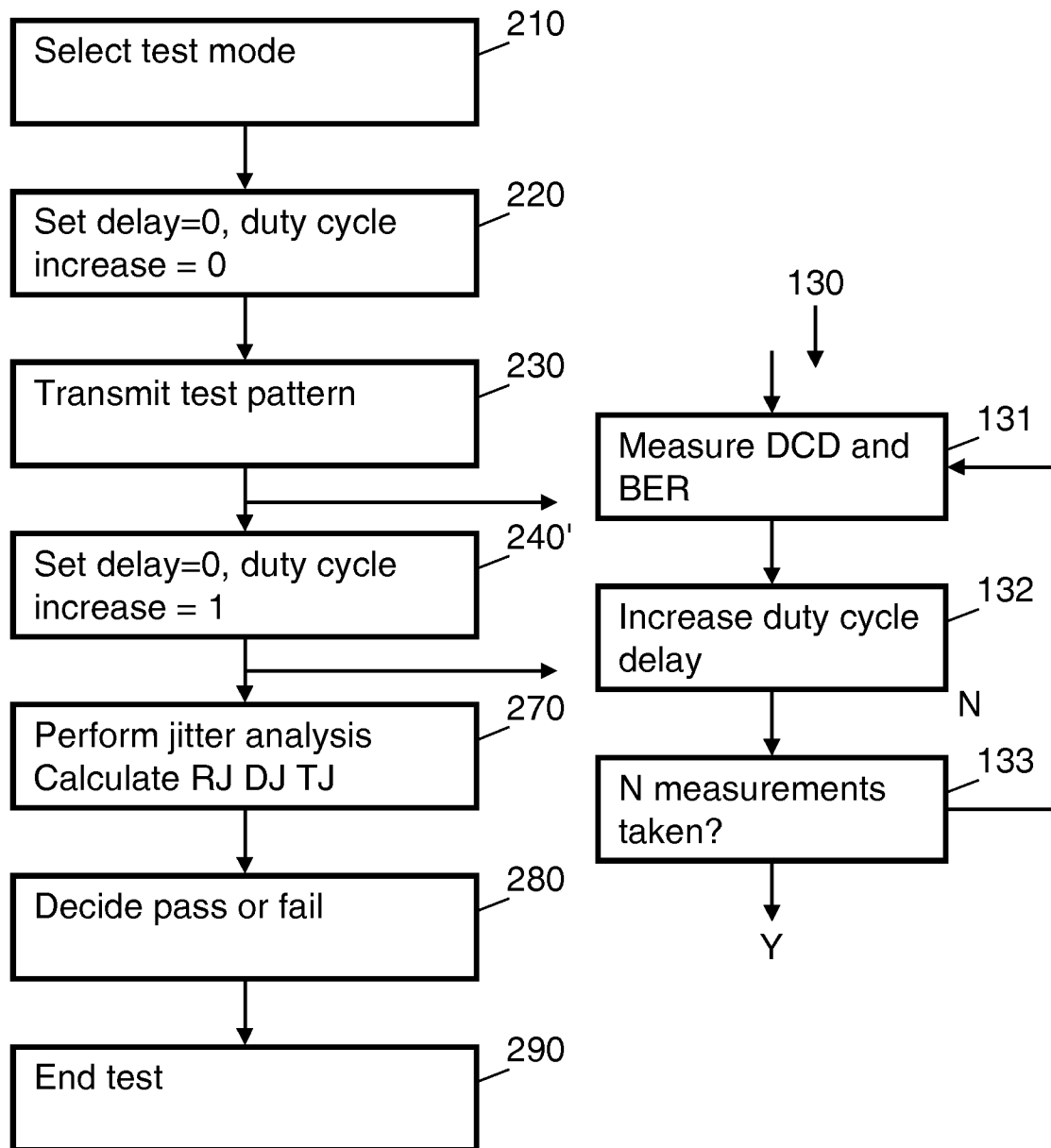


FIG. 13

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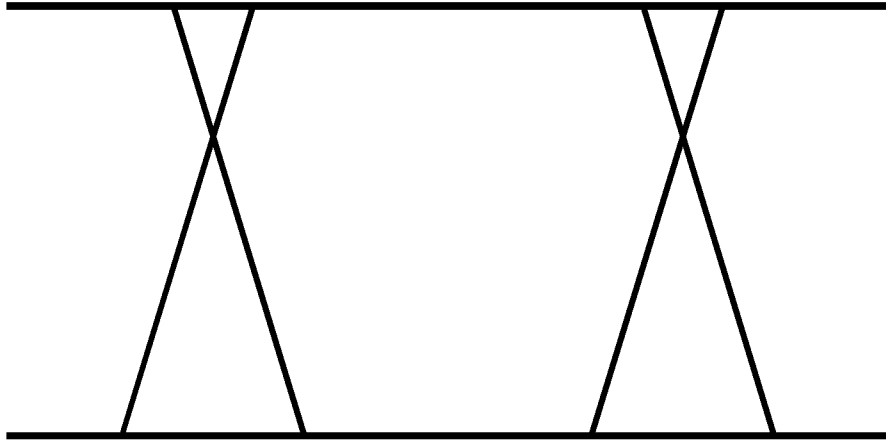


FIG. 14A

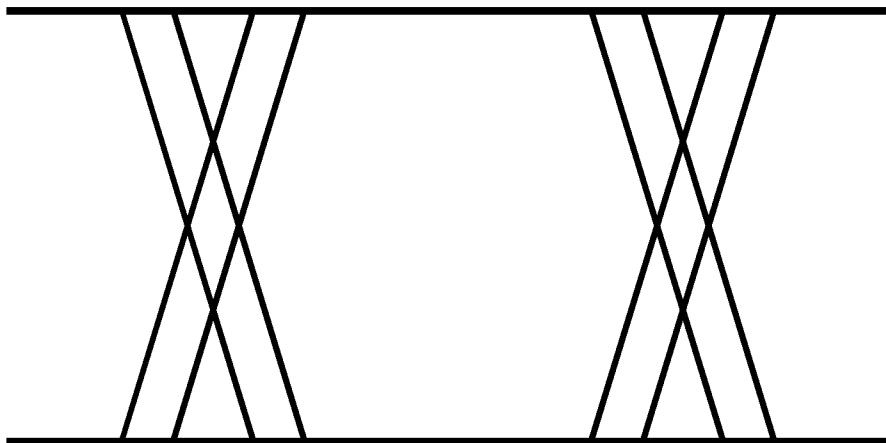


FIG. 14B

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2009/053540

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L1/24 G01R31/317 G01R31/3193

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007/010452 A (KONINKL PHILIPS ELECTRONICS NV [NL]; SCHUTTERT RODGER F [NL]; JOORDENS) 25 January 2007 (2007-01-25) the whole document	1-29



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- *&* document member of the same patent family

Date of the actual completion of the international search

16 November 2009

Date of mailing of the international search report

20/11/2009

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2009/053540

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2007010452 A	25-01-2007	CN 101223726 A	16-07-2008
		JP 2009501480 T	15-01-2009
		US 2009105978 A1	23-04-2009