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- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM,

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- (54) **Title:** MANUFACTURING MEMRISTORS

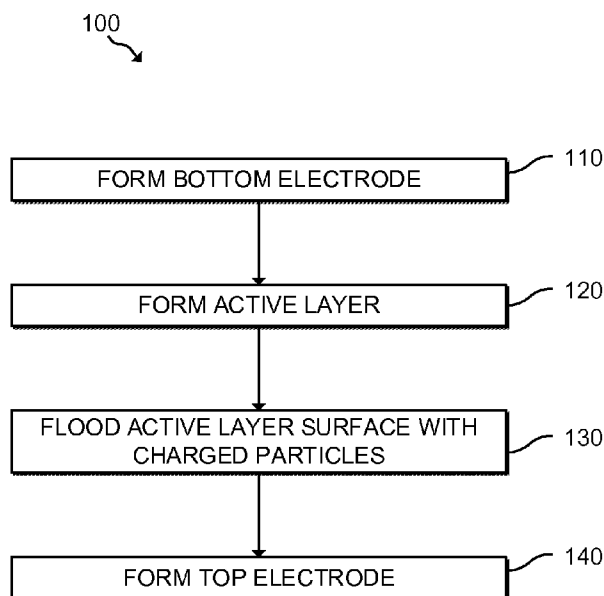


FIG. 1

- (57) **Abstract:** Examples relate to manufacturing memristors. The examples herein form a bottom electrode, form an active layer coupled to the bottom electrode, flood a surface of the active layer with charged particles, and form a top electrode coupled to the active layer. The charged surface of the active region induces formation of a conducting filament through the active layer.

MANUFACTURING MEMRISTORS

BACKGROUND

[0001] Memristors are devices that can be programmed to different resistive states by applying a programming energy, such as a voltage. Large crossbar arrays of memory devices can be used in a variety of applications, including random access memory, non-volatile solid state memory, programmable logic, signal processing control systems, pattern recognition, and other applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The following detailed description references the drawings, wherein:

[0003] FIG. 1 is a flowchart of an example method for manufacturing a memristor;

[0004] FIG. 2 is a flowchart of an example method for manufacturing a memristor including forming a filament formation structure;

[0005] FIG. 3 is a cross-sectional diagram of an example memristor having a conducting filament and a filament formation structure; and

[0006] FIG. 4 is a cross-sectional diagram of an example memristor having multiple conducting filaments and multiple filament formation structures.

DETAILED DESCRIPTION

[0007] Memristors are devices that may be used as components in a wide range of electronic circuits, such as memories, switches, radio frequency circuits, and logic circuits and systems. In a memory structure, a crossbar array of memory devices having memristors may be used. When used as a basis for memory devices, memristors may be used to store a bit of information, such as a 1 or 0. The resistance of a memristor may be changed by applying an electrical stimulus, such as a voltage or a current, through the memristor. Generally, at least one channel may be formed that is capable of being switched between

two states—one in which the channel forms an electrically conductive path (“ON”) and one in which the channel forms a less conductive path (“OFF”). In some other cases, conductive paths represent “OFF” and less conductive paths represent “ON”.

[0008] Memristors may be formed by first depositing and etching necessary physical structures of the memristor, including address lines (typically electrodes) and active regions. After fabrication, memristors may be subject to a formation voltage which may cause the formation of a conducting filament through a typically insulating active region. The filament may be switched between a high resistance state (“HRS”) and a low resistance state (“LRS”) by the application of set and reset voltages, which provides the switching abilities of the memristor.

[0009] The voltage required to form the conducting filament may often times be significantly larger than the set and reset voltages. The formation voltage may be applied using the address lines. The higher voltage needed for formation may affect the area and cost of the addressing circuits. Furthermore, because the formation voltage may be high, the conducting filament formed may draw excessive current in the LRS, leading to inefficient operation. Additionally, in some instances, the filament may be stuck in a particular resistance state due to an excessively high formation voltage.

[0010] Examples disclosed herein provide for manufacturing memristors involving flooding a memristor with charged particles to induce the formation of a conducting filament. In examples, a method for manufacturing a memristor may include forming a bottom electrode, forming an active layer coupled to the bottom electrode, flooding a surface of the active layer with charged particles, and forming a top electrode. The charged surface of the active layer may induce formation of a conducting filament through the active layer.

[0011] By flooding the surface with a finite amount of charged particles, the voltage across the active region may be controlled. In this manner, the current that travels through the conducting filament upon its formation can be controlled. Furthermore, example processes may facilitate the parallel formation of multiple conducting filaments in an active region.

[0012] Referring now to the drawings, FIG. 1 depicts an example method 100 for manufacturing a memristor. Method 100 may include operation 110 for forming a bottom electrode, operation 120 for forming an active layer coupled to the bottom electrode, operation 130 for flooding a surface of the active layer with charged particles, and operation 140 for forming a top electrode coupled to the active layer.

[0013] A memristor may be a device that may be programed to different resistive states by applying a voltage or current. Furthermore, a memristor may “memorize” its last resistance even if the applied voltage or current is removed. In such a manner, a memristor may store digital data. In some examples, a sufficiently high current compliance may be set on the memristors to enable the resistance states of the memristors to be switched in response to the application of a voltage.

[0014] A memristor may be bipolar or unipolar. Bipolar memristors may depend on the polarity of an applied voltage. Specifically, bipolar memristors may be switched from a first state to a second state by application of a voltage of a first polarity, while they may be switched from the second state to the first state by application of a voltage of a second polarity. Unipolar memristors, on the other hand, may depend on the amplitude of an applied voltage.

[0015] In some examples, a memristor may exhibit nonlinear current-voltage (I-V) behavior. For example, linear materials may follow Ohm’s law, where the current through them is proportional to the voltage. On the other hand, the current through a nonlinear memristor may be small at low voltages, while the current increases disproportionately with increasing voltage. As a result, the I-V behavior in a voltage range may be highly nonlinear.

[0016] As described in detail below in reference to FIG. 3 and FIG. 4, a memristor may include a bottom electrode, an active layer, and a top electrode. The bottom electrode and the top electrode may be electrical conductors that, in some implementations, serve as the connection for the memristor to other components. For example, the first and second electrodes may serve as conducting lines in a crossbar array having a plurality of memristors.

[0017] In an operation 110, a bottom electrode may be formed. In some examples, the bottom electrode may be formed on a substrate, such as a semiconductor chip. The bottom electrode may be formed using a variety of techniques, including ion beam assisted deposition, sputtering, atomic layer deposition, evaporation, and chemical vapor deposition. Non-limiting example materials for the bottom electrode include Pt, Ta, Hf, Zr, Al, Co, Ni, Fe, Nb, Mo, W, Cu, Ti, TiN, TaN, Ta₂N, WN₂, NbN, MoN, TiSi₂, TiSi, Ti₅Si₃, TaSi₂, WSi₂, NbSi₂, V₃Si, electrically doped polycrystalline Si, electrically doped polycrystalline Ge, and combinations thereof.

[0018] In an operation 120, an active layer may be formed. The active layer may be coupled to the bottom electrode. As used herein, components may be coupled by forming an electrical connection between the components. For example, the active layer may be coupled to the bottom electrode by forming a direct, surface contact between the two. The active layer may be formed using a variety of techniques, including ion beam assisted deposition, sputtering, atomic layer deposition, evaporation, and chemical vapor deposition.

[0019] The active layer may be the active region within the memristor that provides the memristive properties. The active layer may include an electrically insulating material. In some examples the memristor may be nitride-based, meaning that at least a portion of the memristor is formed from a nitride-containing composition. The memristor may also be oxide-based, meaning that at least a portion of the memristor is formed from an oxide-containing material. Furthermore, the memristor may be oxy-nitride based, meaning that at least a portion of the memristor is formed from an oxide-containing material and that at least a portion of the memristor is formed from a nitride-containing material. Example materials of the memristor may include tantalum oxide, hafnium oxide, titanium oxide, yttrium oxide, niobium oxide, zirconium oxide, or other like oxides, or non-transition metal oxides, such as aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, silicon nitride, and oxynitrides such as silicon oxynitride. In addition, other functioning memristors may be employed in the practice of the teachings herein.

[0020] In an operation 130, a surface of the active layer may be flooded with charged particles. The charged particles may induce formation of a conducting filament through the active layer. For example, charged particles may be placed on the surface of the active layer so that the surface of the active layer is covered with charged particles. In some examples, an electrical capacitance may be induced between the bottom electrode and the charged surface. This potential may cause the formation of at least one conducting filament in the active layer. For example, the charge may promote the movement of charge carriers within the active layer which may form the conducting filament.

[0021] In some examples, the charged particles may include electrons. For example, electrons may be provided by an electron flood gun, which may directly place electrons onto the surface of the active layer. In addition or as an alternative, the charged particles may include ions. For example, air may be blown past a charged electrode, such as a wire. The charged wire may create ions which are blown onto the surface of the active layer. The ions may flood the surface and provide the charge to induce formation of the conducting filament.

[0022] The conducting filament may be a region in the active layer that is electrically conducting. The conducting filament may be the component that provides the memristor its properties. For example, the memristor may be in a low resistance state when the filament connects the top electrode and the bottom electrode through the active layer. When the filament is broken, and therefore not connecting the electrodes, the memristor may be in a high resistance state. The conducting filament may be connected or broken by the application of a write voltage or current, which may be applied during the writing of the memristor. In some examples, multiple conducting filaments may be formed in the active layer.

[0023] In an operation 140, a top electrode may be formed, where the top electrode is coupled to the active layer. The top electrode may be formed using a variety of techniques, including ion beam assisted deposition, sputtering, atomic layer deposition, evaporation, and chemical vapor deposition. Non-limiting example materials for the top electrode include Pt, Ta, Hf, Zr, Al, Co, Ni, Fe, Nb, Mo, W, Cu, Ti, TiN, TaN, Ta₂N, WN₂, NbN, MoN, TiSi₂, TiSi, Ti₅Si₃, TaSi₂, WSi₂, NbSi₂, V₃Si, electrically doped polycrystalline Si, electrically doped

polycrystalline Ge, and combinations thereof. In some examples, the top electrode and the bottom electrode may serve as conducting lines for the memristor in a crossbar array.

[0024] In some examples, a top electrode may be formed prior to flooding the active layer with charged particles. In such instances, the charged particles may be placed on the surface of the top electrode. Because the top electrode is conducting, the charged particles may cause an electrical potential difference that induces the formation of the conducting filament.

[0025] In some examples, the top electrode may be formed under temperature control so that the conducting filament is not annealed. If annealed, the conducting filament may be reformed using the examples processes described herein.

[0026] FIG. 2 depicts an example method 200 for manufacturing a memristor including forming a filament formation structure. Method 200 may include operation 210 for forming a bottom electrode, operation 220 for forming an active layer coupled to the bottom electrode, operation 230 for forming a filament formation structure, operation 240 for forming a top electrode coupled to the active layer, operation 250 for flooding the top electrode with charged particles, and operation 260 for stopping the flooding of the top electrode.

[0027] In an operation 210, a bottom electrode may be formed. Operation 210 may be analogous to operation 110 of FIG. 1. In an operation 220, an active layer may be formed that is coupled to the bottom electrode. Operation 220 may be analogous to operation 120 of FIG. 1.

[0028] In an operation 230, a filament formation structure may be formed on the surface of the active layer. The filament formation structure may be coupled to the surface of the active layer. The filament formation structure may be an electrically conducting region or layer that directs the formation of the conducting filament. In some examples, the filament formation structure may be an electrode that is more conducting than the active layer. Accordingly, the filament formation structure may cause a greater electrical potential difference to be formed between the bottom electrode and regions of the surface of the active layer that is coupled to the filament formation structure.

[0029] Specifically, the surface of the active layer may be flooded with charged particles in an operation 240, which may be analogous to operation 130 of FIG. 1. The charged particles, which may be electrons or ions, may flood the surface of the active layer. Because the filament formation structure is more electrically conducting than the active layer, the electrical potential difference may be greater across the regions of the active layer that is directly in series with the bottom electrode and the filament formation structure. As a result, the formation of the conducting filament may be favored in the region of the active layer between the bottom electrode and the filament formation structure.

[0030] When the surface of the active layer has been flooded with an amount of charged particles that is adequate for inducing the formation of the conducting filament, the flooding of the active layer may be stopped in an operation 250. Stopping the flooding of the active surface may allow greater control over the filament formation. By allowing an amount of charge to be placed on the active layer that induces the formation of the conducting filament, but not an amount that is excessively high, the current that will pass through the conducting filament following formation may not be large enough to cause potential issues.

[0031] In an operation 260, the top electrode may be formed. Operation 260 may be analogous to operation 140 of FIG. 1.

[0032] FIG. 3 depicts an example memristor 300 having a conducting filament 325 and a filament formation structure 340. Memristor 300 may include a bottom electrode 310, an active layer 320 coupled to bottom electrode 310, a filament formation structure 340 coupled to at least a portion of a surface of active layer 320, and a top electrode 330 coupled to the surface of active layer 320 and to filament formation structure 340.

[0033] In some examples, bottom electrode 310 may be formed on a substrate, such as a semiconductor chip. Bottom electrode 310 may be formed using a variety of techniques, including ion beam assisted deposition, sputtering, atomic layer deposition, evaporation, and chemical vapor deposition. Non-limiting example materials for bottom electrode 310 include Pt, Ta, Hf, Zr, Al, Co, Ni, Fe, Nb, Mo, W, Cu, Ti, TiN, TaN, Ta₂N, WN₂, NbN, MoN, TiSi₂, TiSi, Ti₅Si₃, TaSi₂, WSi₂, NbSi₂, V₃Si, electrically doped polycrystalline Si, electrically doped polycrystalline Ge, and combinations thereof.

[0034] Active layer 320 may be coupled to bottom electrode 310. Active layer 320 may include an electrically insulating material, such as a metal oxide or metal nitride. Active layer 320 may have a conducting filament 325. Conducting filament 325 may be formed or broken when memristor 300 is switched. For example, memristor 300 may be in a low resistance state when filament 325 is connected through the active layer 320. When filament 325 is broken, memristor 320 may be in a high resistance state. Conducting filament 325 may be formed by processes described herein.

[0035] Filament formation structure 340 may be an electrically conducting region or layer that directs the formation of conducting filament 325. Filament formation structure 340 may be an electrode that is more conducting than active layer 320. Filament formation structure 340 may direct the conducting filament 325 to be formed between bottom electrode 310 and filament formation structure 340. Non-limiting example materials for filament formation structure 340 include Pt, Ta, Hf, Zr, Al, Co, Ni, Fe, Nb, Mo, W, Cu, Ti, TiN, TaN, Ta₂N, WN₂, NbN, MoN, TiSi₂, TiSi, Ti₅Si₃, TaSi₂, WSi₂, NbSi₂, V₃Si, electrically doped polycrystalline Si, electrically doped polycrystalline Ge, and combinations thereof.

[0036] Top electrode 330 may be coupled to active layer 320 and filament formation structure 340. Top electrode 330 and bottom electrode 310 may serve as connecting lines to a crossbar array of memristors. For example, memristor 300 may be one of a plurality of memristors in a crossbar array, such as a memory array. Non-limiting example materials for top electrode 330 include Pt, Ta, Hf, Zr, Al, Co, Ni, Fe, Nb, Mo, W, Cu, Ti, TiN, TaN, Ta₂N, WN₂, NbN, MoN, TiSi₂, TiSi, Ti₅Si₃, TaSi₂, WSi₂, NbSi₂, V₃Si, electrically doped polycrystalline Si, electrically doped polycrystalline Ge, and combinations thereof.

[0037] FIG. 4 depicts an example memristor 400 having multiple conducting filaments 425 and multiple filament formation structures 440. Memristor 400 may be depicted in FIG. 4 in an example form during manufacturing. For example, memristor 400 is shown to be lacking a top electrode but including a plurality of charged particles 450 that have been flooded onto the surface of an active layer 420.

[0038] Memristor 400 may include a bottom electrode 410, active layer 420 having a plurality of conducting filaments 425, a plurality of filament formation structures 440, and a plurality of charged particles 450. The placement of filament structures 440 on active layer

420 induces formation of the conducting filaments 425 in the regions of active layer 320 that is directly between the conducting filaments 425 and the bottom electrode 410. When connected to a crossbar array, each conducting filament 425 may be addressed individually. Accordingly, examples disclosed herein may provide for effective manufacture of a crossbar array of a plurality of memristors.

[0039] The foregoing describes a number of examples for manufacturing memristors. It should be understood that the memristors and processes described herein may include additional components or steps and that some of the components or steps described herein may be removed or modified without departing from the scope of the memristors and processes. It should also be understood that the components depicted in the figures are not drawn to scale, and thus, the components may have different relative sizes with respect to each other than as shown in the figures.

[0040] It should be noted that, as used in this application and the appended claims, the singular forms “a,” “an,” and “the” include plural elements unless the context clearly dictates otherwise.

CLAIMS

What is claimed is:

1. A method for manufacturing a memristor, comprising:
forming a bottom electrode;
forming an active layer coupled to the bottom electrode, wherein the active layer comprises an electrically insulating material;
flooding a surface of the active layer with charged particles, wherein the charged surface induces formation of a conducting filament through the active layer; and
forming a top electrode coupled to the active layer.
2. The method of claim 1, wherein the charged particles comprises electrons.
3. The method of claim 1, wherein the charged particles comprises ions.
4. The method of claim 1, wherein forming the top electrode is formed before flooding the surface of the active layer with charged particles.
5. The method of claim 1, further comprising flooding the surface with charged particles to place a sufficient charge on the surface to induce the formation of the conducting filament.
6. The method of claim 5, further comprising stopping the flooding of the surface of the active layer in response to a sufficient charge being placed on the surface to induce the formation of the conducting filament.
7. The method of claim 1, further comprising forming at least one filament formation structure coupled to the surface of the active layer before flooding the surface of the active layer with charged particles.

8. A method for manufacturing a memristor, comprising:
 - forming a bottom electrode;
 - forming an active layer coupled to the bottom electrode, wherein the active layer comprises an electrically insulating material;
 - forming at least one filament formation structure coupled to the active layer;
 - forming a top electrode coupled to the active layer;
 - flooding a surface of the top electrode with charged particles to place a sufficient charge on the surface to induce formation of a conducting filament through the active layer that connects the bottom electrode and the filament formation structure.
9. The method of claim 8, wherein the charged particles comprises at least one of electrons and ions.
10. The method of claim 8, further comprising stopping the flooding of the surface of the top electrode in response to a sufficient charge being placed on the surface to induce the formation of the conducting filament.
11. A memristor, comprising:
 - a bottom electrode;
 - a top electrode;
 - an active layer coupled between the bottom electrode and the top electrode, wherein the active layer comprises an electrically insulating material and an electrically conducting filament through the active layer; and
 - at least one filament formation structure coupled between the active layer and the top electrode, wherein the conducting filament of the active layer connects the bottom electrode with the filament formation structure.
12. The memristor of claim 11, further comprising a plurality of charged particles, wherein the charged particles induces the formation of the electrically conducting filament.

13. The memristor of claim 12, wherein the charged particles comprises at least one of electrons and ions.
14. The memristor of claim 11, further comprising a plurality of filament formation structures, wherein the active layer comprises a plurality of electrically conducting filaments that connect the bottom electrode and the filament formation structures.
15. The memristor of claim 10, wherein the active layer comprises a metal oxide.

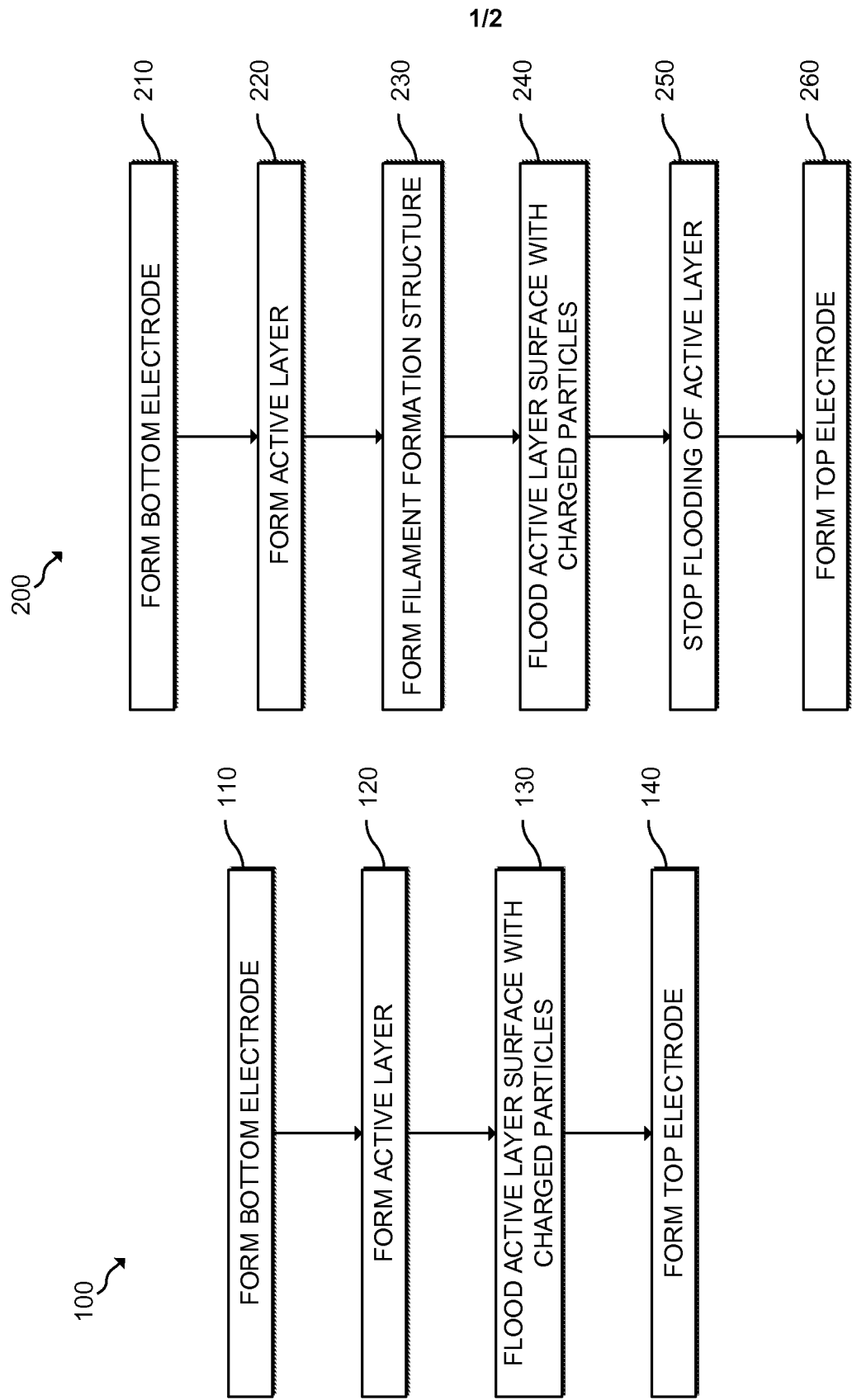


FIG. 1

FIG. 2

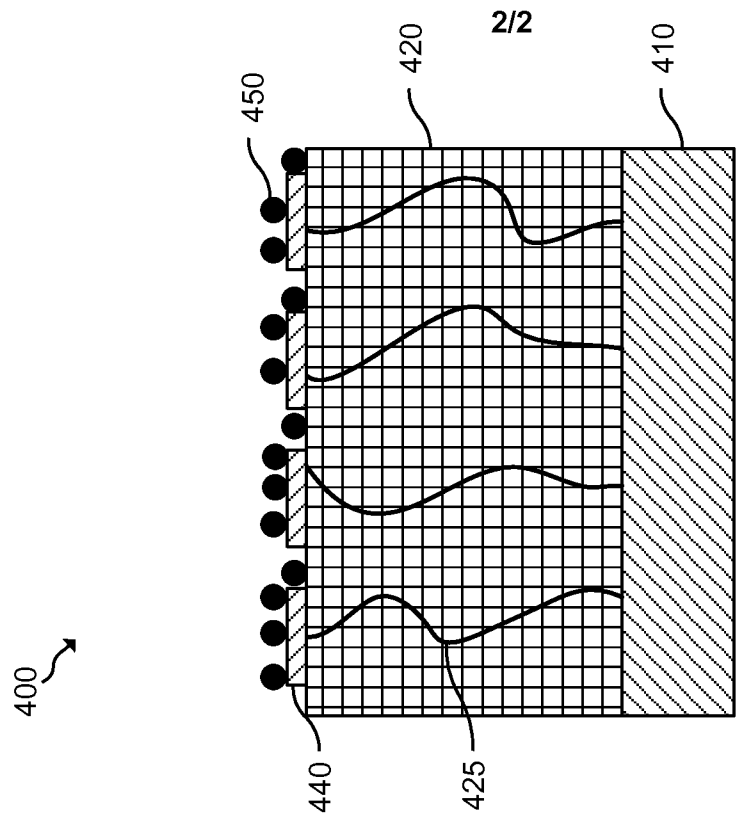


FIG. 3

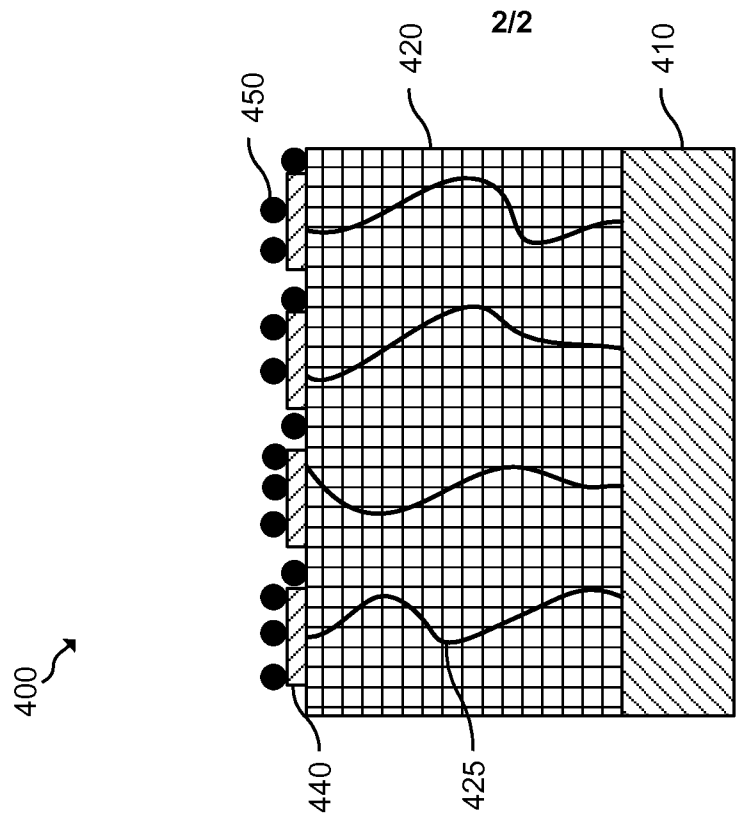


FIG. 4

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/8247(2006.01)i, H01L 27/115(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/8247; G11C 11/02; H01L 45/00; H01L 29/68; H01L 27/10; H01L 21/44; H01L 27/115

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: memristor, filament, charge, flood

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0019219 A1 (YU-JIN LEE) 28 January 2010 See abstract, paragraphs [0015]-[0019] and figure 1B.	11, 14-15
A		1-10, 12-13
A	WO 2007-105284 A1 (FUJITSU LIMITED) 20 September 2007 See abstract, paragraphs [0071]-[0130] and figures 5-9.	1-15
A	US 2013-0299763 A1 (JI-WON MOON et al.) 14 November 2013 See abstract, paragraphs [0036]-[0043] and figures 3A-3C.	1-15
A	WO 2014-194069 A2 (SHIH-YUAN WANG et al.) 04 December 2014 See abstract, paragraphs [0076]-[0087] and figures 12A-15B.	1-15
A	US 2013-0228734 A1 (SEAGATE TECHNOLOGY LLC.) 05 September 2013 See abstract, paragraphs [0026]-[0038] and figures 1-3B.	1-15
** NOTE: This International Search Report has been established on the assumption that claim 15 refers to claim 11.		



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 December 2015 (21.12.2015)

Date of mailing of the international search report

21 December 2015 (21.12.2015)

Name and mailing address of the ISA/KR

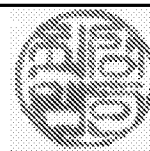
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/023270

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