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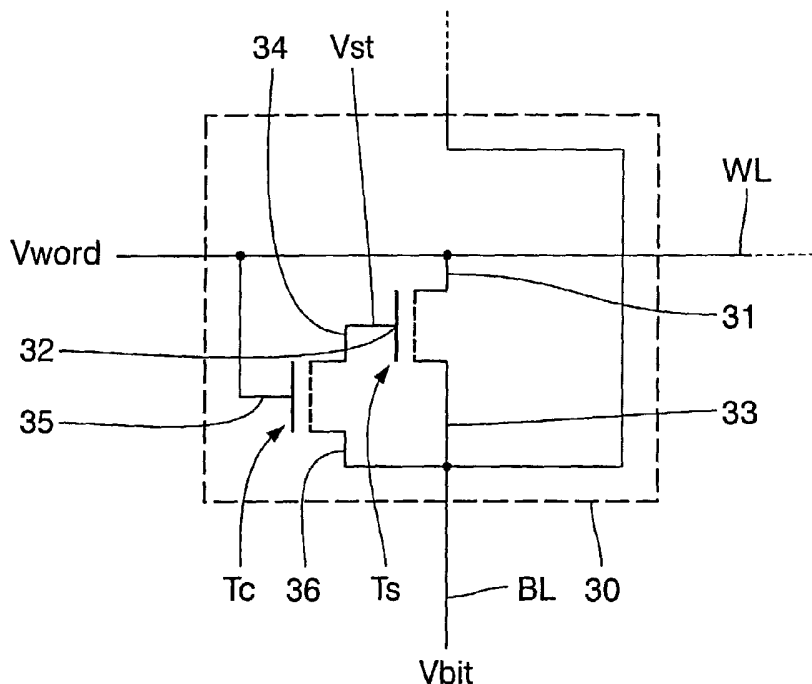
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(54) Title: MEMORY ARRAY HAVING 2T MEMORY CELLS



(57) Abstract: The present invention relates to a memory array having a plurality of memory cells. In order to combine the compactness of DRAM with the speed and uncomplicated processing profits of SRAM the present invention proposes a memory array having a plurality of memory cells each comprising: - a storage transistor having a drain coupled to a word-line of said array, a source coupled to a bit-line of said array and a gate, and - a control transistor having a drain coupled to the gate of said storage transistor, a source coupled to said bit-line and a gate coupled to said word-line.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

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 IPC 7 G11C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 943 270 A (BORKAR SHEKHAR YESHWANT) 24 August 1999 (1999-08-24) column 3, line 61-67; figure 2 ---	1
A	US 5 995 410 A (FORBES LEONARD) 30 November 1999 (1999-11-30) figure 2 ---	1
A	US 5 066 607 A (BANERJEE SANJAY K) 19 November 1991 (1991-11-19) figure 1 -----	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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US 5995410	A	30-11-1999	US 5835403 A	10-11-1998
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