



- (51) International Patent Classification:
GI1C 11/15 (2006.01) *H01L 27/115* (2006.01)
- (21) International Application Number:
PCT/US2015/024444
- (22) International Filing Date:
6 April 2015 (06.04.2015)
- (25) Filing Language: English
- (26) Publication Language: English
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to the identity of the inventor (Rule 4.17(i))

[Continued on next page]

- (54) Title: ELECTRICALLY CONDUCTING OXYGEN DIFFUSION BARRIERS FOR MEMRISTORS AND SELECTORS

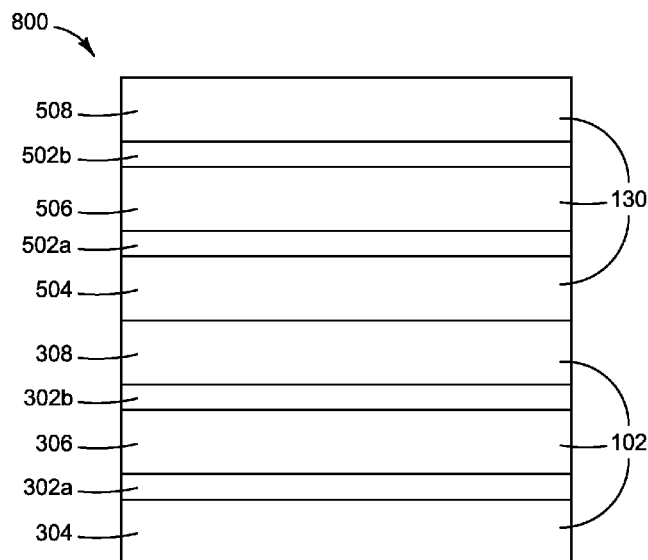


FIG. 8

(57) Abstract: A memory cell includes either a nonvolatile resistance memory device or a non-volatile memory device in series with a selector. The nonvolatile resistance memory device includes a dielectric layer sandwiched between a first bottom electrode and a first top electrode. The selector includes a selector insulator layer sandwiched between a second bottom electrode and a second top electrode. Either or both of the nonvolatile resistance memory device and selector include an electrically conducting oxygen diffusion barrier layer between one of the electrodes and the dielectric layer or selector insulator layer, respectively.



— *as to applicant's entitlement to apply for and be granted
a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

ELECTRICALLY CONDUCTING OXYGEN DIFFUSION BARRIERS FOR MEMRISTORS AND SELECTORS

BACKGROUND

[0001] Non-volatile memory is computer memory that can get back stored information even when not powered. Types of non-volatile memory may include resistive RAM (random access memory) (RRAM or ReRAM), phase change RAM (PCRAM), conductive bridge RAM (CBRAM), ferroelectric RAM (F-RAM), etc.

[0002] Resistance memory elements, such as resistive RAM, or ReRAM, can be programmed to different resistance states by applying programming energy. After programming, the state of the resistive memory elements can be read and remains stable over a specified time period. Large arrays of resistive memory elements can be used to create a variety of resistive memory devices, including non-volatile solid state memory, programmable logic, signal processing, control systems, pattern recognition devices, and other applications. Examples of resistive memory devices include valence change memory and electrochemical metalization memory, both of which involve ionic motion during electrical switching and belong to the category of memristors.

[0003] Memristors are devices that can be programmed to different resistive states by applying a programming energy, for example, a voltage or current pulse. This energy generates a combination of electric field and thermal effects that can modulate the conductivity of both non-volatile switch and non-linear select functions in a memristive element. After programming, the state of the memristor can be read and remains stable over a specified time period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A-1B depict, in perspective, a memristor crossbar and a selector-memristor crossbar, respectively, according to an example.

[0005] FIG. 2 depicts a half V scheme with selector, according to an example.

[0006] FIG. 3 depicts a cross-sectional view of a memristor multilayer structure with an oxygen diffusion barrier at the bottom electrode – memristive switch interface, according to an example.

[0007] FIG. 4 depicts a cross-sectional view of a memristor multilayer structure with oxygen diffusion barriers at both bottom electrode - memristive switch interface and top electrode - memristive switch interfaces, according to an example.

[0008] FIG. 5 depicts a cross-sectional view of a selector multilayer structure with an oxygen diffusion barrier at the bottom electrode – selector interface, according to an example.

[0009] FIG. 6 depicts a cross-sectional view of a selector multilayer structure with an oxygen diffusion barrier at the top electrode – selector interface, according to an example.

[0010] FIG. 7 depicts a cross-sectional view of a selector multilayer structure with oxygen diffusion barriers at both bottom electrode - selector switch interface and top electrode – memristive switch interfaces, according to an example.

[0011] FIG. 8 depicts a cross-sectional view of a combination memristor-selector multilayer structure with oxygen diffusion barriers denoted in phantom at various locations in the structure, showing different possible placement locations, according to an example.

DETAILED DESCRIPTION

[0012] It is appreciated that, in the following description, numerous specific details are set forth to provide a thorough understanding of the examples. However, it is appreciated that the examples may be practiced without limitation to these specific details. In other instances, well-known methods and structures may not be described in detail to avoid unnecessarily obscuring the description of the examples. Also, the examples may be used in combination with each other.

[0013] While a limited number of examples have been disclosed, it should be understood that there are numerous modifications and variations therefrom. Similar or equal elements in the Figures may be indicated using the same numeral.

[0014] It is to be noted that, as used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise.

[0015] As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint, and may be related to manufacturing tolerances. The degree of flexibility of this term can be dictated by the particular variable and would be within the knowledge of those skilled in the art to determine based on experience and the associated description herein. In some examples, "about" may refer to a difference of $\pm 10\%$.

[0016] Memristors are nano-scale devices that may be used as a component in a wide range of electronic circuits, such as memories, switches, radio frequency circuits, and logic circuits and systems. In a memory structure, a crossbar array of memristor devices may be used. When used as a basis for memories, memristors may be used to store bits of information, 1 or 0. When used as a logic circuit, a memristor may be employed as configuration bits and switches in a logic circuit

that resembles a Field Programmable Gate Array, or may be the basis for a wired-logic Programmable Logic Array. It is also possible to use memristors capable of multi-state or analog behavior for these and other applications. While specific examples to memristors are provided herein, it is appreciated that many other types of non-volatile memory may beneficially employ the teachings herein. Examples of such other types of non-volatile memory may include resistive RAM (random access memory) (RRAM or ReRAM), phase change RAM (PCRAM), conductive bridge RAM (CBRAM), ferroelectric RAM (F-RAM), etc.

[0017] The resistance of a memristor may be changed by applying a voltage across or a current through the memristor. Generally, at least one channel may be formed that is capable of being switched between two states—one in which the channel forms an electrically conductive path (“ON”) and one in which the channel forms a less conductive path (“OFF”). In some cases, conducting channels may be formed by ions and/or vacancies. Some memristors exhibit bipolar switching, where applying a voltage of one polarity may switch the state of the memristor and where applying a voltage of the opposite polarity may switch back to the original state. Alternatively, memristors may exhibit unipolar switching, where switching is performed, for example, by applying different voltages of the same polarity.

[0018] When used as a switch, the memristor may either be in a low resistance (ON) or high resistance (OFF) state in a crosspoint memory. During the last few years, researchers have made great progress in finding ways to make the switching function of these memristors behave efficiently. For example, tantalum oxide (TaO_x)-based memristors have been demonstrated to have superior endurance over other nano-scale devices capable of electronic switching. In lab settings, tantalum oxide-based memristors are capable of over 10 billion switching cycles.

[0019] A memristor may use a switching material, such as TiO_x , HfO_x or TaO_x , sandwiched between two electrodes. Memristive behavior is achieved by the movement of ionic species (e.g., oxygen ions or vacancies) within the switching

material to create localized changes in conductivity via modulation of a conductive filament between two electrodes, which results in a low resistance “ON” state, a high resistance “OFF” state, or intermediate states. Initially, when the memristor is first fabricated, the entire switching material may be nonconductive. As such, a forming process may be required to form the conductive channel in the switching material between the two electrodes. A known forming process, often called “electroforming”, includes applying a sufficiently high (threshold) voltage across the electrodes for a sufficient length of time to cause a nucleation and formation of a localized conductive channel (or active region) in the switching material. The threshold voltage and the length of time required for the forming process may depend upon the type of material used for the switching material, the first electrode, and the second electrode, and the device geometry.

[0020] Metal or semiconductor oxides may be employed in memristive devices; examples include either transition metal oxides, such as tantalum oxide, titanium oxide, yttrium oxide, hafnium oxide, niobium oxide, zirconium oxide, or other like oxides, or non-transition metal oxides, such as aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include transition metal nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride.

[0021] A common problem with memristor cells is excessive electrical resistance requiring high operating voltage to switch between high resistance states (HRS, OFF, 0) and low resistance states (LRS, ON, 1). Often, this problem is caused or exacerbated by oxidation of bottom conducting material (bottom electrode) during oxide processing which typically requires exposure to oxygen environments at elevated temperatures and by diffusion of oxygen into conducting layers during later high temperature processing and electrical testing of the device. This uncontrolled oxidation and oxygen diffusion also leads to further problems of variance contributing to low device yield.

[0022] Because oxidation of the bottom metal is also a common problem in fabrication of MIM (metal-insulator-metal) capacitors, there is a wealth of investigation

into binary and ternary oxygen diffusion barriers, mostly of the following basic structures: refractory metal-nitrogen, refractory metal-aluminum-nitrogen, and refractory metal-silicon-nitrogen. These barriers, however, were developed for use in Al and Cu metallization and are not suitable as oxygen diffusion barriers due to their reactivity and diffusivity, particularly with respect to oxygen. In addition, their relatively high electrical resistance consumes a significant amount of applied voltages. Some success has been seen using conductive oxide (CeO_2 , RuO_2) diffusion barriers in Al and Cu metallization in tandem with a Ta layer. It is hypothesized that this success is due to either the strong chemical bonding in the Ta-Ce(Ru)-O or Ta-O and the amorphous structure that forms at the Ta- CeO_2 (RuO_2) interface. This is still not the best solution, however, because a barrier oxide deposition process would pose the same oxidation problem as the subsequent memristor dielectric layer.

[0023] A selector is a highly nonlinear two-terminal device of general structure conductor-selector-conductor. When built in series with a memristor device, it increases the overall current-voltage nonlinearity of the memory cell, thereby resulting in much lower sneak path currents through partially-selected cells in high-density crossbar memory arrays. A common problem with selectors is excessively high electrical resistance requiring high operating voltage for the whole memory cell. Often, this problem is caused or exacerbated by oxidation of bottom conducting material (bottom electrode) during oxide processing (which typically requires exposure to oxygen environments at elevated temperatures) and by diffusion of oxygen into conducting layers during later high temperature processing and electrical operation of the device. This undesirable oxidation and oxygen diffusion also lead to further problems of variance contributing to low device yield and high device operation failures. Additionally, the known IMT (insulator-metal-transition)-based selector oxides (NbO_2 , Ti_2O_3 , and VO_2) are all suboxides whose stoichiometry must be tightly maintained in order to sustain the necessary negative differential resistance (NDR) behavior. Thus, blocking diffusion of oxygen

into or out of the selector layer from other oxygen containing layers and subsequent processing and electrical operation may be important.

[0024] In accordance with the teachings herein, an electrically conducting oxygen diffusion barrier is provided for a memristor structure of the general multilayer structure: conductor-oxygen barrier-dielectric-conductor and conductor-oxygen barrier-dielectric-oxygen barrier-conductor. The oxygen barrier described herein may be of the general chemical composition: Metal1-Metal2-Nonmetal, where Metal1 may be a relatively noble metal, Metal2 may be a relatively refractory metal, and Nonmetal may be nitrogen, carbon, or oxygen or mixtures thereof.

[0025] The noble metal M1 may be one of the following: Ru, Rh, Pd, Os, Ir, Pt, and Re or alloys thereof. The refractory metal M2 may be one of the following: Ta, W, Nb, V, Ti, Zr, Hf, Cr, and Mo or alloys thereof. The composition M1-M2-NM of the oxygen barrier may be described by the following composition ranges: M1 ranges from about 10 to 80 atomic percent (at%), M2 ranges from about 10 to 50 at%, and NM ranges from about 5 to 70 at%.

[0026] The finished memristor cell can be operated by applying an electric potential across the two conducting layers to change between resistance states. The virgin resistance, and therefore the operation voltage of a given memristor with the barrier layer may be significantly lower than one without. The barrier layer blocks oxidation of and oxygen diffusion into the bottom electrode conducting layer during subsequent processing. It has been shown that compounds composed from these element groups form strong chemical bonds and amorphous microstructures, thereby enabling them to block diffusion. They are also oxidation resistant and their oxides remain electrically conductive. These properties may make them ideal for use as electrically conductive oxygen diffusion barriers.

[0027] An advantage of these ternary oxygen diffusion barriers is that they can be deposited without oxidizing the bottom conducting layer (with exception of the Metal1-Metal2-oxygen composition) and they effectively block oxidation of the

conducting layer as well as maintain their own electrical conductivity during further processing. This may allow for fabrication of memristors without oxidation of bottom electrodes, thereby resulting in less variance across an array of memristor cells and lower virgin resistance, which reduces the required operating voltage.

[0028] The ternary oxygen diffusion barrier may be a single layer or may be multiple layers, depending on the solid state solubility of the components. For example, two layer schemes may be formed as a method of deposition, i.e., M1 and M2-NM deposited in thin alternating layers but the net effect may be a single, ultrathin barrier layer.

[0029] The sneak-path issue is inherent for crossbar architectures, regardless of the memory element employed. FIG. 1A depicts a crossbar 100 containing a plurality of memory elements 102. Each memory element 102 may include a switching oxide sandwiched between a bottom electrode and a top electrode (not visible in FIG. 1, but depicted in FIG. 4). Each memory element 102 is sandwiched between a bottom electrically conducting trace 106 and a top electrically conducting trace 108. The crossbar 100 is made of a lower layer 110 of electrically conducting traces formed by a plurality of bottom conducting traces 106 and an upper layer 112 of electrically conducting traces formed by a plurality of top conducting traces 108, with the memory element 102 at each crosspoint 114 formed by a bottom trace 106 and a top trace 108. The bottom conductive traces 106 may be referred to as row, or bit, lines, while the top conductive traces 108 may be referred to as column, or word, lines. However, it is immaterial whether the row (bit) lines are above or below the column (word) lines.

[0030] FIG. 1A depicts the situation that while trying to read the high resistive element 102a, a current sneak path exists due to three low resistive elements 102b. The thin line 116 with arrow head shows the desired current path. The dashed line 118 with arrow head shows a sneak path current path.

[0031] The solution, illustrated in FIG. 1B, may be to increase the nonlinearity or asymmetry of the I-V characteristic of the memristor elements 102, which may ensure that the memristor, or other nonlinear memory device, can be used in large crossbar arrays 150. Increasing the nonlinearity of the memristor cells 102 may result in reduction or even elimination of the sneak path current path 118. As noted above, a nonlinear, nonvolatile memristor cell 102' may include a selector 130 (discussed below in connection with FIG. 5) and a memristor element 102. The selector 130 may be nonlinear and volatile; the memristor 102 may be linear and nonvolatile. While these are the ideal states of the selector 130 and memristor 102, respectively, it is understood that there may be slight variations from the ideal state. In any event, the net intent is to provide a memory cell 102' that is both nonlinear and nonvolatile.

[0032] The selector 130 may be used to mitigate the sneak path current issue by utilizing its nonlinearity, i.e., exhibiting a very low leakage current at low voltage regime while a very high current level once the applied voltage is above a threshold value. Nonlinearity may depend on the operating voltage range, which in turn depends on the materials used and structure of the device stack (memristor plus selector).

[0033] The following is a description on selector set/reset operating voltage. The selector is a volatile threshold switch. A selector may have a threshold voltage, V_{th} , that when a voltage $V > V_{th}$, the selector is in a low resistance state. On the other hand, when $V < V_{th}$, the selector is in a high resistance state. In one illustrative example, a voltage V was selected, V being above V_{th} while $\frac{1}{2} V$ was below V_{th} .

[0034] When $+1/2 V$ is applied on one row (selected row), and $-1/2V$ on one column (selected column), the device at the junction (selected device) has V so that it is in a low resistance state. In this example, as a voltage divider the voltage drop on this selector becomes low, and main voltage V drops on the resistive memory element e.g., ReRAM, such as memristor) for memristor set or reset. The remaining devices on selected row or column has either $+1/2V$ or $-1/2V$ (half

selected devices), and they are in high resistance state. The remaining devices in the array are all unselected, all in a high resistance state.

[0035] The concept for a selector associated with the popular reading scheme is shown in FIG. 2. The selected high resistance cell is denoted 102'a and the cells having low resistance are denoted 102'b. The low resistance cells 102'b are in the same row or column as the selected cell 102'a. It is the low resistance cells 102'b that may support sneak path currents. V is the applied voltage, V/2 is half voltage, and G is ground.

[0036] A structure 300 having a memristor 102 with one oxygen barrier 302 is depicted in FIG. 3. The memristor 102 may have a bottom electrode 304, a memristive switch layer 306, and a top electrode 308. The oxygen barrier 302 may be formed between the bottom electrode 304 and the memristive switch layer 306.

[0037] A structure 400 having a memristor 102 with two oxygen barriers 302a, 302b is depicted in FIG. 4. One oxygen barrier 302a may be formed between the bottom electrode 304 and the memristive switching layer 306 and the other oxygen barrier 302b may be formed between the top electrode 308 and the memristive switching layer 306.

[0038] A structure 500 having a selector 130 with one oxygen barrier 502 is depicted in FIG. 5. The selector 130 may have a bottom electrode 504, a selector insulator layer 506, and a top electrode 508. The oxygen barrier 502 may be formed between the bottom electrode 504 and the selector insulator layer 506.

[0039] A structure 550 having a selector 130 with one oxygen barrier 502 is depicted in FIG. 6. The selector 130 may have a bottom electrode 504, a selector insulator layer 506, and a top electrode 508. The oxygen barrier 502 may be formed between the top electrode 508 and the selector insulator layer 506. For the selector, one oxygen barrier may be useful if the bottom electrode and top electrode are not symmetric. In this case, the barrier may be placed where oxygen can migrate between the electrode and the selector insulator layer 506. This electrode can be either the bottom electrode or the top electrode. If electrodes

are symmetric, then two oxygen barriers, one for each electrode, may be useful, as shown in FIG. 7.

[0040] A structure 575 having a selector 130 with two oxygen barriers 502a, 502b is depicted in FIG. 7. One oxygen barrier 502a may be formed between the bottom electrode 504 and the selector insulator layer 506 and the other oxygen barrier 502b may be formed between the top electrode 508 and the selector insulator layer 506.

[0041] A structure 800 having a combined memristor 102 and a selector 130 with four oxygen barriers is depicted in FIG. 8. A first oxygen barrier 302a may be formed between the first bottom electrode 304 and the memristive switching layer 306 and a second oxygen barrier 302b may be formed between the first top electrode 308 and the memristive switching layer 306. A third oxygen barrier 502a may be formed between the second bottom electrode 504 and the selector insulator layer 506 and a fourth oxygen barrier 502b may be formed between the second top electrode 508 and the selector insulator layer 506. At least the second barrier layer 302b is optional. For the selector 130, it may be desirable to have two barriers 502a, 502b so as to maintain oxide stoichiometry to preventing oxygen migration at both electrodes 504, 508.

[0042] For the memristor 120, one barrier 302a or 302b may suffice. Alternatively, two barriers, 302a, 302b may be used. It may be desirable to prevent oxygen migration between the switching oxide 306 and switching electrode (either 304 or 308), where a barrier layer would be desirable. On the other hand, it may be desirable to maintain oxygen migration between the switching oxide and the oxygen reservoir electrode, in which case, the barrier would not be needed. That is to say, the electrodes 304, 304 of the memristor 120 may be non-symmetric, one as the switching electrode (channel contact/non-contact) and the other as the oxygen vacancy reservoir. In this case, the barrier may be desired for the switching electrode, and a barrier may not be needed at the oxygen reservoir electrode.

[0043] In the structure 800 shown in FIG. 8, all four of the barrier layers 302a, 302b, 502a, 502b may be present. In some examples, at least one layer 302a, 302b, 502a or 502b may be present, in either the memristor 102 or selector 130.

[0044] Deposition of the metal layers 304, 308, 504, and 508 may be performed by such processes as electroplating, sputtering, evaporation, ALD (atomic layer deposition), co-deposition, chemical vapor deposition, IBAD (ion beam assisted deposition), oxidation of pre-deposited materials, or any other film deposition technology. The switching oxide layer 306, and the selector insulator layer 506 may be formed by e-beam deposition, e-beam co-evaporation, sputter deposition, co-sputter deposition, reactive sputter deposition, reactive co-sputter deposition, atomic layer deposition (ALD) sequential deposition, sputter sequential deposition, e-beam sequential deposition, and the like. The barrier layers 302a, 302b, 502a, 502b, to the extent that they are used, may be deposited by any of the foregoing listed processes. Further examples may include co-deposition of M1 (or M1-NM_x) and M2-NM_y and reactive co-deposition and sequential deposition of M1, M2-NM_x.

[0045] The layers 304, 302a (if used), 306, 302b (if used), 308, 504, 502a (if used), 506, 502b (if used), and 508 may be deposited sequentially. It will be appreciated that in FIG. 8, the selector 130 is shown on “top” and the memristor 102 is shown on the “bottom” of the device 800. However, in some examples, the memristor 102 may be on “top” and the selector 130 on the “bottom”.

[0046] Three compositions, all in the Pt-Nb-N system, were prepared by co-sputtering Pt and NbN targets with Ar and N₂. Table I below lists the conditions of preparation, including the power settings (in W) for Pt and NbN and the flow rates (in sccm) for Ar and N₂.

Table I. Pt-Nb-N Compositions and Preparation Parameters (Composition in at%).

	Pt, W	NbN, W	Ar, sccm	N ₂ , sccm	Final Compo- sition
Composi- tion 1	50	350	250	50	25% Pt, 26% Nb, 41% O, 8% N
Composi- tion 2	50	250	250	50	65% Pt, 29% Nb, 6% N
Composi- tion 3	100	250	250	50	78% Pt, 20% Nb, 2% N

[0048] Each composition was tested for oxidation resistance by measuring resistivity before anneal and after anneal. Annealing was done by an in-air anneal at 750°C for 24 hr. Table II lists the results before and after the anneal. The substrate was 200 nm thermally-grown SiO₂ on silicon.

Table II. Oxidation Resistance (Composition in at%).

Pt-Nb-N	Composition	Sub- strate	Thickness	Resistivity (before an- neal)	Resistivity (after an- neal)
Comp1	25% Pt, 26% Nb, 41% O, 8% N	SiO ₂ 200 nm/Si	109 nm	199 $\mu\Omega\text{cm}$	(too resis- tive)
Comp2	65% Pt, 29% Nb, 6% N	SiO ₂ 200 nm/Si	93.3 nm	176 $\mu\Omega\text{cm}$	79.5 $\mu\Omega\text{cm}$

Comp3	78% Pt, 20% Nb, 2% N	SiO ₂ 200 nm/Si	139 nm	113 $\mu\Omega\text{cm}$	19.8 $\mu\Omega\text{cm}$
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[0049] The advantage of these ternary oxygen diffusion barrier layers 302a, 302b, 502a, 502b is that they can be deposited without oxidizing the bottom conducting layer (with some exceptions with the Metal1-Metal2-oxygen composition) and they may effectively block oxidation of the conducting layers 304, 308, 504, 508 and suboxide layers 306, 506 as well as maintain their own electrical conductivity during further processing. This allows for fabrication of selector-memristor memory cells without oxidation of bottom electrodes or further oxidation of the suboxide selector layers resulting in less variance across an array of selector-memristor memory cells and lower virgin resistance, thereby reducing the required operating voltage.

CLAIMS

What is claimed is:

1. A memory cell comprising either a nonvolatile resistance memory device or a nonvolatile memory device in series with a selector, in which the nonvolatile resistance memory device includes a dielectric layer sandwiched between a first bottom electrode and a first top electrode and wherein the selector includes a selector insulator layer sandwiched between a second bottom electrode and a second top electrode, wherein either or both of the nonvolatile resistance memory device and selector include an electrically conducting oxygen diffusion barrier layer between one of the electrodes and the dielectric layer or selector insulator layer, respectively, wherein the barrier layer comprises a composition M1-M2-NM, where M1 is a noble metal, Metal2 is a refractory metal, and Nonmetal is nitrogen, carbon, or oxygen or mixtures thereof.

2. The memory cell of claim 1, in which the nonvolatile resistance memory device is a memristor.

3. The memory cell of claim 1, in which the nonvolatile resistance memory device includes the barrier layer between either the first bottom electrode and the dielectric or between the dielectric and the first top electrode, or both.

4. The memory cell of claim 1, in which the selector includes the barrier layer between either the second bottom electrode and the selector insulator or between the selector insulator and the second top electrode, or both.

5. The memory cell of claim 1, in which the M1 is a metal selected from the group consisting of Ru, Rh, Pd, Os, Ir, Pt, and Re, and M2 is a metal selected from the group consisting of Ta, W, Nb, V, Ti, Zr, Hf, Cr, and Mo.

6. The memory cell of claim 5, in which M1 ranges from about 10 to 80 at% of the structure, M2 ranges from about 10 to 50 at% of the structure, and NM ranges from about 5 to 70 at% of the structure.

7. A memory array with nonvolatile memory cells, the memory array including:

a set of electrically conducting row lines intersecting a set of electrically conducting column lines to form intersections; and

each nonvolatile memory cell disposed at each intersection between one of the row lines and one of the column lines;

wherein the memory cell comprises either a nonvolatile resistance memory device or a nonvolatile memory device in series with a selector, in which the nonvolatile resistance memory device includes a dielectric sandwiched between a first bottom electrode and a first top electrode and wherein the selector includes a selector insulator sandwiched between a second bottom electrode and a second top electrode, wherein either or both of the nonvolatile resistance memory device and selector include an electrically conducting oxygen diffusion barrier layer between one of the electrodes and the dielectric or selector insulator, respectively, and

wherein the first bottom electrode is electrically coupled to a row trace or to a column trace and wherein the second top electrode is electrically coupled to the other of the row trace or the column trace.

8. The memory array of claim 7, wherein the non-volatile memory device is a memristor.

9. The memory array of claim 7, in which the nonvolatile resistance memory device includes the barrier layer between either the first bottom electrode and the dielectric or between the dielectric and the first top electrode, or both.

10. The memory array of claim 7, in which the selector includes the barrier layer between either the second bottom electrode and the selector insulator or between the selector insulator and the second top electrode, or both.

11. The memory array of claim 7, in which the barrier layer comprises a structure comprising M1-M2-NM, where M1 is a metal selected from the group consisting of Ru, Rh, Pd, Os, Ir, Pt, and Re, M2 is a metal selected from the group consisting of Ta, W, Nb, V, Ti, Zr, Hf, Cr, and Mo, and NM is a non-metal selected from the group consisting of O, N, and C.

12. The memory array of claim 11, in which M1 ranges from about 10 to 80 at% of the structure, M2 ranges from about 10 to 50 at% of the structure, and NM ranges from about 5 to 70 at% of the structure.

13. A method of manufacturing a memory array with nonvolatile memory cells, the method including:

providing a set of electrically conducting row traces;

providing a plurality of memory cells, each memory cell disposed at a location along each of the row traces, wherein each memory cell comprises either a nonvolatile resistance memory device or a nonvolatile memory device in series with a selector, wherein the nonvolatile resistance memory device includes a dielectric layer sandwiched between a first bottom electrode and a first top electrode and

wherein the selector includes a selector insulator layer sandwiched between a second bottom electrode and a second top electrode, wherein either or both of the non-volatile resistance memory device and selector include an electrically conducting diffusion barrier layer between one of the electrodes and the dielectric layer or selector insulator layer, respectively, and

providing a set of electrically conducting column traces to contact each memory cell at a unique intersection.

14. The method of claim 13, in which the barrier layer is a structure comprising M1-M2-NM, where M1 is a metal selected from the group consisting of Ru, Rh, Pd, Os, Ir, Pt, and Re, M2 is a metal selected from the group consisting of Ta, W, Nb, V, Ti, Zr, Hf, Cr, and Mo, and NM is a non-metal selected from the group consisting of O, N, and C.

15. The method of claim 14, in which M1 ranges from about 10 to 80 at% of the structure, M2 ranges from about 10 to 50 at% of the structure, and NM ranges from about 5 to 70 at% of the structure.

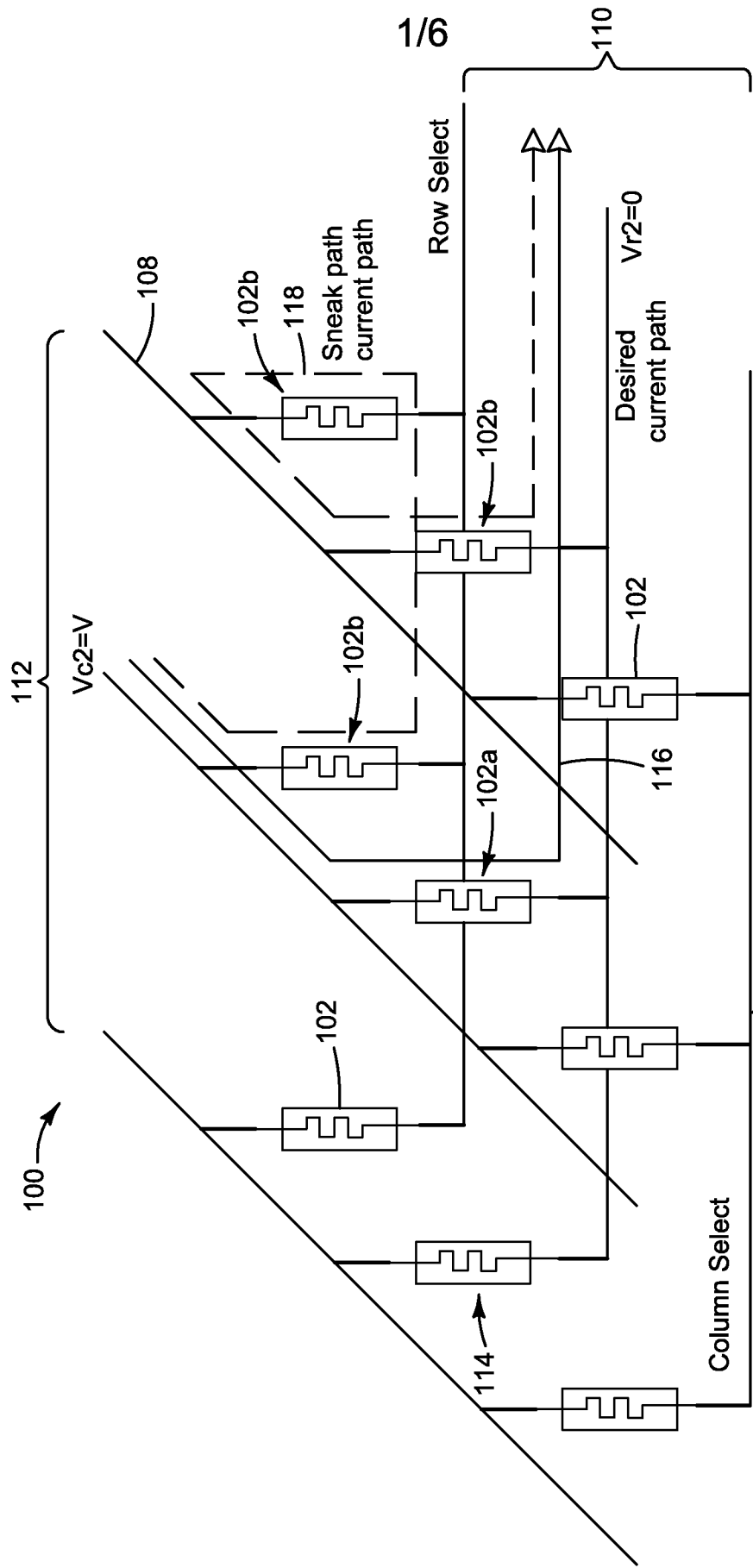


FIG. 1A

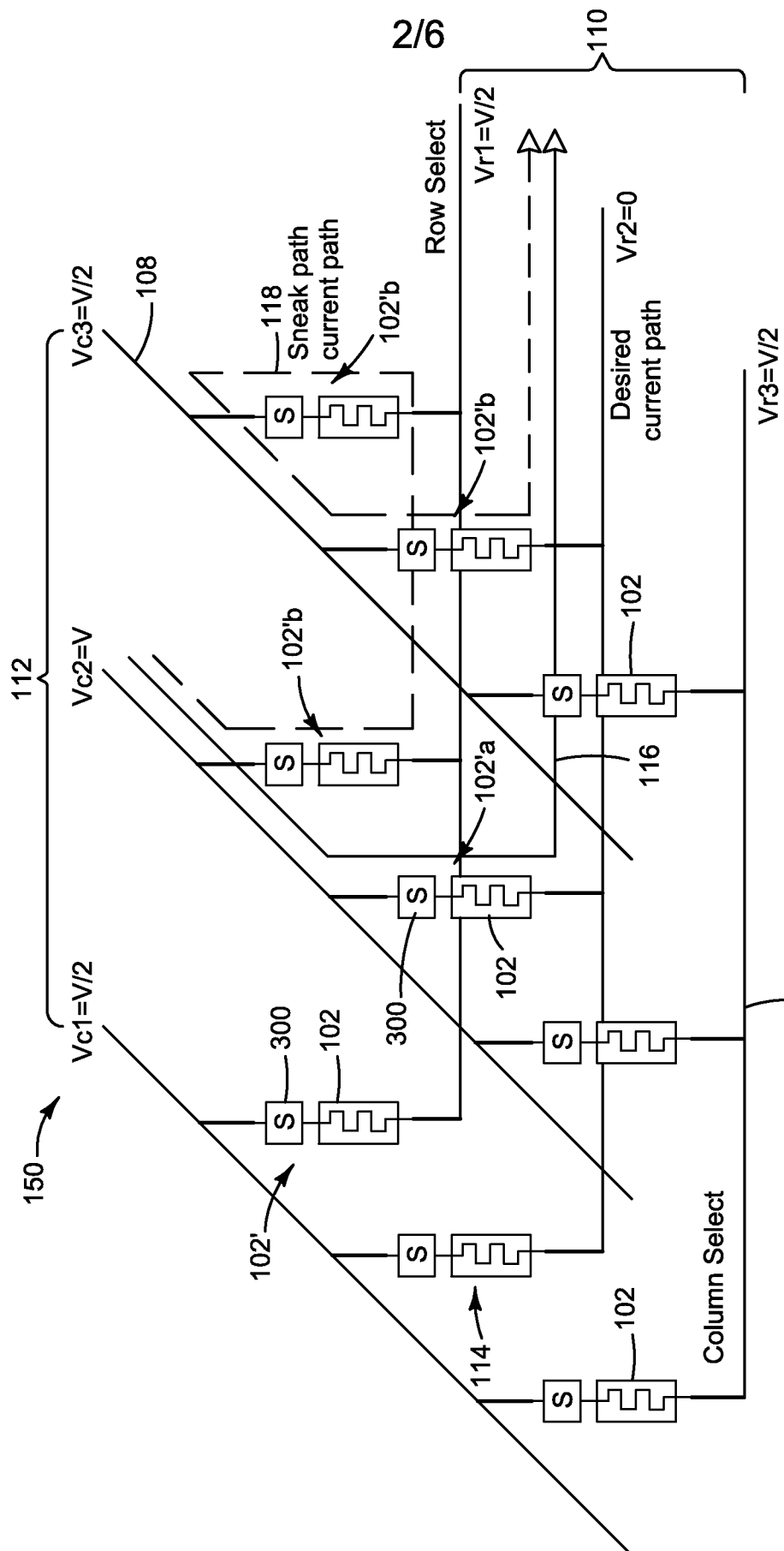


FIG. 1B

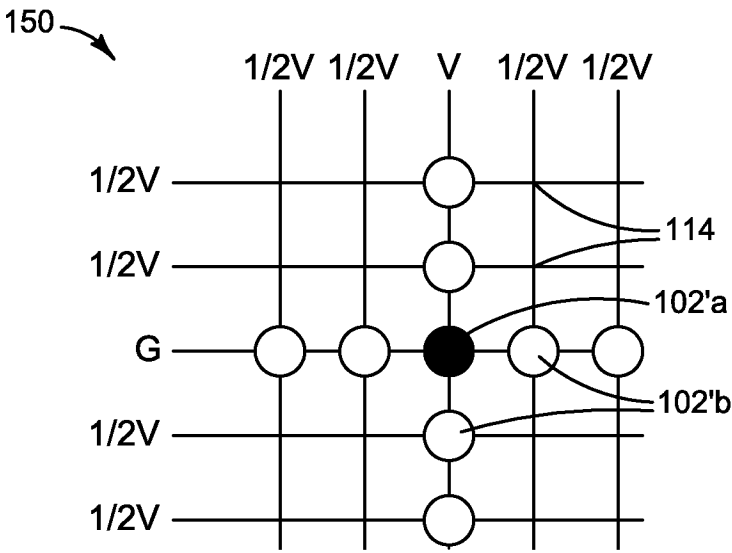


FIG. 2

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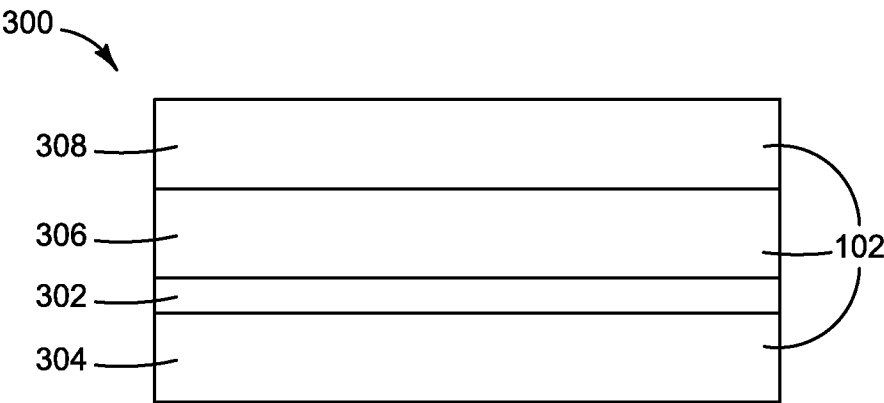


FIG. 3

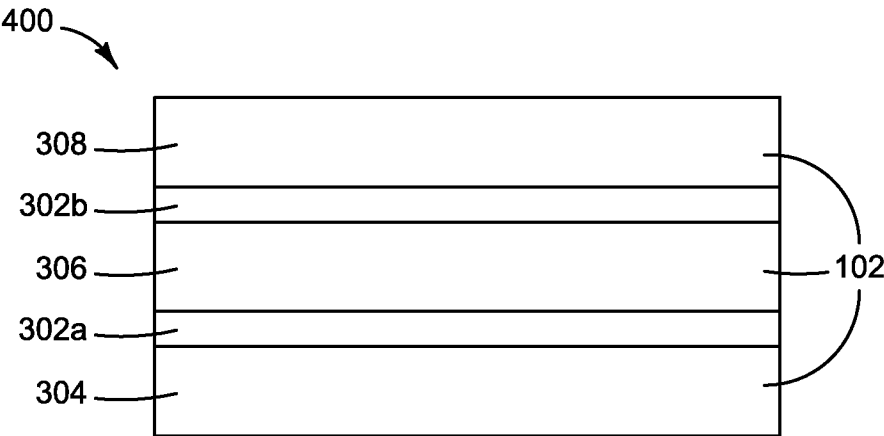


FIG. 4

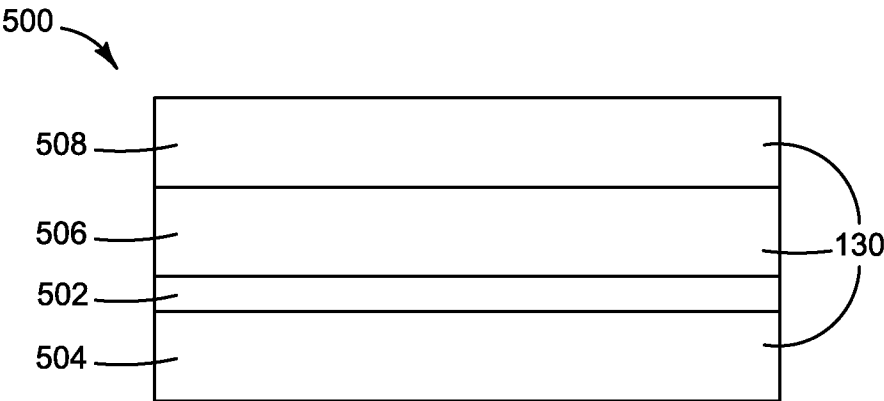


FIG. 5

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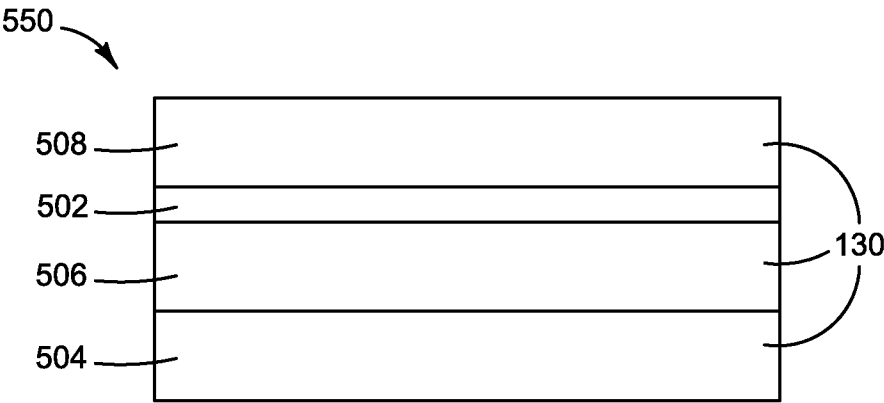


FIG. 6

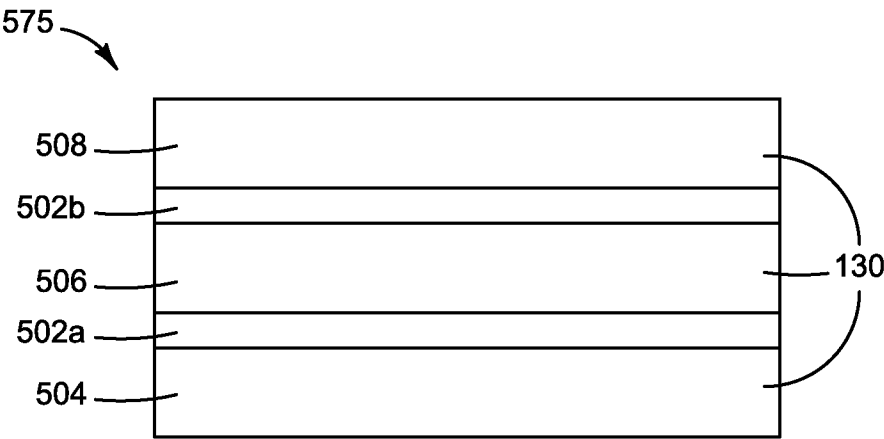


FIG. 7

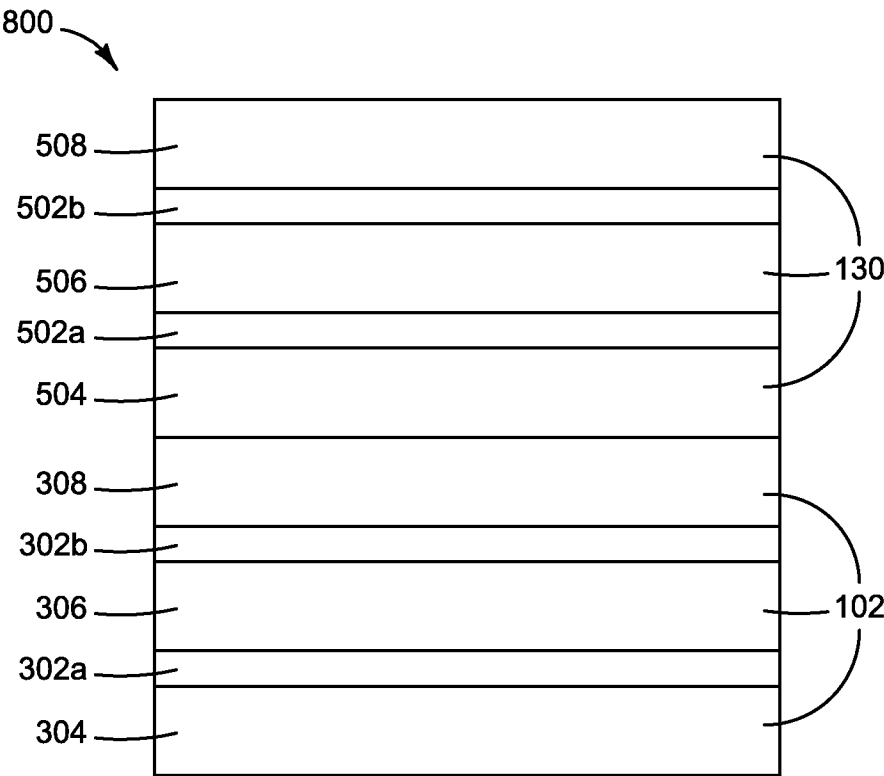


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/024444**A. CLASSIFICATION OF SUBJECT MATTER****G11C 11/15(2006.01)i, H01L 27/115(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/15; H01L 27/108; H01L 21/16; H01L 45/00; H01L 21/02; H01L 49/02; G11C 11/00; H01L 27/115

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: nonvolatile, resistance, memory, selector, insulator, dielectric, layer, barrier, noble, refractory, nitrogen, metal, nonmetal, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0175603 A1 (VENKAT ANANTHAN et al.) 26 June 2014 See paragraphs [0038], [0040], [0053]; and figures 2, 5B.	1-15
Y	US 2008-0278990 A1 (PRAGATI KUMAR et al.) 13 November 2008 See paragraphs [0018], [0032], [0035]-[0036], [0039]; claim 4; and figures 2A-2B.	1-15
A	US 2012-0313070 A1 (R. STANLEY WILLIAMS et al.) 13 December 2012 See paragraph [0018]; and figure 2A.	1-15
A	US 2003-0173612 A1 (JURI H. KRIEGER et al.) 18 September 2003 See paragraphs [0035]-[0037]; and figure 1.	1-15
A	US 2011-0310655 A1 (FRANZ KREUPL et al.) 22 December 2011 See paragraphs [0074]-[0075]; and figure 1.	1-15



Further documents are listed in the continuation of Box C.



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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

05 January 2016 (05.01.2016)

Date of mailing of the international search report

06 January 2016 (06.01.2016)

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Information on patent family members

International application No.

PCT/US2015/024444

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