United States Patent [19]
Duley

[11] **3,858,703**
[45] **Jan. 7, 1975**

[54] **BIDIRECTIONAL DUAL HEAD PRINTER**

[75] Inventor: **Howard Duley**, Hudson, N.H.

[73] Assignee: **Centronics Data Computer Corp.**, Hudson, N.H.

[22] Filed: **Nov. 12, 1973**

[21] Appl. No.: **414,645**

[52] **U.S. Cl.** .... **197/1 R**
[51] **Int. Cl.** **B41j 1/34**
[58] **Field of Search** .... 197/1 R; 346/75, 78; 101/93 C; 340/172.5

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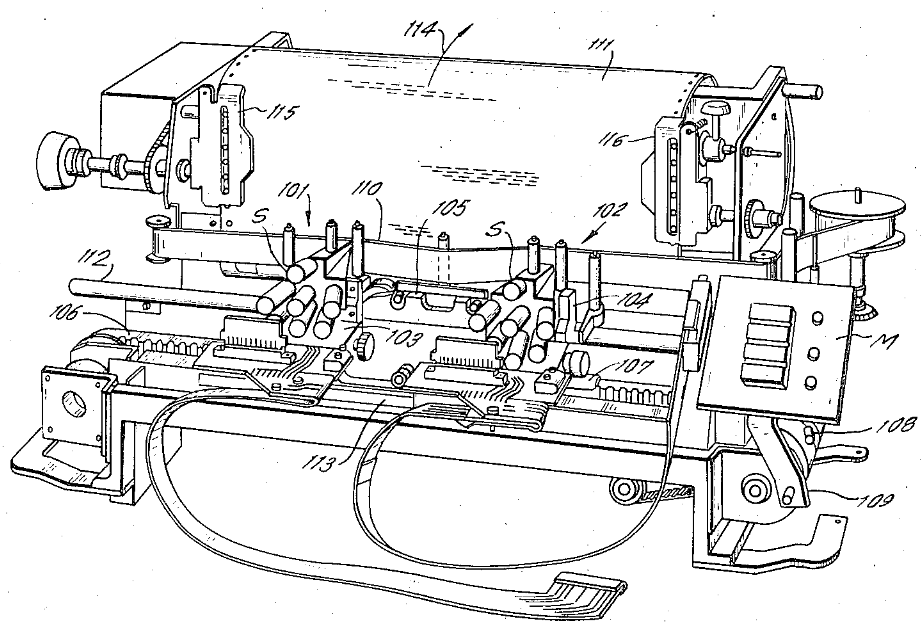
Primary Examiner—Robert E. Bagwill
Assistant Examiner—R. T. Rader
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen

[57] **ABSTRACT**

A high-speed impact printer of the dot-matrix type employing at least first and second print head assemblies for printing characters or other symbols in line-by-line fashion upon a paper document. In the dual head embodiment each print head assembly prints substantially one-half of the line of characters or symbols and both heads operate simultaneously during the print mode. The print mode is such that printing of every other line occurs as the print heads move from left to right and printing of the interspersed lines occurs as the print heads move from right to left after having completed the previous line of characters or other symbols. Novel electronics are provided to accomplish the above printing modes. The multiple head printer may also be employed in a graphics mode. It is further possible to employ more than two heads, for example, three or more, in either the printing or graphic modes, if desired. The printer has the further capability of "half-step" printing.

13 Claims, 38 Drawing Figures



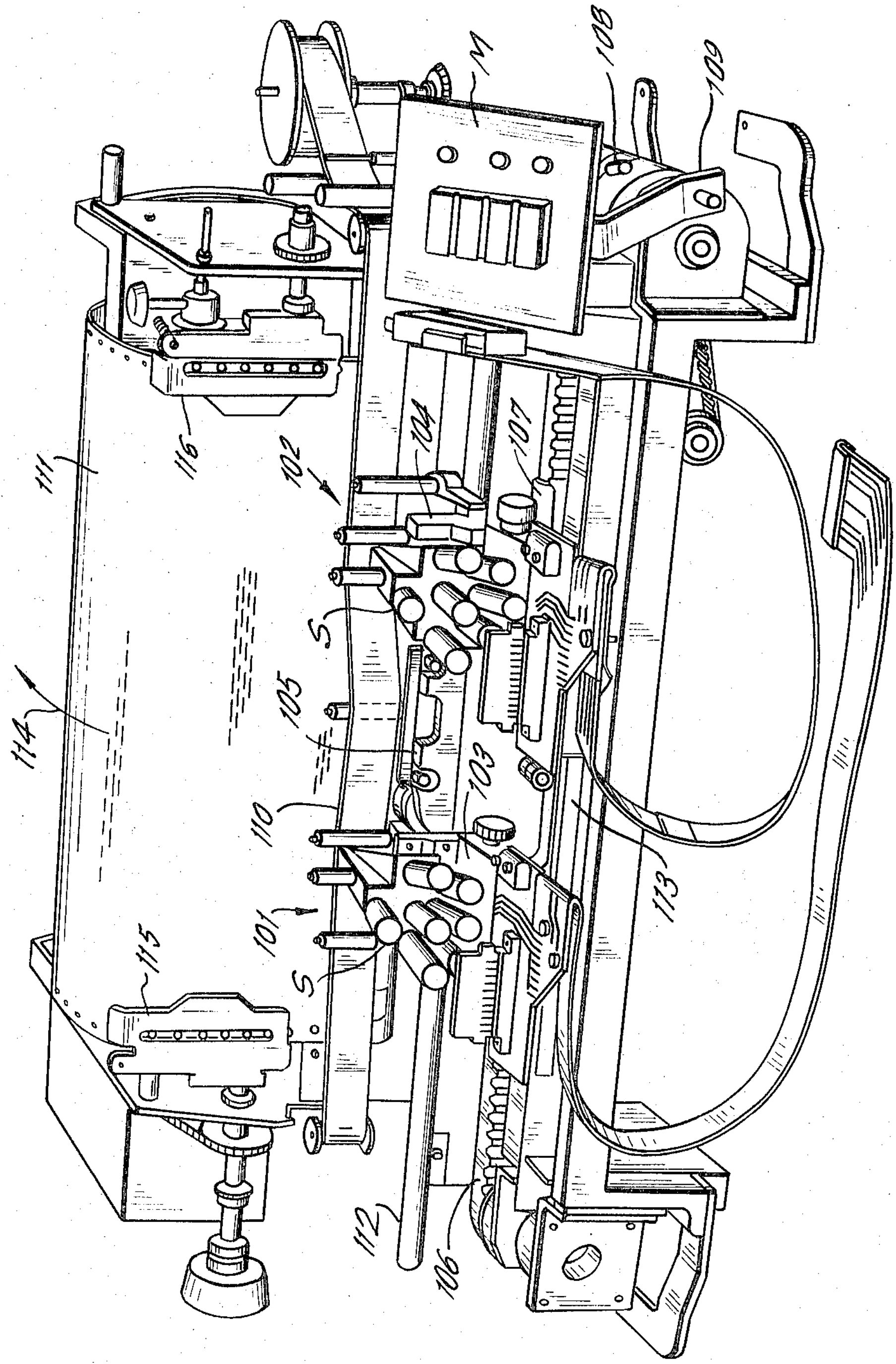

M
108
109
116
111
102
104
107
S
105
103
110
114
101
S
113
115
112
106

FIG. 1

FIG. 2a

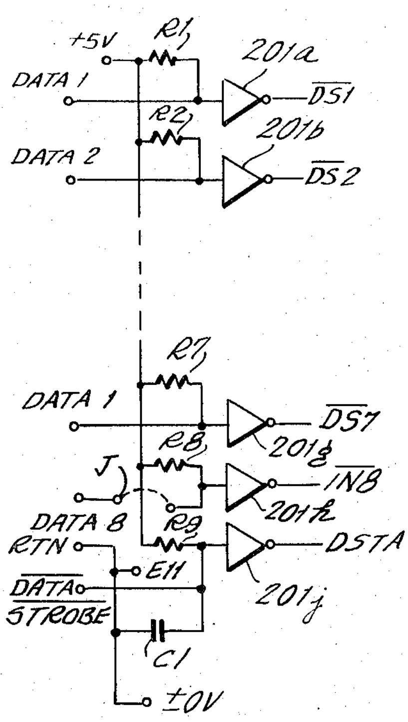


FIG. 2b

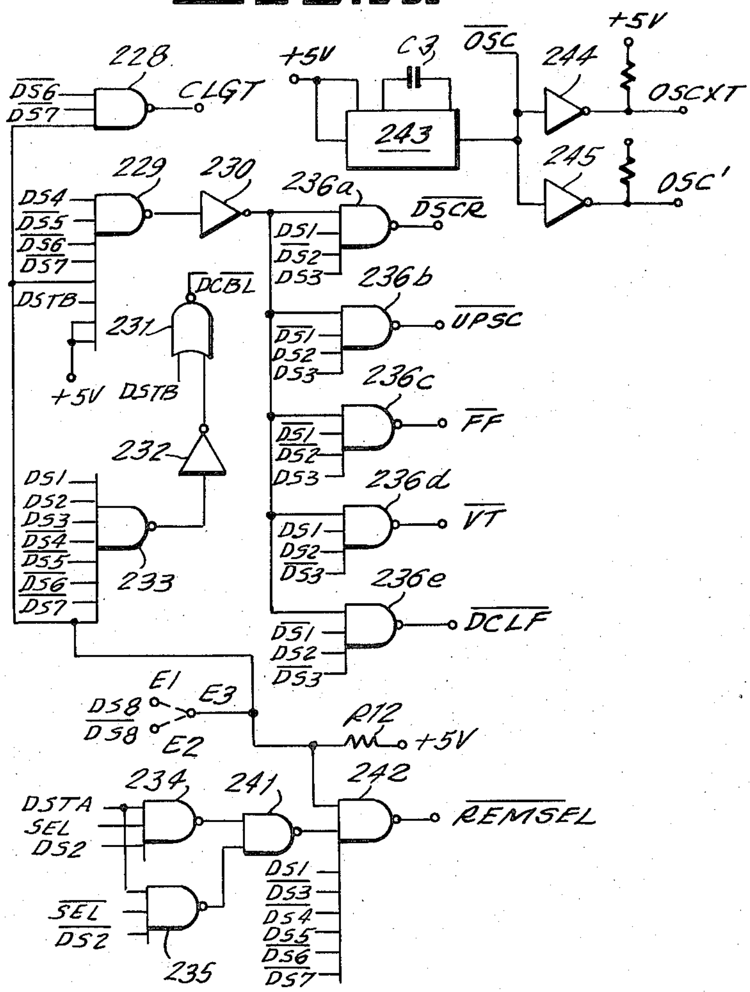


FIG. 2c

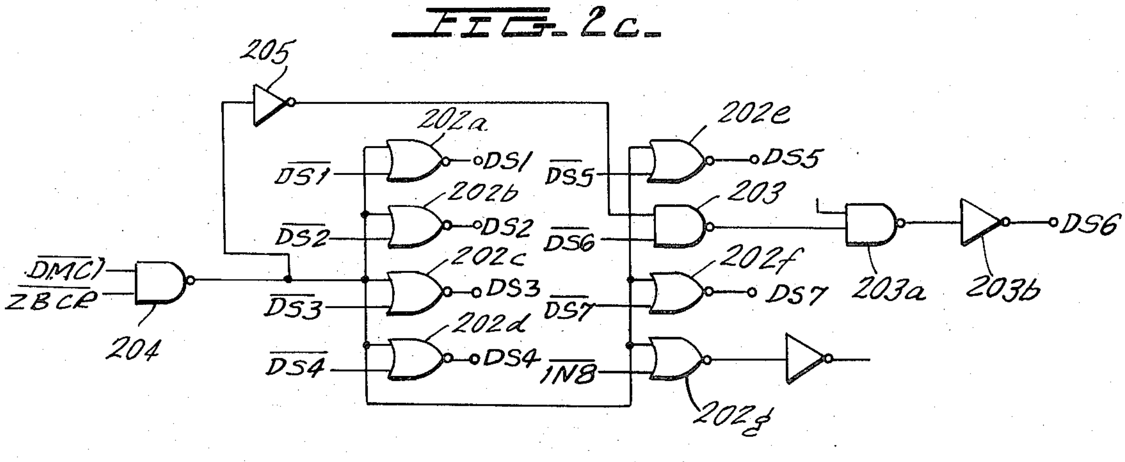


FIG. 2d

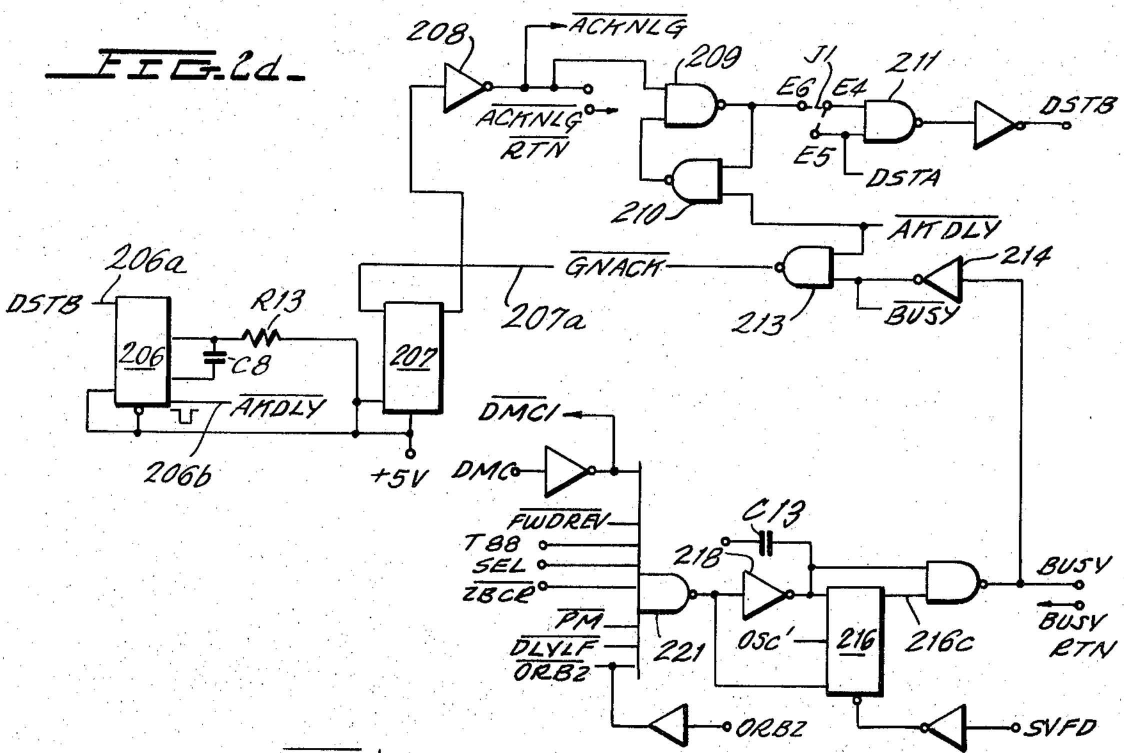


FIG. 2e

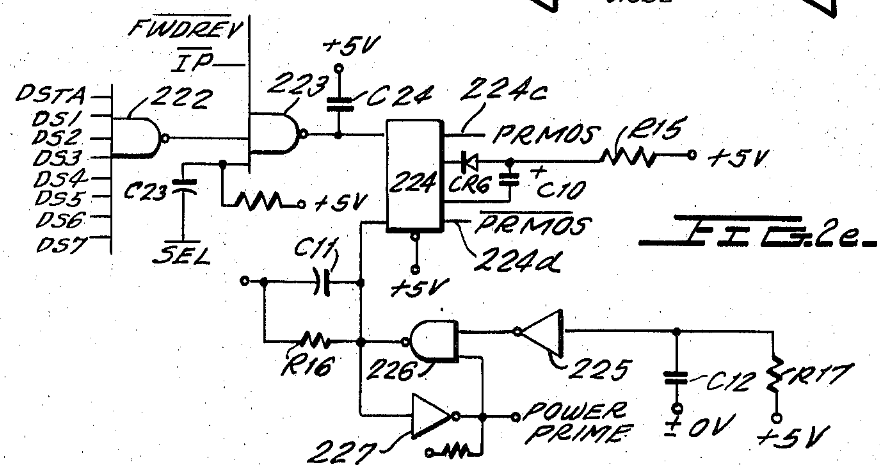


FIG. 2f

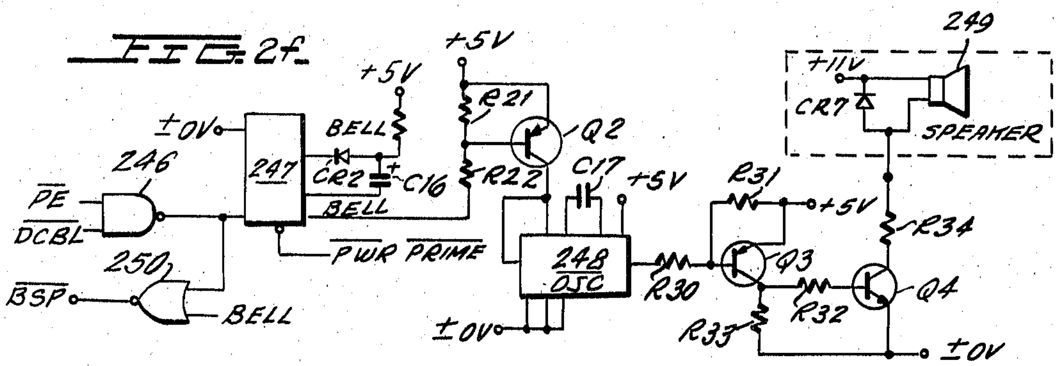
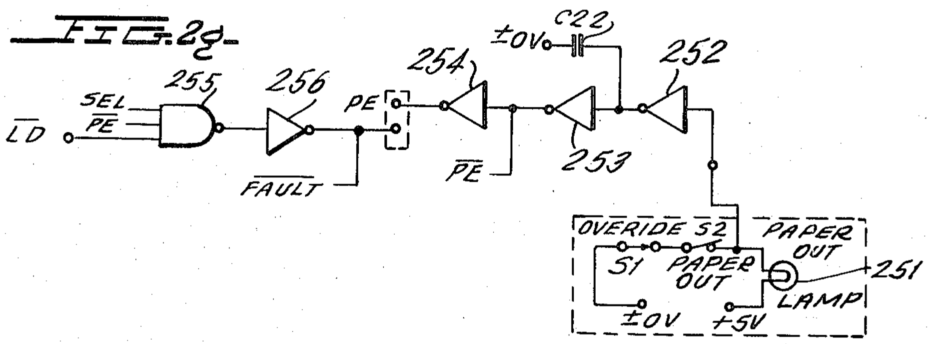


FIG. 2g.



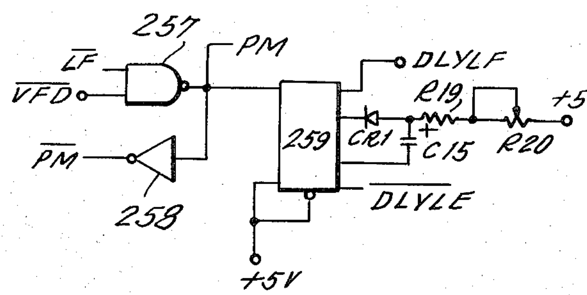


FIG. 2h.

FIG. 2j.

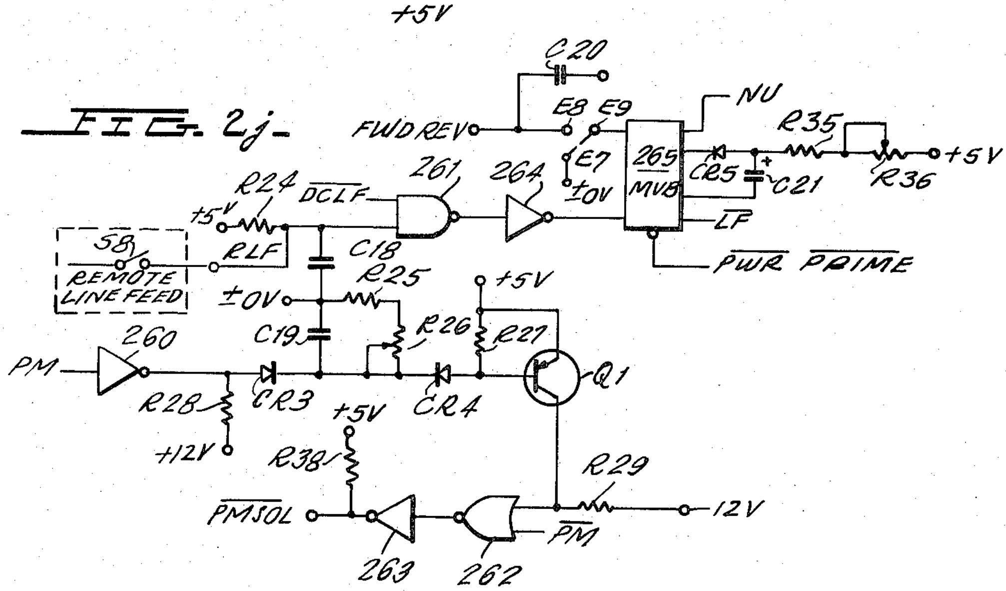


FIG. 2k.

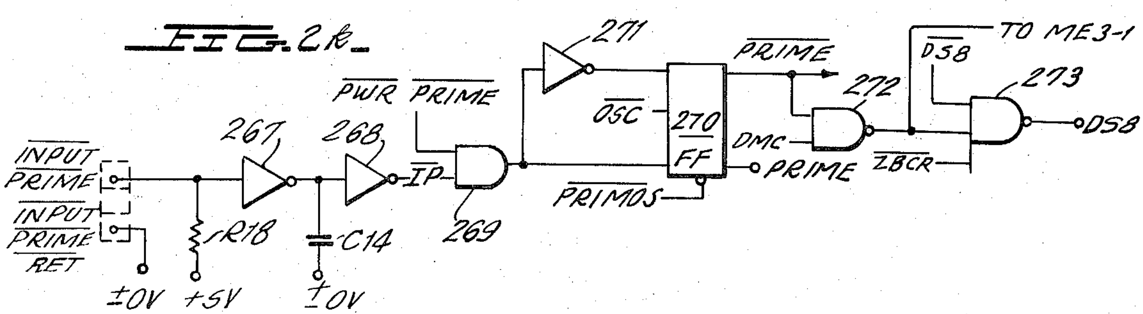


FIG. 2m.

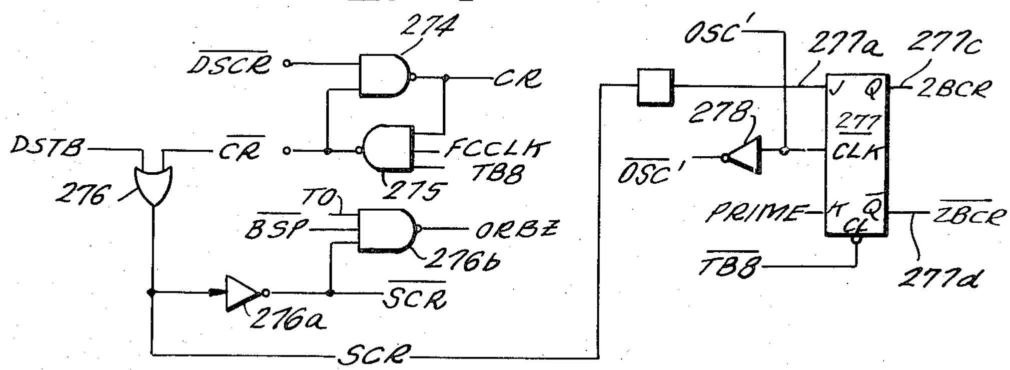


FIG. 2n.

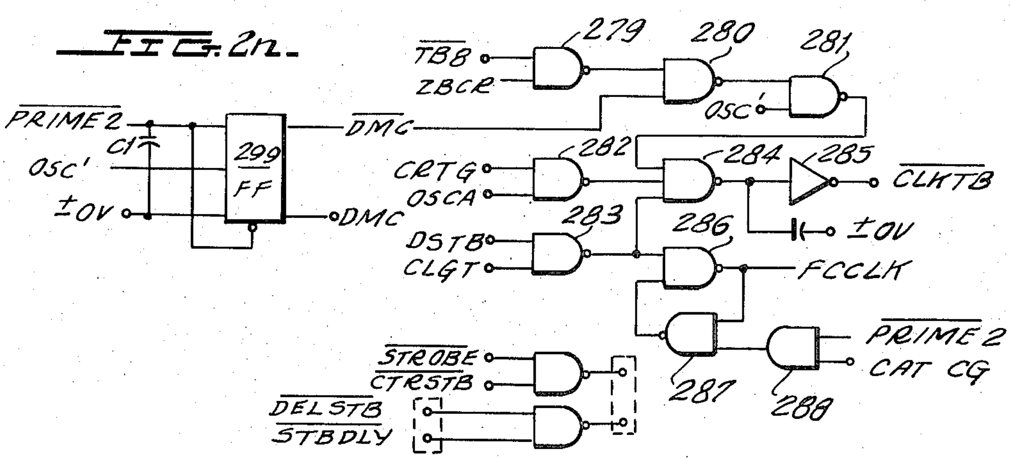
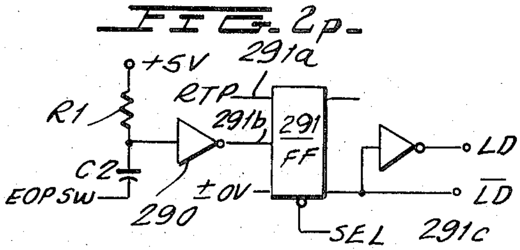


FIG. 2p.



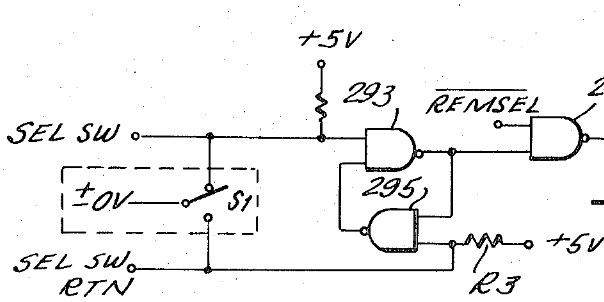
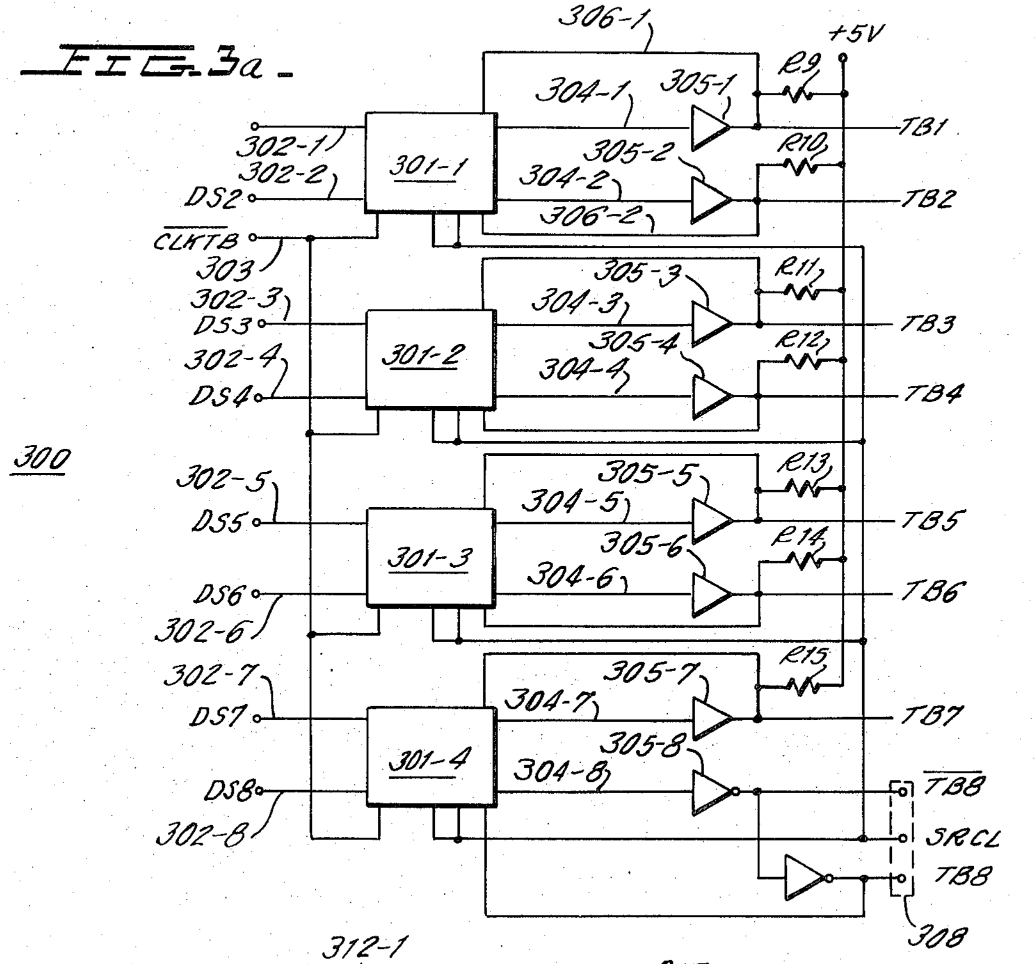


FIG. 2q.

FIG. 3a


300
306-1
+5V
R9
304-1
305-1
TB1
302-1
302-2
301-1
305-2
R10
304-2
DS2
306-2
TB2
CLKTB
303
305-3
R11
302-3
304-3
DS3
TB3
302-4
301-2
305-4
R12
304-4
DS4
TB4
305-5
R13
302-5
304-5
DS5
TB5
301-3
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R14
304-6
DS6
TB6
302-6
R15
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SRCL
TB8
302-8
308

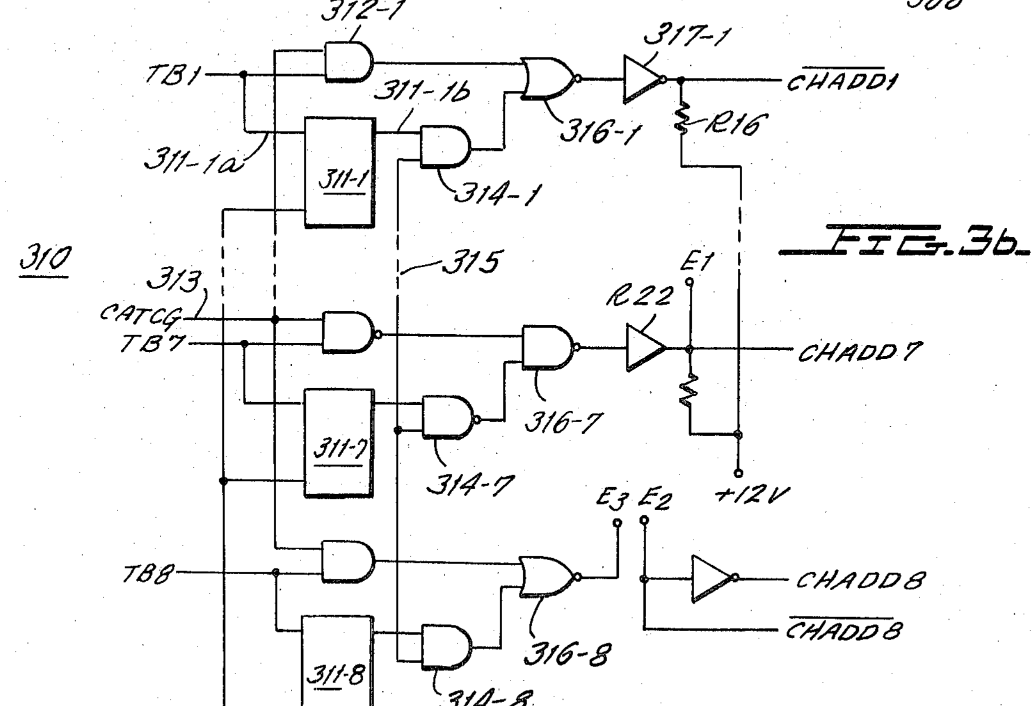
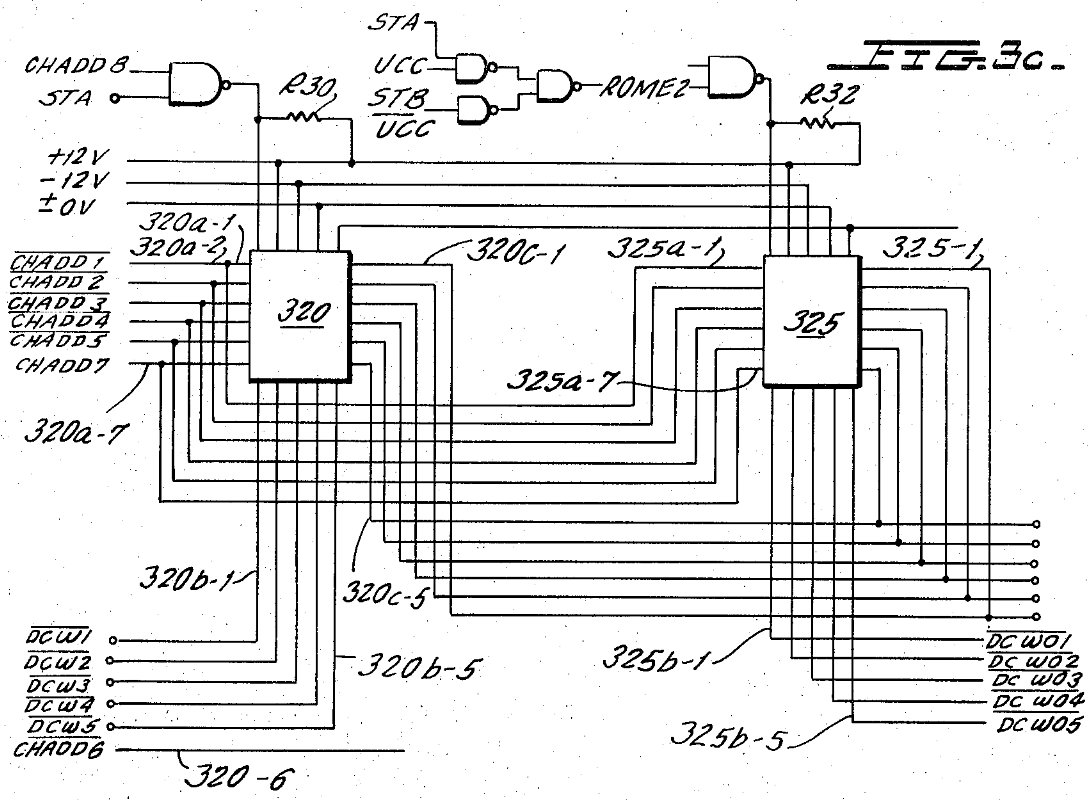

312-1
317-1
TB1
CHADD1
311-1b
316-1
R16
311-1a
311-1
314-1
310
315
313
E1
CATCG
R22
TB7
CHADD7
311-7
316-7
314-7
+12V
E3
E2
TB8
CHADD8
CHADD8
311-8
316-8
314-8

FIG. 3b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STA
R30
STA
UCC
STB
UCC
ROMEZ
R32
+12V
−12V
±0V
320a-1
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CHADD1
CHADD2
CHADD3
CHADD4
CHADD5
CHADD7
320
320C-1
325a-1
325-1
325
325a-7
320a-7
320b-1
320c-5
320b-5
DCW1
DCW2
DCW3
DCW4
DCW5
CHADD6
320-6
325b-1
325b-5
DCW01
DCW02
DCW03
DCW04
DCW05

FIG. 3c

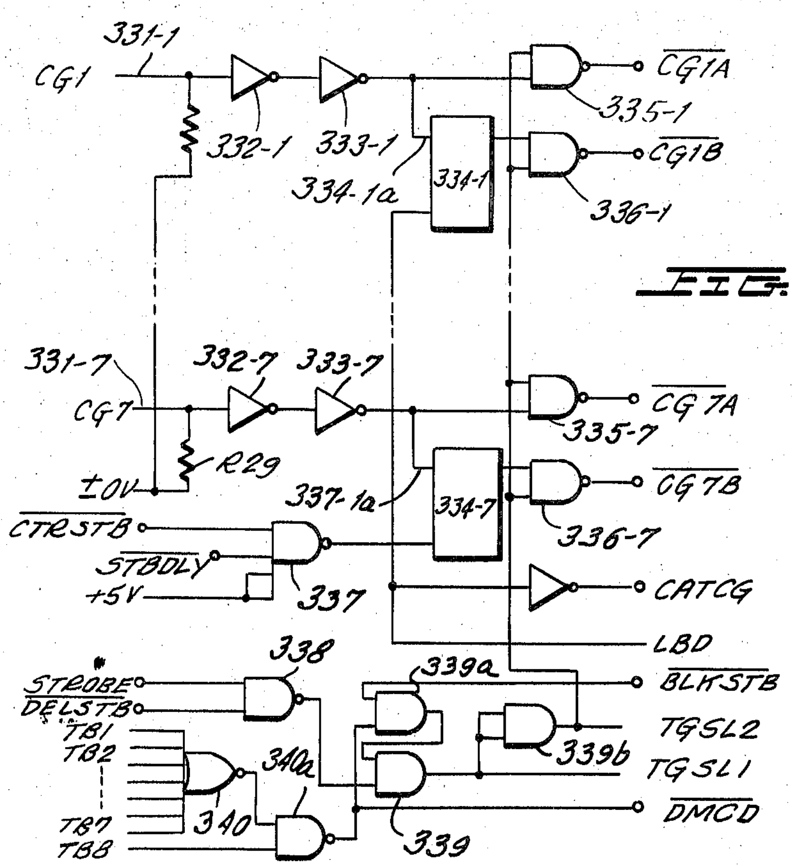

331-1
CG1
332-1
333-1
334-1a
334-1
CG1A
335-1
CG1B
336-1
331-7
332-7
333-7
CG7
R29
±0V
337-1a
334-7
CG7A
335-7
CG7B
336-7
CTRSTB
STBDLY
+5V
337
CATCG
LBD
338
339a
STROBE
DELSTB
TB1
TB2
TB7
TB8
340
340a
339
339b
BLKSTB
TGSL2
TGSL1
DMCD

FIG. 3d

FIG. 4a.

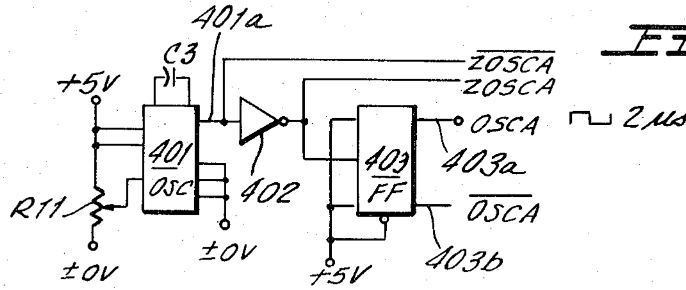


FIG. 4b

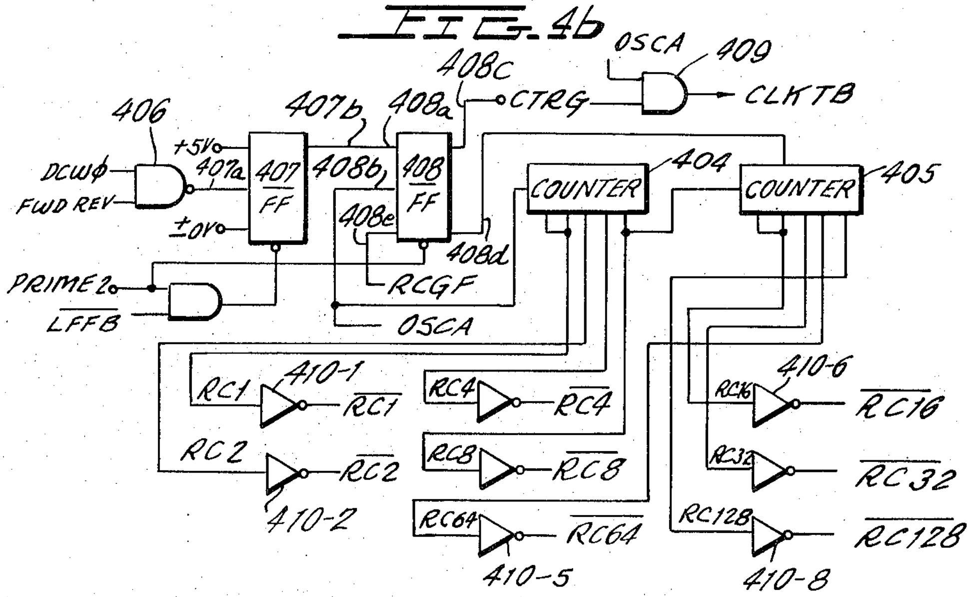


FIG. 4c.

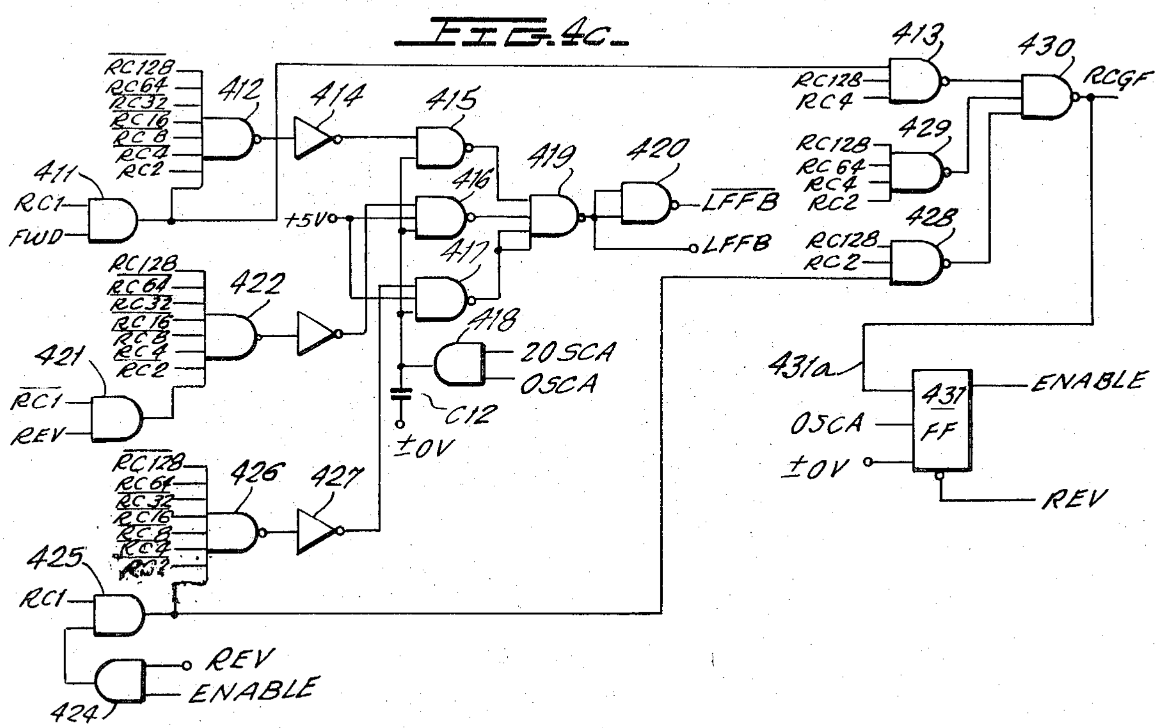


FIG. 4e

VIDEO STROBE TIMING

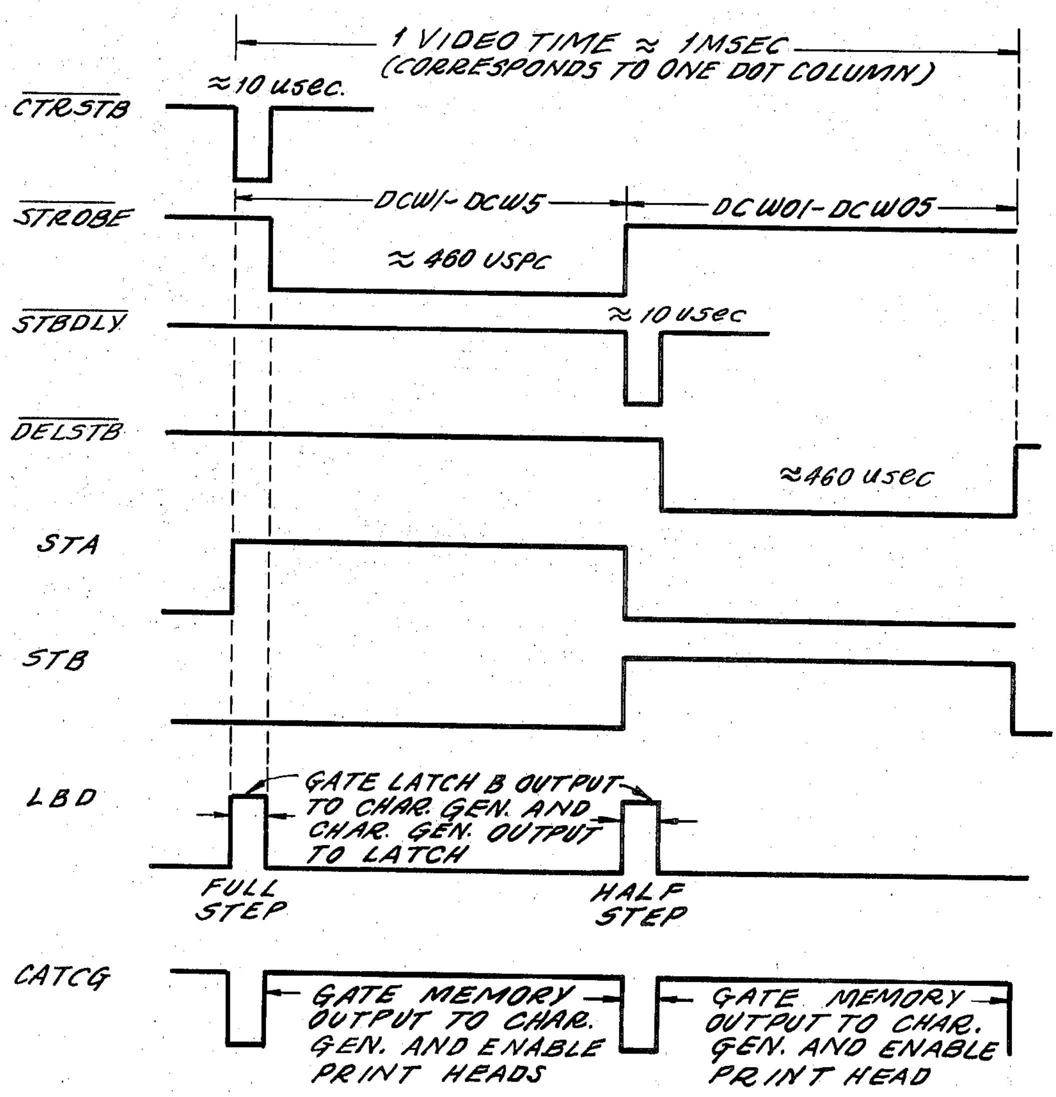


FIG. 4g.

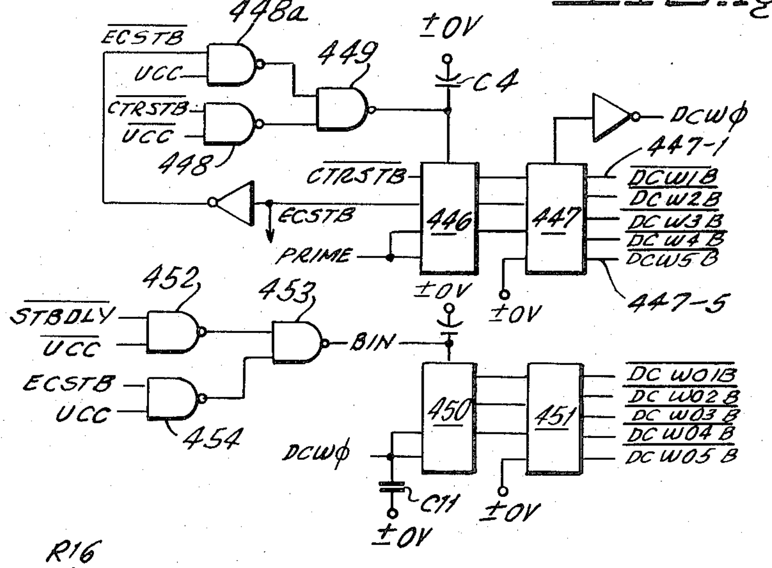
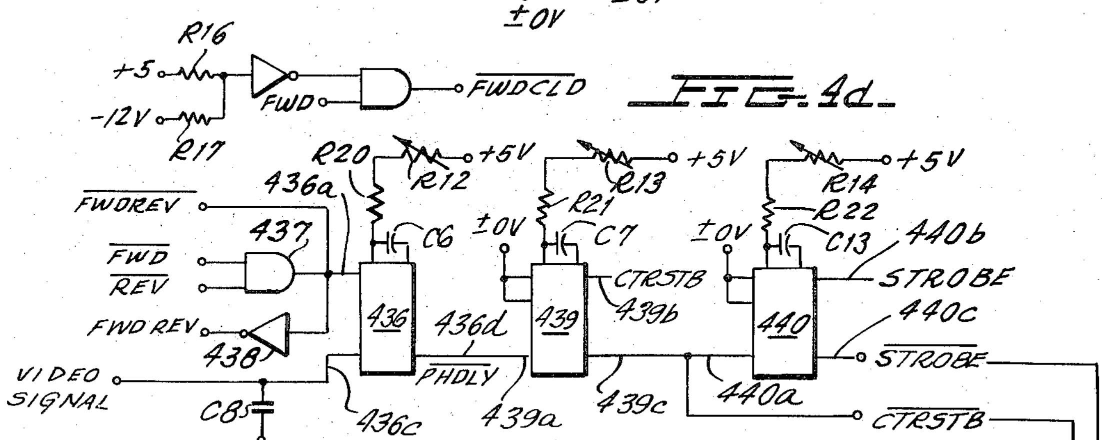


FIG. 4d.



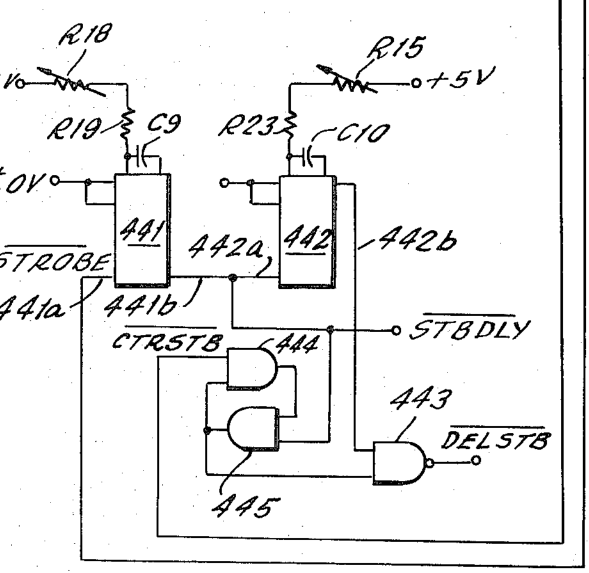


FIG. 4j.

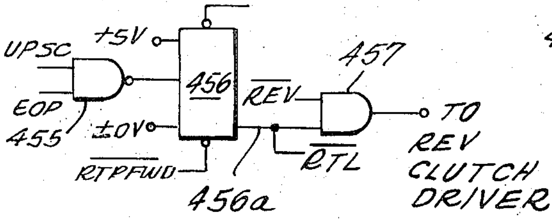


FIG. 4K.

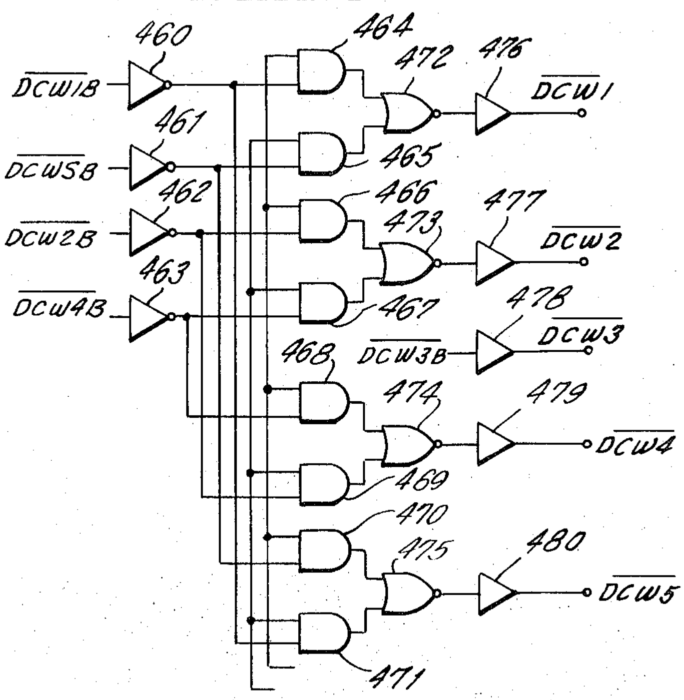


FIG. 4h.

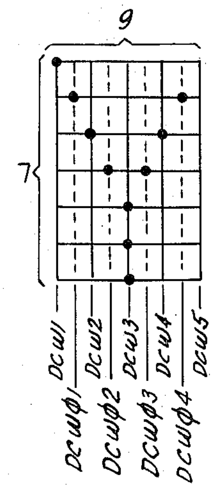


FIG. 4m.

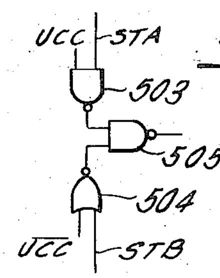
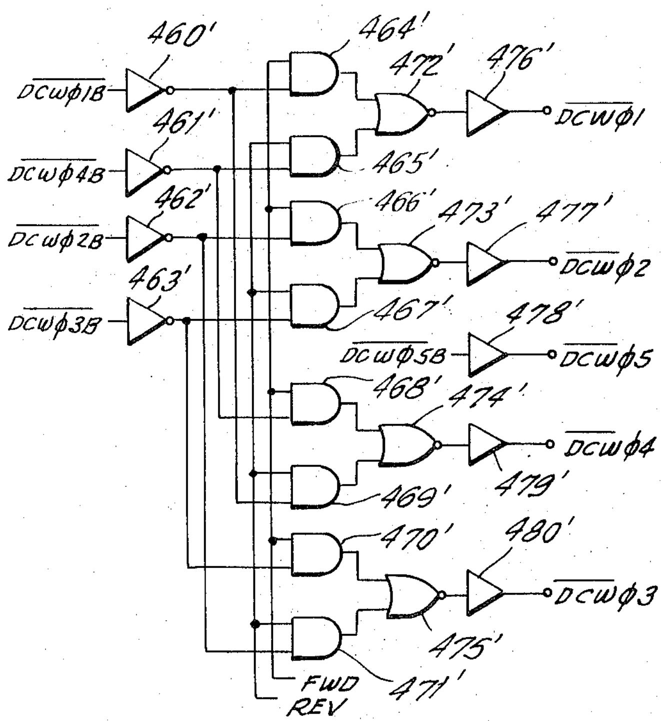


FIG. 4l.



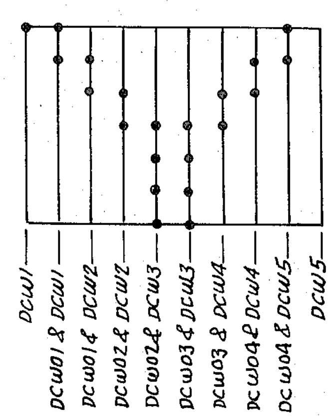


FIG. 4i.

FIG. 4f.

CHARACTER GENERATOR TIMING

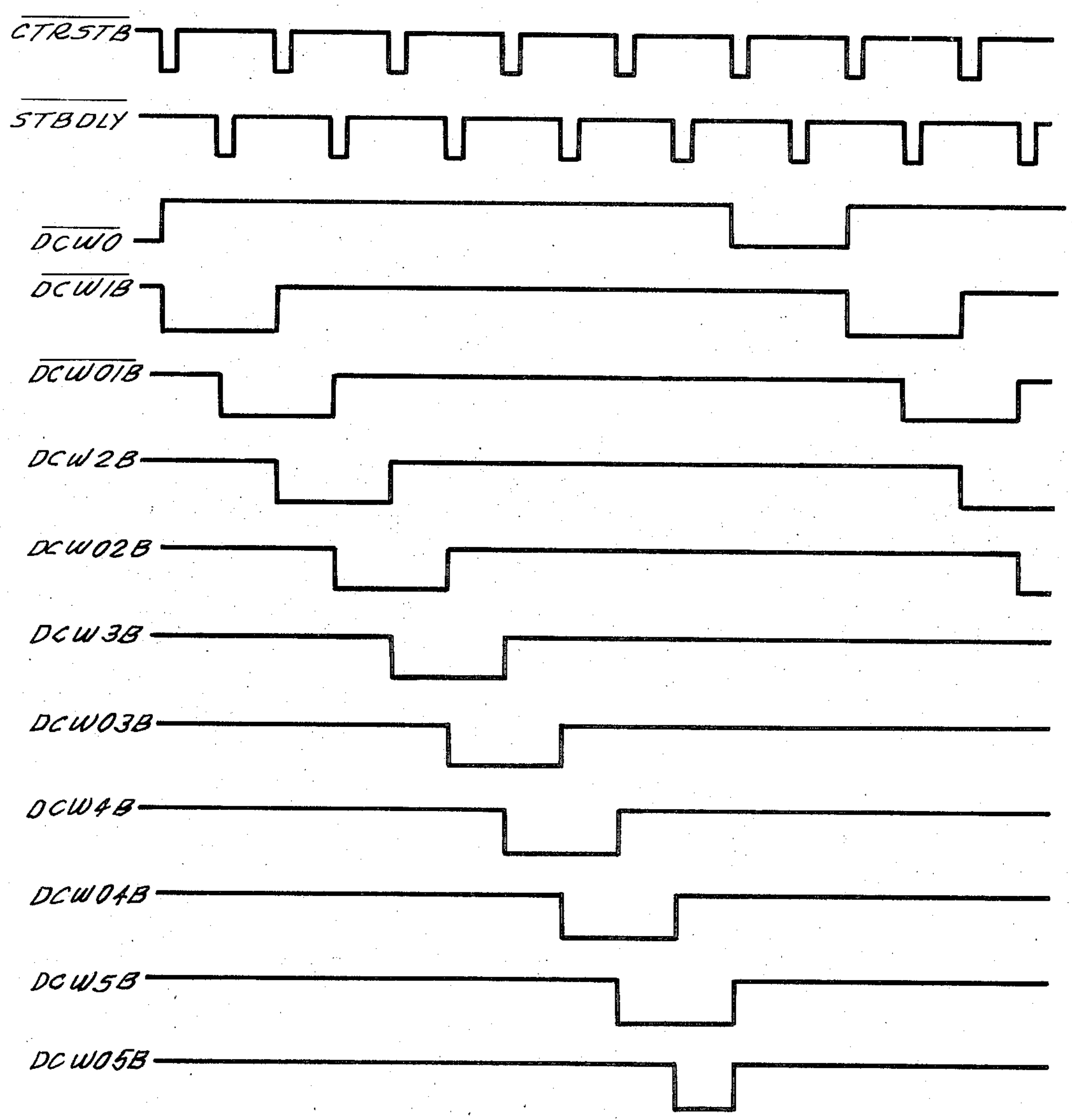


FIG. 5a

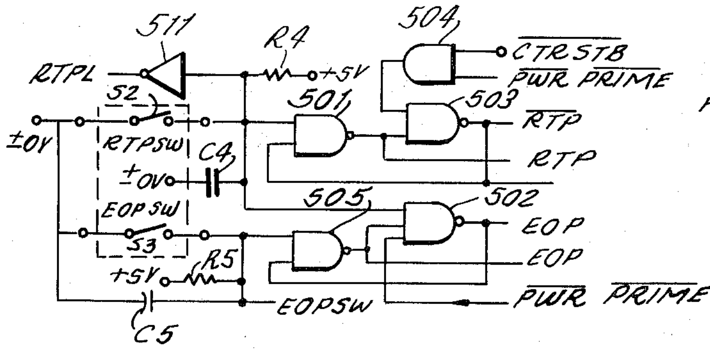


FIG. 5b

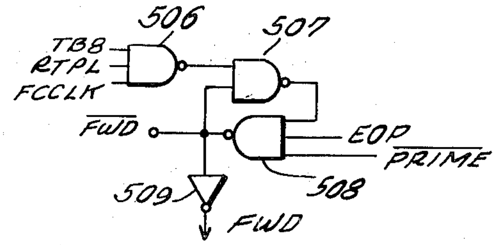


FIG. 5c

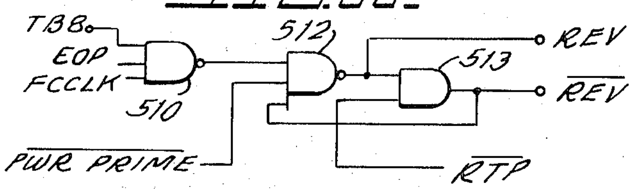


FIG. 5d

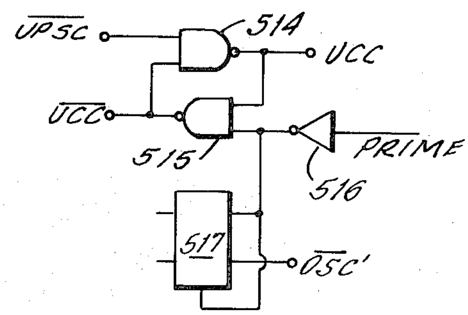


FIG. 6a

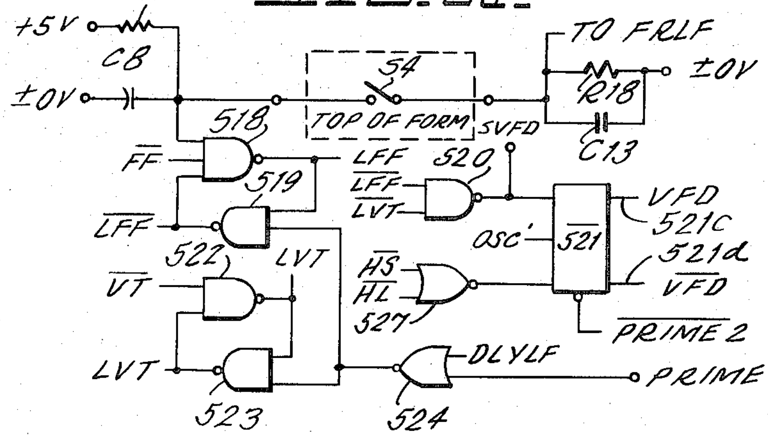
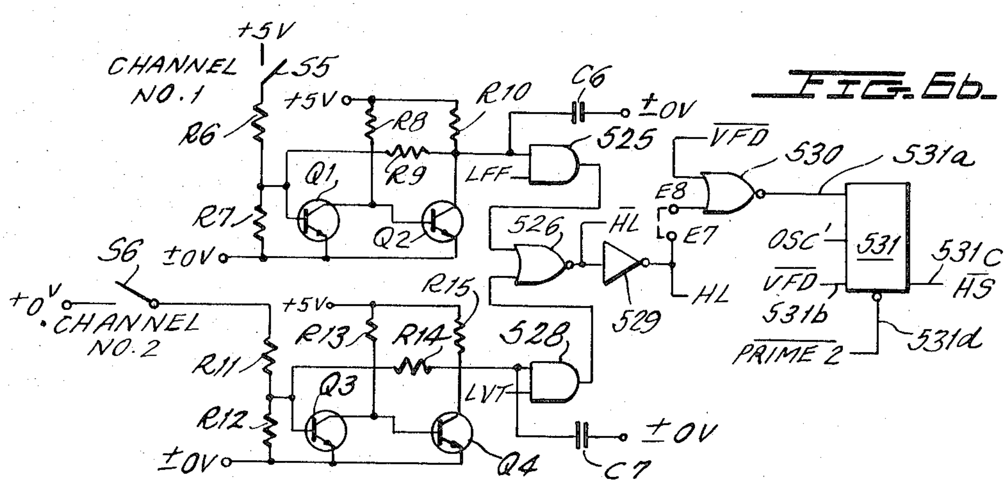


FIG. 6b



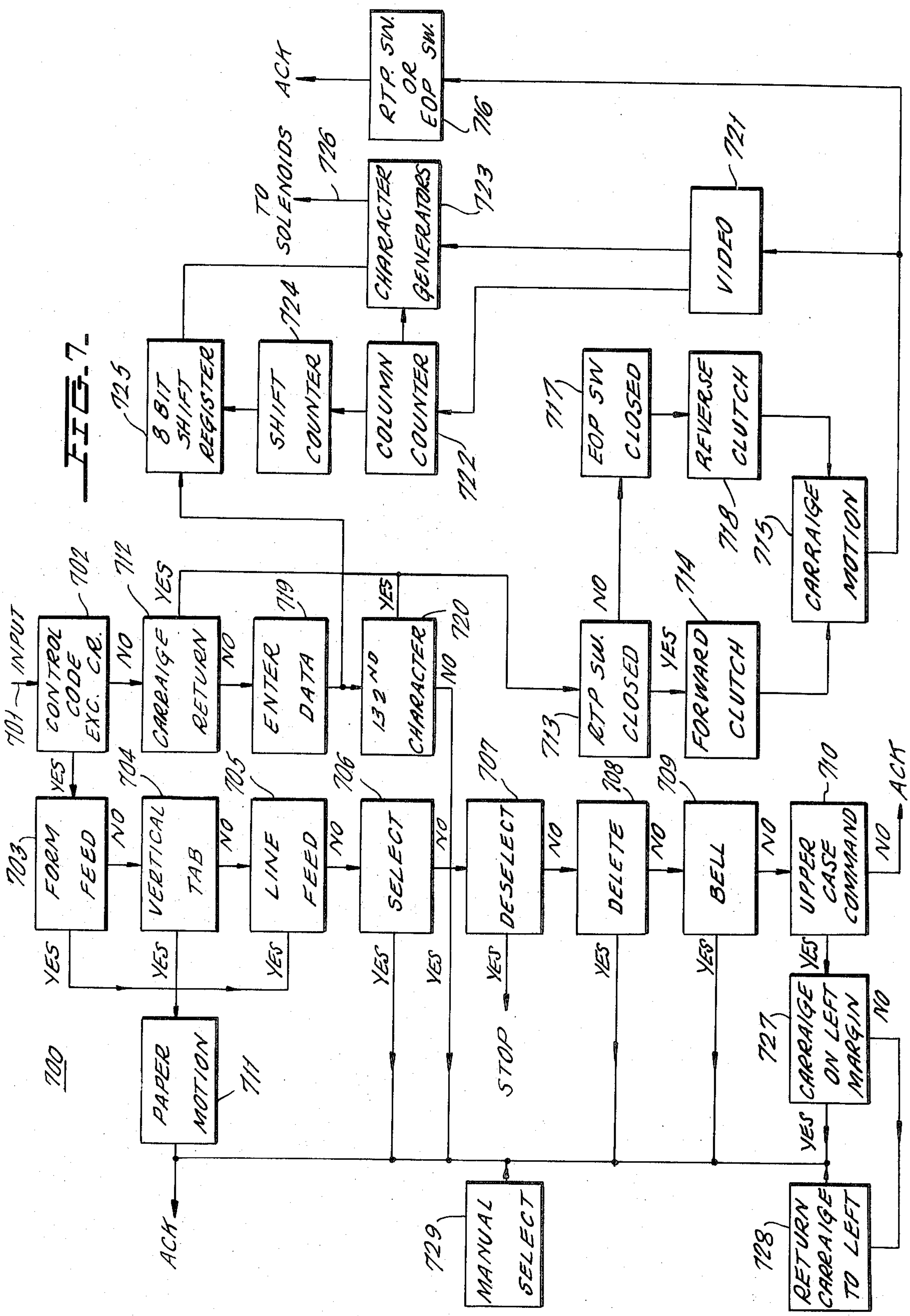

700
701 INPUT
CONTROL CODE EXC. CR. 702
CARRAIGE RETURN 712
ENTER DATA 719
132ND CHARACTER 720
8 BIT SHIFT REGISTER 725
SHIFT COUNTER 724
COLUMN COUNTER 722
CHARACTER GENERATORS 723
TO SOLENOIDS 726
RTP. SW. OR EOP SW. 716
ACK
VIDEO 721
EOP SW CLOSED 717
REVERSE CLUTCH 718
CARRAIGE MOTION 715
RTP SW. CLOSED 713
FORWARD CLUTCH 714
FORM FEED 703
VERTICAL TAB 704
LINE FEED 705
SELECT 706
DESELECT 707
DELETE 708
BELL 709
UPPER CASE COMMAND 710
CARRAIGE ON LEFT MARGIN 727
RETURN CARRAIGE TO LEFT 728
PAPER MOTION 711
MANUAL SELECT 729
STOP
ACK
YES
NO

FIG. 7.

BIDIRECTIONAL DUAL HEAD PRINTER

The present invention relates to line printers and more particularly to a novel multiple head line printer device wherein the heads are arranged in spaced fashion and are simultaneously performing print operations as well as being capable of printing in both the forward and reverse feed directions.

BACKGROUND OF THE INVENTION

Wire matrix printers are becoming increasingly more important and more useful in the field of high-speed document printing. Printers of this type are extremely advantageous for use in conjunction with computers, data terminals, communication systems and the like, wherein it is desired to provide a print-out of the data either received or converted and compiled by a computer.

One extremely advantageous wire printer of the dot-matrix type is described in U.S. Pat. No. 3,703,949 issued Nov. 28, 1972 and assigned to the assignee of the present invention. The wire matrix printer described therein is comprised of a carriage assembly which supports a print head assembly carrying a plurality of solenoid driven print wires. The print head assembly, including the solenoid drivers, is moved transversely across a paper document, usually at a constant rate of speed. The arrangement of the print head assembly is such as to provide a lightweight compact structure and to minimize the mass which is moved across the paper document, enabling the structure to move at relatively high speed. The location of the print head assembly at any given instant is detected by a position read-out or registration assembly which permits print-out at any given location regardless of the speed at which the print head assembly is being moved and, even deviations of the speed of movement will not affect or reduce the registration quality.

The print head assembly is arranged preferably so as to align the print wires which impact the paper document along an imaginary straight line which is typically arranged in vertical fashion. The print head assembly moves from left to right in the printing phase with the solenoids being selectively operated so as to print any combination of "dots" upon the paper document, which dots are typically formed by causing the free ends of the print wires to be impacted against an inked ribbon so as to form dot patterns upon the paper document. Combinations of the dot patterns (i.e., vertical rows of the dot patterns) cooperatively represent a character or other symbol. The printer described in the above-mentioned United States patent is capable of printing up to 132 characters per line of print. Upon the completion of printing of a line, the print head is moved from the right toward the left, preferably at a "carriage return" speed which is greater than the speed at which the print head assembly is moved during the print operation. This time interval thus constitutes a "dead" time interval since no printing occurs during a "carriage return" operation.

Although the aforementioned wire matrix printer provides reasonably good operating speeds, continued efforts have been made to improve the state of the art in order to advance printing speeds measurably. The wire matrix printer of the above-mentioned U.S. Pat. No. 3,703,949 is capable of printing a line of 132 characters at a rate of the order of **60** lines per minute (for full 132 character lines). Whereas this operating speed may be useful for certain applications, it is still nevertheless desirable to provide a capability of printing at ever increasing speeds.

BRIEF DESCRIPTION OF THE INVENTION

The present invention is characterized by providing a novel multiple print head wire matrix printer which retains all of the advantageous features of the single print head printer embodied in the aforementioned U.S. Pat. No. 3,703,949 but, due to its significantly increased capability, is capable of printing at speeds of 125 lines per minute for full 132 character lines, which is an output speed more than double that of the printing capabilities of the wire matrix printer disclosed in the above-mentioned U.S. Pat. No. 3,703,949.

The printer of the present invention is comprised of a printer housing having means movably mounting at least first and second print head assemblies which are moved in a direction transverse to the direction of feed of the paper document and which are moved simultaneously so as to affect the simultaneous operation of the plurality of print head assemblies. In the preferred embodiment incorporating first and second print head assemblies (i.e., in the dual head printer), each print head operates to print one-half of a line of characters. In operation, the dual print heads are initially moved to their left-hand most positions and move from left to right as the printing operation of the first line of characters is initiated. As soon as the dual print heads reach their extreme right-hand most positions, a paper feed operation is performed, causing the paper document to be advanced in preparation for printing the next line of characters. At this time, the dual head assemblies are moved toward the left from their right-hand most positions and printing of the second line of characters is initiated as the dual heads move from the right toward the left. It can thus be seen that printing occurs in both directions, eliminating the need for a "carriage return" operation. In this manner, every "odd" line of characters is printed by moving the dual head assemblies from left toward the right while every even (interspersed) line of characters is printed by moving the dual head assemblies from the right toward the left.

Even greater operating speeds may be obtained through the use of the same concept and by increasing the number of individual print head assemblies to a number greater than two thus even further enhancing operating speeds.

The printer of the present invention, in order to assure absolute registration of each vertical column of dots printed by each of the print head assemblies, employs a registration means which is comprised of a registration strip having a plurality of substantially equispaced narrow substantially transparent slits. The registration strip is mounted in a stationary fashion and has a length which is physically about one-half the length of the line of characters about one-half the length of the line of characters to be printed. The number of slits provided in the registration strip is of a magnitude approximately equal to at least one-half the total number od characters which may be printed on a line multiplied by the number of vertical dot patterns employed to represent any given character. In one preferred embodiment, each print head assembly is provided with seven slender print wires whose impact ends are arranged along a vertically aligned imaginary straight line. Nine closely spaced vertically aligned dot patterns cooperatively form each character or symbol with the dots of the 9x7 matrix being selectively formed to represent any given character or symbol. Since the vertically aligned dot columns are very closely spaced to one another, it is not possible, as a practical matter, to provide vertically aligned transparent slits in the registration strip with such close spacing. As an alternative therefore, the registration strip is provided with only five closely spaced vertically aligned transparent slits for each character with the slits being sufficient in number to control the printing of five of the nine columns employed to form each character. The electronics of the printer, however, is designed to provide for "half-step" printing whereby the electronic logic initiates formation of vertical dot columns at "half-step" locations between the five registration slits. Thus, it is possible through the system logic to create "half-step" dot patterns at four positions interspersed between the five registration slits to create a 7-row by 9-column matrix of dots with those particular dots selected being adapted to represent any desired character of symbol.

The printer electronics includes shift register means having a capacity sufficient to store up to 132 characters or other symbols plus a dummy character. After the shift register is loaded with the dummy character and the number of characters to be printed for a particular line (either 132 characters or some lesser quantity) means are provided for shifting the characters in the shift register, which is of the recirculating type, a sufficient number of places so as to move the binary code representing the first character to be printed by the right-hand print head assembly (i.e., the print head assembly which is designed to print the right-hand portion of a line of characters) into the right-hand most stage of the shift register. In the recirculating mode of the shift register all those characters which pass out of the right-hand most stage of the shift register are reinserted into the left-hand most stage so that all of the characters originally loaded into the shift register are retained therein at least until a full line of characters is printed. The binary coded combination now in the right-hand most stage of the shift register is then applied to a buffer stage to temporarily store this first character. Immediately thereafter, the shift register then undergoes a sufficient number of shift operations so as to place the binary coded representation of the first character to be printed by the left-hand print head assembly (i.e. the print head assembly adapted to print the left-hand half of a line of characters) into the right-hand most stage of the shift register.

The coded representation for the character to be printed by the right-hand print head assembly is transferred from temporary storage to the character generator for generating the left-hand most or first dot column for that character without erasing the character from the temporary storage. The information developed by the character generator representing the first dot column to be printed by the right-hand print head assembly is temporarily stored in a second buffer means. Thereafter, the coded representation of the character to be printed by the left-hand print head assembly and which is located in the right-hand most stage of the shift register is then applied to the full-step character generator causing it to develop the first dot column pattern for the character to be printed by the left-hand print head assembly. The output of the character generator at this time, simultaneously with the output of the character generator just previously stored is simultaneously caused to enable both left and right-hand print head assemblies to print the first or left-hand most dot column for the first character to be printed by each of these print head assemblies. This completes the first full step dot column.

Immediately thereafter and between the first two adjacent vertically aligned registration slits, the timing of the system logic causes the binary coded representations of the first character to be printed by the left and right-hand print head assemblies to be sequentially applied to the "half-step" character generator which causes the dot column pattern for the first half-step dot column of the right-hand character to be printed to be generated by the half-step character generator and temporarily stored in the second buffer means. Immediately thereafter, the binary coded representation of the character to be printed by the left-hand print head assembly and which is stored in the right-hand most stage of the shift register, to be applied to the "half-step" character generator. The first half-step vertical dot patterns are then simultaneously applied to the print head assemblies to develop the first half-step dot column pattern. This technique is repeated for the four remaining "full-step" dot patterns and the three remaining "half-step" dot patterns thereby completing the simultaneous printing of the first character of both the right and left print head assemblies. The shift register is then shifted the appropriate number of steps to shift the binary coded representations of the second characters or symbols to be printed by the left and right-hand print assemblies to again cause the printing of the second character by each print head assembly. This operation is repeated until both of the left and right-hand print head assemblies complete the printing of an entire line. After completion of the first entire line, the right-hand-most print head assembly will have moved to the extreme right-hand end of the paper document while the left-hand print head assembly will have moved to a location substantially equal to half the width of a full line of characters on the paper document. At this time, the shift register will be operated so as to permit the dual head assemblies to print the next line of characters while the print head assemblies move from the left to the right, thereby totally eliminating the need for a conventional "carriage return" operation which, for example, is the type of operation employed in the aforementioned U.S. patent.

In printing operations wherein the plurality of print head assemblies move from the right toward the left, the shifting operation imposed upon the shift register is substantially the same in nature as the shifting operations imposed upon the shift register in cases where the plurality of print head assemblies move from left to right. However, the logic of the system is adapted to automatically transfer dot column patterns in the reverse order during printing operations in which the plurality of print head assemblies move from the right to the left. Thus, the binary coded representations of the characters or symbols to be printed are transferred to the full and half-step character generators in the same manner as was previously described. However, the distinction in printing with the print head assemblies moving from right to left is such that the right-hand most dot column patterns of the characters to be printed by the print head assemblies are the first dot column patterns to be transferred to the print head assemblies, therefore the dot column patterns for the characters to be printed by the print head assemblies are transferred to the print head assemblies in the reverse order from that employed during printing operations in which the print head assemblies move from the left to the right. The electronic logic of the system is such as to immediately recognize the direction of movement of the print head assemblies in order to automatically and properly transfer the appropriate dot column pattern to the print head assemblies.

Regardless of which direction the print head assemblies move, each "full-step" dot column pattern is printed when the registration system detects the presence of a transparent registration slit. The electronics of the system functions to control the printing of each "half-step" dot column pattern which necessarily will be positioned between a pair of adjacent transparent registration slits representative of "full-step" dot column positions. The registration system further includes a light source and a light sensitive detector mounted upon the carriage assembly which moves the plurality of print head assemblies. A signal is generated by the movement of the optical pickup head and light source moving across the vertically aligned registration strip which consists of a series of alternately transparent and opaque slots. At each transparent slot the signal developed is amplified and shaped to generate a strobe pulse that initiates the timing for the printing of each character. The strobe pulses are counted (there are six pulses per character) and a decoder provides a plurality of individual states which are employed for the dotcolumn positions of the dot matrix. The strobe also undergoes a delay to develop a signal called "delay strobe" which enables the time sharing between two character generators. This allows the dot column patterns in the "half-step" positions to be inserted between the five "full-step" positions to provide better definition in character formation.

The carriage assembly is slidably mounted upon guide means and is provided with means for supporting and accurately positioning the plurality of print head assemblies upon the carriage assembly. Various adjustment mechanisms are provided for each print head assembly to assure its correct alignment, as well as its alignment relative to the other print head assemblies. The driving force for the carriage assembly consists of a closed loop belt drive wherein the timing belt is entrained about a drive pulley and a driven pulley with the free ends of the timing belt being fixedly secured to opposite ends of the carriage assembly to thereby form a closed loop for the timing belt. Single motor means are employed for driving the carriage assembly in both the forward and reverse print directions with clutch means being provided to move the carriage assembly alternatively in the forward and reverse directions as each succeeding line of characters is completed. An electromagnetic brake means is employed for abruptly terminating the movement of the carriage assembly as it arrives at each of its extreme left and right-hand most positions.

The single motor means is further employed as the driving means for imparting all other forms of mechanical or physical motion such as, for example, paper feed (i.e., line feed), form feed and ribbon feed.

It is therefore one primary object of the present invention to provide a high speed impact printer of the dot matrix type employing a plurality of simultaneously operating print heads which cooperatively function to print each line of characters.

Another object of the present invention is to provide a novel impact printer of the dot-matrix type in which printing is performed by the print head assemblies regardless of the direction in which the print head assembly is moving as as to totally eliminate the need for conventional "carriage-return" operations.

Still another object of the present invention is to provide a novel high-speed impact printer of the dot-matrix type in which "half-step" dot patterns may be generated to significantly improve the resolution of characters or other symbols to be printed.

Still another object of the present invention is to provide a novel high-speed impact printer of the dot-matrix type employing a simplified and yet highly reliable mechanical driving means for the rapid and accurate movement of the print head assemblies, as well as for performing all other mechanical functions such as paper feed and ribbon feed operations.

BRIEF DESCRIPTION OF THE FIGURES

The above as well as other objects of the present invention will become apparent when reading the accompanying description and drawings in which:

FIG. 1 is a perspective view of a printer incorporating the principles of the present invention.

FIG. *2a* – *2q* show schematic diagrams of logical control circuitry employed to operate the printer of FIG. 1.

FIGS. *3a* – *3d* is a logic circuit diagram which shows the circuits for storing data to be printed by the printer of of FIG. 1.

FIG. *3b* shows a logic diagram of the latch circuits for temporarily storing the character to be ultimately transferred to the right hand print head.

FIG. *3c* is a logic diagram showing the character generators used to generate "full" and "half" step dot column patterns.

FIG. *3d* shows the latch circuitry for temporarily storing the dot column pattern used to operate this right-hand print head.

FIGS. *4a*–*4d*, *4h* and *4k*–*4m* logical circuit diagrams of the circuitry employed to control the operation of the shift register, character, generators and latch circuits of FIGS. *3a*–*3d*.

FIGS. *5a*–*5d* are logic diagrams of the logical circuitry employed to control print head movement.

FIGS. *6a* and *6b* are logic diagrams showing the logical circuitry employed to control paper document movement.

FIG. 7 shows a flow diagram of the operation of the printer of FIG. 1 and its logical circuitry.

DETAILED DESCRIPTION OF THE FIGURES

FIG. 1 shows a simplified version **100** of the printer which comprises first (A) and second (B) print head assemblies **101** and **102** mounted upon carriages **103** and **104** respectively, which, in turn, are mechanically joined by coupler **105** so as to move in unison. Each print head assembly is provided with seven solenoids each utilized to selectively print seven vertically aligned dots. Copending application M–7127 shows a typical print head construction. The carriages are secured to a closed loop timing belt **106** as shown at **107**. Belt **106** is driven by a motor M whose output is selectively coupled to belt **106** by either forward clutch **108** or a reverse clutch **109.**

An inked ribbon **110** is positioned in front of both print heads **101** and **102** and spans paper document **111.** The selective energization of solenoids S of the two print heads causes the ribbon to inpact the paper document **111** and form the dot column patterns.

The print heads each form characters or other symbols, each printing nine dot columns which collectively form a character. The carriages **103–104** ride along guide tracks **112** (only one is shown in FIG. 1) in moving in the forward and reverse directions.

The registration or accurate placement of the dot columns is assured by a photo-sensing device comprised of a light source and phototransistor (not shown) which cooperates with a registration strip **113** having vertical slits **113***a*. The light source and phototransistor are positioned on opposite sides of registration strip **113** to generate "video" pulses whenever they are aligned with one of the slits **113***a* to permit "full-step" dot columns to be printed. "Half-step" dot columns are printed in between adjacent slits **113a** under the control of a logic circuit to be more fully described.

The paper document is moved in the direction of arrow **114** by pin feed mechanism **115** and **116** under control of form feed, line feed and top of form signals to be more fully described. The pin feed mechanisms are selectively coupled to the motor M through clutch mechanisms (not shown for purposes of simplicity) which are activated to provide the appropriate paper movement.

The printer, in addition to providing simultaneous operation of the print heads **101** and **102,** also provide for printing in the forward (left to right) direction, as well as the reverse (right to left) direction. Although the data representing the characters and other symbols to be printed is always entered into the printer member in the same order, logical circuitry is provided to assure that the correct dot column patterns are applied to the print heads regardless of the direction of movement of the print heads.

FIG. 3*a* shows the shift register **300** comprised of four register sections **301–1** through **301–4** which are cooperatively capable of storing **132** 8-bit data words plus a dummy character to provide a large plurality of character combinations representing characters, symbols and other special functions. It should be understood however that the register length (i.e., the number of stages and the number of registers) may be modified to be either greater or lesser in number than that specified hereinbelow to accommodate either more complex or simpler applications. The dummy character, which is a ONE at DS8, when detected at the output stage indicates that the register is full or that loading of the register with less than a full line of 132 characters has been completed.

Each data word is fed in in parallel at the inputs **302–1** through **302–8,** respectively. Input **303** serves as the input terminal for shifting each data word applied to input terminals **302** into the left-hand most stages of the shift register sections **301,** as will be described in more detail hereinbelow.

Since each of the register stages are substantially identical to one another, some of the stages have been omitted from FIG. 3*a* for purposes of simplicity, it being understood that their design and operation is the same. Considering register section **301–1,** it is capable of storing **133** pairs of bits and, upon the application of each shift pulse, loading the pair of bits of the data word applied to input terminals **302–1** and **302–2** into its left-hand most stage, while shifting all previously loaded pairs of bits one stage to the right. Shift register section **301–1** is provided with output terminals **304–1** and **304–2** for coupling the contents of its right-hand most stage to other circuitry. These output terminals are coupled, in turn, to respective amplifier stages **305–1** and **305–2,** respectively, whose outputs are simultaneously coupled to the output terminals TB1 and TB2, respectively, for coupling to the inputs of other electronic hardware to be more fully described and further for feeding back the pair of bits appearing in the right-hand most stage back to the left-hand most stage of the two-bit register section so as to provide a recirculating shift register. In this respect, the outputs of amplifiers **305–1** and **305–2** are coupled to leads **306–1** and **306–2,** respectively, which are coupled to the recirculation inputs **307–1** and **307–2,** respectively, for feeding back the contents of the right-hand most stage of the shift register into the left-hand most stage thereof. The input of an SRCL signal at terminal **308** is coupled to inputs **307–1** through **307–8** to operate the register in the recirculate mode. Clearing of the shift register is accomplished by loading space codes to clear all stages of the shift register **300** when it becomes necessary to do so, with the circuitry employed therefore to be more fully described hereinbelow.

FIG. 3*b* shows the buffer register employed for temporary storage of the data word to be ultimately employed for operating the right-hand or "B" print head assembly (in a manner to be more fully described). The buffer register **310** is comprised of 8 bistable flip-flop stages **311–1** through **311–8,** each being capable of storing one of the 8 binary bits transferred thereto from the right-hand most stage of shift register **300** shown in FIG. 3*a* by means of the output terminals **TB1-TB8,** respectively.

Since all of the bistable flip-flop stages are substantially identical in both design and operation, only one will be described herein in detail for purposes of simplicity. Also, it should be understood that some of the flip-flop stages have been omitted from FIG. 3*b* likewise for purposes of simplicity. The output terminal TB1 is sumultaneously coupled to input terminal **311–1***a* of bistable **311–1** and to one input of AND gate **312–1,** there being one such gate **312–1** through **312–8** associated with each of the remaining bistable stages. The remaining inputs of the stages **312–1** through **312–8** are coupled in common to lead **313** which receives the signal CATCG which is generated for a purpose to be more fully described hereinbelow.

Bistable **311–1** has its output **311–1***b* coupled to one input of AND gate **314–1,** there being a similar such AND gate **314–2** through **314–8** associated with each of the remaining bistables **311–2** through **311–8,** respectively. The remaining input of each of the gates **314** are coupled in common to lead **315** which receives signal LBD which is generated for a purpose to be more fully described.

The outputs of gates **312–1** and **314–1** are each coupled to respective inputs of OR gate **316–1** whose output is coupled to inverter stage **317–1** (noting that a similar OR gate and amplifier is provided for each of the remaining bistables **311–2** through **311–8,** respectively). The outputs of each of the inverters 317–1 through 317–8 appear at output terminals $\overline{CHADD1}$ – $\overline{CHADD8}$ for application of the output of the amplifiers to the respective input stages of the appropriate character generator circuits, as will be more fully described in connection with FIG. 3c.

In operation, the 8-bit data word appearing in the right-hand most stage of shift register 300 is coupled through outputs TB1–TB8 and is either passed by gates 312–1 through 312–8 when the signal CATCG is present so as to be passed through the respective OR gates 316 and amplifiers 317 and appear at outputs $\overline{CHADD1}$ – $\overline{CHADD8}$, or alternatively to be loaded into the bistables 311–1 through 311–8 in the presence of the signal LFFB which is selectively applied to terminal 318. Thus, the 8-bit word appearing in the right-hand most stage of shift register 301 is either passed directly to output leads $\overline{CHADD1}$ – $\overline{CHADD8}$ or is temporarily stored in bistables 311-1 through 311-8 and at some later time is gated out by LBD through gates 314 and 316 for a purpose to be more fully described hereinbelow.

FIG. 3c shows the "full-step" and "half-step" character generators 320 and 325, respectively. Each of these character generators have a first set of input terminals 320a–1 through 320a–6 and 325a–1 through 325a–6, respectively, a second set of input terminals 320b–1 through 320b–5 and 325b–1 through 325b–5; and a set of output terminals 320c–1 through 320c–7 and 325c–1 through 325c–7, respectively. Input sets 320a–1 through 320a–7 and 325a–1 through 325a–7 are coupled in common to the associated leads $\overline{CHADD1}$ through $\overline{CHADD7}$ as is shown. Input sets 320b–1 through 320b–5 and 325b–1 through 325b–5 are respectively coupled to input terminals $\overline{DCW1}$ through $\overline{DCW5}$ and $\overline{DCW01}$ to $\overline{DCW05}$ for receiving full-step and half-step dot column selection signals which are generated by the registration means in a manner to be more fully described. The character generators are basically read-only-memories of the MOS type capable of producing a 9×7 dot-matrix for a 64 character set. The timing pulse sets DCW1 through DCW5 and DCW01 through DCW05, respectively control the generation of the appropriate enabling signals for the print head assembly solenoids at each of the five "full-step" positions in the case of character generator 320 and at each of the four half-step positions in the case of the "half-step" character generator 325.

The six bits of information available from the buffer circuitry of FIG. 3b and which are applied to the inputs of the character generators 320 and 325 at 320a–1 through 320a–6 and 325a–1 through 325a–6 respectively, represent six binary bits which identify a character or other symbol. The character generators are adapted to provide binary information at their outputs 320c–1 through 320c–7 and 325c–1 through 325c–7 which represent the dots to be printed for a particular dot column. The dot column selected is determined by the timing pulses available at inputs 320–1 through 320b–5 and 325b–1 through 325b–5. Each timing pulse for the "full step" character generator is developed together with the presence of a registration slit, whereas each timing pulse for the "half step" character generator is developed a predetermined time delay period after the occurance of each registration slit and before the occurrence of the next registration slit, in order to provide for half-step printing.

The outputs 320–1 through 320c–7 and 325c–1 through 325c–7 of the respective full and half-step character generators are all coupled in common to the output leads CG1 through CG7 as shown. This common connection is possible due to the fact that only one of the two character generators will be developing a dot column pattern at any given instant, i.e., outputs 320c–1 to 320c–7 generates the "full" step dot patterns while outputs 325c–1 to 325c–7 generates the "half" step dot patterns.

Turning to a consideration of FIG. 3d there is shown therein the buffer circuits for simultaneously coupling the dot column patterns developed by the character generators to the printing head driving circuits.

As was described hereinabove, the dot column pattern for the right-hand or B head will be transferred first. This dot column pattern will be applied to input terminals 331–1 through 331–7. Each dot position signal passes through first and second inverters 332–1 through 332–7 and 333–1 through 333–7 which are connected in cascade. The outputs of the inverters 333 are each coupled simultaneously to one input 334–1a of a bistable flip flop 334–1 and to one input of a gate 335. The dot column pattern for the B head is loaded into bistables 334–1 through 334–7 upon the development of the LBD signal which is applied to the inputs of all of the bistables 334 when the dot column pattern is derived from the half-step character generator. The digital state of the bistable circuits appearing at the outputs 334–1b through 334–7b is applied to one input of a gate 336–1 through 336–7 when the signal DGSL1 is present.

The signal LBD is generated by the presence of either the strobe delay signal $\overline{(STBDLY)}$ or the center strobe signal $\overline{(CDRSTB)}$. These enabling signals are applied to gate 337 whereupon the dot column patterns for the B print head generated by the "full-step" and "half-step" character generators are applied to inputs 331–1 through 331–7 temporarily loaded into bistables 334–1 through 334–7 respectively.

The transfer of the "full-step" and "half-step" dot column patterns for driving the A print head occurs subsequent thereto whereupon the "full" and "half" step dot column patterns sequentially appear at inputs 331–1 through 331–7 and are passed by gates 335–1 through 335–7 upon the occurrence of the TGSL1 and TGSL2 signals which gate the dot column patterns through gates 335 simultaneously with the gating of the respective "full-step" and "half-step" dot column patterns for the B print head through gates 336. The TGSL signal is developed when either the strobe signal $\overline{(STROBE)}$ or the delay strobe signal $(\overline{DELSTB})$ are present at their respective inputs to gate 338, causing gate 338 to go high, which condition is applied to gate 339. When the coded character in the right-hand most stage of shift register 301 (see FIG. 3a) is binary zero in all of its positions TB1 through TB7 and is binary 1 in its 8th position TB8, i.e., is a dummy character, gates 340 and 340a apply a disabling level to the remaining input of gate 339 causing the output TGSL to be inhibited. This causes the dot column patterns for both the A and B print heads to be simultaneously disabled to driver amplifier circuits (not shown) which selectively drive the print wires of the A and B heads to form the dot column patterns developed by the character generator.

The CATCG signal is developed by inverter **341** which is coupled to the output of gate **337** so that when LBD is high, CATCG is low, and vice versa. As soon as LBD goes low, it causes the "full-step" and "half-step" dot column patterns for the B print head to be stored in the buffer bistable flip-flops **331–1** to **311–7** of FIG. 3*b*. This operation continues until all nine columns of a character has been printed by both the A and B heads.

FIGS. 4*a*–4*m* show the circuits employed for shift control operations of the counter and the means provided for controlling operation of the dot column patterns developed by the character generators.

FIG. 4*a* shows the system clock source which is comprised of a free-running multivibrator (FRM) **401** whose output **401***a* appears as a first output $\overline{\text{20SCA}}$ which is further inverted by inverter **402** into the signal 20SCA, both of which signals are complements of one another and which are twice the clock rate of the system. The output of inverter **402** is applied to a bistable flip-flop (FF) **403** whose outputs **403***a* and **403***b* develop the signals OSCA and $\overline{\text{OSCA}}$ which represent the system clock rate, bistable **403** functioning in this case as a frequency divider and dividing the output of the frequency rate of free running multivibrator **401** by one-half.

FIG. 4*b* shows the counter employed for remembering the positions occupied by the characters in the register **301,** shown in FIG. 3*a*. The counter is comprised of two four-bit counter stages **404** and **405.** The RC8 output stage of **404** is applied to the input of stage **405** as shown for incrementing counter stage **405** by one count. The counter stages **404** and **405** together form a counter capable of developing a total count of **256.** The counter is started by gate **406** which is enabled when the signal DCW0 is developed simultaneously with the signal FWDREV which is generated when the print head carriage has moved to either its extreme left-hand or right-hand position. The simultaneous presence of the DCW0 and FWDREV signals causes gate **406** to apply a clock pulse to the clock pulse input **407***a* of bistable J-K flip-flop **407.** The output **407***b* of bistable flip-flop **407** is caused to go high, which level is applied to input **408***a* of bistable J-K flip-flop **408,** whereby the next oscillator signal $\overline{\text{OSCA}}$ applied to clock pulse input **408***b* causes output **408***c* to go high and simultaneously causes output **408***d* to go low. Signal RCGF applied to input **408***e* of bistable **408** causes output **408***d* to go high during the occurrence of the next oscillator signal OSCA whereupon the counter stages **404** and **405** are cleared.

Output **408***c* of bistable **408** (i.e., signal CTRG) is ANDED with the oscillator (signal OSCA) to develop the shift pulse signal for the register **301** (signal CLKTB) through the provision of gate **409.** FIG. 3*a* shows signal $\overline{\text{CLKTB}}$ as being applied at input terminal **303** and simultaneously coupled to the shift input of each register stage **301–1** through **301–4** to shift all binary characters one position to the right and further to transfer the character shifted out of the right-hand most stage through the feedback paths **306–1** through **306–8.** The number of shifting operations which occur upon the completion of the printing of each character on a line and prior to initiating of the next character to be printed on that line are "remembered" and controlled by the counter **404–405.** The completion of the total number of shifting operations required during the aforesaid time interval causes the generation of the signal RCGF which terminates the shift pulses CLKTB and clears the counter stages **404–405** in readiness for the next sequence of shifting operations.

The logic utilized for control purposes in conjunction with counter stages **404–405** is shown in FIG. 4*c*. The invertor gates of FIG. 4*b*, designated as **410–1** through **410–8,** produce inverted outputs at each of the stages of counter **404–405.**

The logic of FIG. 4*c* comprises gate **411** whose output goes high upon the presence of signals FWD (indicating that printing in the "forward" direction is occurring) and RC1 (indicating that the count of one developed by counter stage **404**). This output is simultaneously applied to gates **412** and **413.** Gate **412** is normally high until all of its inputs go high, at which time the output of gate **412** goes low. This occurs only upon the development of the binary equivalent of the decimal count **67** in counter **404–405.** The output of gate **412** is inverted at **414** to be applied to one input of gate **415.**

Gate **421** has its output go high during printing in the reverse (i.e., the right to left-hand printing) direction as indicated by the presence of signal REV together with the absence of signal RC1, (hence, during the presence of $\overline{\text{RC1}}$). The output of gate **421** is applied to gate **422** whose output is normally high until all of its inputs go high, at which time the output of gate **422** goes low. Gate **422** goes low when counter **404** has developed the binary equivalent of the decimal count 132 indicating that 132 shift operations have taken place in register **301.** The output of gate **422** is inverted at **423** and applied to one input of gate **416.**

Gate **424** has its output go high during the presence of both the ENABLE signal and the REV signal. The output of gate **424** is applied to gate **425** which goes high when the RC1 signal is present. The output of gate **426** is simultaneously applied to one input of gates **426** and **428.**

The output of gate **426** is normally high until all of its inputs go high. This occurs when counter **404–405** accumulates **65** oscillator pulses. The output of gate **426** is inverted at **427** and applied to one input of gate **417.** Gate **418** enables all of gates **415, 416** and **417** during the occurrence of the signals $\overline{\text{OSCA}}$ and $\overline{\text{2OSCA}}$.

Since gates **412, 422** and **426** are normally high except during the respective counts of **67, 132** and **65** by counter **404,** then all of these gate outputs are applied as low levels to gates **415, 416** and **417,** respectively. Thus, the outputs of gates **415–417** will remain high regardless of the enabling signal applied thereto by gate **418.** Gate **419** will have its output low with the simultaneous presence of high levels at its inputs which are coupled at gates **415–417.** The output of gate **419** (signal LFFB) is thus absent except during the times when counter **404–405** has accumulated 67, 132 or 65 oscillator pulses respectively. The output of gate **419** thus prevents loading of the flip-flops for the B head except during the occurrence of either 67, 132 or 65 oscillator pulses. Note FIG. 3*b* wherein input **318** is coupled to the output of gate **419.** The output of gate **419** is further coupled through inverter **420** to develop the complementary signal $\overline{\text{LFFB}}$.

Assuming movement of the print heads in the forward direction, as soon as counter **404** has developed a decimal count of 67, indicating that the 67th character is in the right-hand most stage of register **300,** the output of gate 412 will go low, which level is applied in inverted form at 414 to the input of gate 415 causing its output to go low when the enabling pulse developed by gate 418 is generated. With one of the outputs of gate 419 going low, the output of gate 419 goes high to develop the signal LFFB which permits the coded character in the right-hand most stage of register 301 to be shifted into the flip-flop stages 311-1 to 311-8 of FIG. 3*b*.

Gate 413 has its output normally high until its inputs are all high, at which time its output goes low. Gate 413 is normally high until counter 404 has developed a decimal count of 133, at which time its output goes low.

Gate 429 operates in a similar fashion wherein its output will go low after counter 404 has developed a decimal count of 198. Gate 428 will also have its output go low when counter 405 has accumulated a decimal count of 131 oscillator pulses. Thus the outputs of gates 413, 429 and 428 are normally high causing the output of gate 430 (signal RCGF) to be low. As soon as one of the three aforementioned counts are accumulated in counter 404 any of the respective gates 413, 429 or 428 will go low causing the output of gate 430 to go high whereupon flip-flop 408 will be reset by the signal RCGF (see FIG. 4*b*) to clear counter 404 and terminate the shift pulses CLKTB. This signal is also applied to one input of bistable flip-flop 431 which develops an ENABLE signal at 431*c* when its input 431*a* goes high, and, upon the occurrence of the next oscillator signal OSCA at input 431*b*. The ENABLE signal is utilized by gate 424 during printing in the "reverse" direction.

FIG. 4*d* shows the circuitry employed for developing the STROBE and DELAY STROBE pulses which control the "full step" and "half step" printing operations. As the printer head carriage moves, the optical pick-up head and light source (see FIG. 1) generates the video signal for controlling the print timing. Only the right-hand half of the timing fence contains vertical timing slots. As the right print head (B) and optical head assembly moves across the timing fence, these slots interrupt the light to the optical pick-up head, generating a video signal. The signal is applied to trigger one-shot multivibrator 436 which initiates the print timing shown in FIG. 4*e*.

The timing is sub-divided into a space interval (DCWO), five full step intervals (DCW1B–DCW5B) and five half-step intervals (DCW01B–DCW05*b*). When the print heads are moving in the forward direction, the dot columns are retrieved from the character generator in a left-to-right sequence. When the heads move in the reverse direction, the dot columns are retrieved in the reverse order (i.e. right-to-left). Since the generator columns are specified by signals DCW1–DCW5, and DCW01–DCW05, these control signals are noted differently, depending on the direction of print head movement. FIG. 4*f* illustrates the distinction.

Turning to a consideration of FIG. 4*d*, when the printer operates in either the forward or the reverse direction, one of the inputs to gate 437 will be low causing the output of gate 437 to go low. The input appears as the $\overline{\text{FWDREV}}$ signal and is further inverted by the invertor gate 438 to generate the signal FWDREV. The output of gate 437 is applied to input 436*a* of one-shot multivibrator 436 enabling the one-shot multivibrator 436 to be triggered by video signals applied at its input 436*c*. The one-shot multivibrator generates an output at 436*d* which is applied to the trigger input 439*a* of one-shot multivibrator 439 whose output 439*b* generates the signal CTRSTB and whose output 439*c* generates the signal $\overline{\text{CTRSTB}}$ (see FIG. 4*e*). Output 439*c* is coupled to the trigger input 440*a* of one-shot multivibrator 440 whose output 440*b* develops the signal STROBE and whose output 440*c* develops the signal $\overline{\text{STROBE}}$. Output 440*c* is further coupled to trigger input 441*a* of one-shot multivibrator 441 whose output 441*b* develops the signal $\overline{\text{STBDLY}}$ (strobe-delay). This output is coupled to trigger input 442*a* of a one-shot multivibrator 442 whose output 442*b* is coupled to one input of gate 443. Output 439*c* is coupled to one input of gate 444, output 442*a* is coupled to one input of gate 445. Gates 444 and 445 are coupled to form a latch circuit. The signal $\overline{\text{CTRSTB}}$ (FIG. 4*e*) is utilized to cause the dot column pattern for the B print head to be generated and stored in the latch flip-flops 311-1 through 311-7. The signal $\overline{\text{STROBE}}$ causes simultaneous firing of the solenoids for the A and B print heads. The signal $\overline{\text{STBDLY}}$ (Strobe Delay) causes the half-step dot column patterns to be temporarily stored in the latch flip-flops 311-1 through 311-7 while the signal $\overline{\text{DELSTB}}$ causes the simultaneous firing of the solenoids for both A and B print heads.

During normal printing, timing signals $\overline{\text{DCW1B}}$ through $\overline{\text{DCW5B}}$ are generated by a divide-by-six counter 446 and a decoder 447 shown in FIG. 4*g*. With the signal UCC low and the signal $\overline{\text{UCC}}$ high (indicating no elongated characters are requested), gate 448 and gate 449 enables counter 446 to be clocked by video STROBE pulse $\overline{\text{CRSTB}}$.

Similarily, signals $\overline{\text{DCW01B}}$ through $\overline{\text{DCW05B}}$ are generated by divide-by-six counter 450 and decoder 451. With the signal UCC low and the signal $\overline{\text{UCC}}$ high, delayed-strobe pulse STBDLY generates the signal BIN through gates 452 and 453.

Once carriage motion is initiated, the internal timing involved in printing a line of characters can be grouped into two categories:

1. Extracting the two characters from memory (one character for the left and one for the right-hand head) during the space interval between characters (DCW0); and
2. Multiplexing both characters through a single full-step and half-step character generator.

This occurs during intervals (DCW1) and (DCW01) through (DCW5) and (DCW05).

The two characters required by the right and left print heads are retrieved from memory during the intercharacter space interval DCW0 (see FIG. 4*f*). The sequence counter 404–405 (FIG. 4*b*) is used to control the recirculating memory. This counter is controlled by a flip-flop 408 which in turn is controlled by flip-flop 407. When either the forward or the reverse clutch of the printer is activated, signal FWDREV goes high to cause the output of gate 406 to go low to set bi-stable flip-flop 407. The next oscillator clock pulse OSCA then sets flip-flop 408 which enables the sequence counter and which further causes a generation of the shift pulses CLKTB with the generation of each OSCA output.

At the time that the first character (i.e., the character for the right hand or B print head) is transferred from memory output to the latch registers 311-1 through 311-7, the flip-flop 407 is reset. When the second character (i.e. the character for the left-hand or A print head) reaches the memory output, flip-flop **408** is set, terminating all memory shifts, In the space interval following the printing of these two characters the signal DCW0 is high clocking bistable flip-flop **407** set again. This initiates the retrieval of the next two characters from memory. The sequence continues until the signal FWDREV if deactivated.

The specific timing and extracting of characters from memory, however, is dependent upon whether the carriage is moving in the forward or reverse direction.

As soon as the signal FWD goes high, each subsequent 0SCA clock pulse (see FIG. 4*a*) shifts the memory register **300** and increments the sequence counter **404–405.** Prior to the first shift, the memory is organized so that the dummy character is in the right-hand most stage, the first character is in the next stage and etc. until the 132d character is in the left-hand most stage, as shown below:

		(B)		(A)	
132		67		1	D

The left hand (A) print head will print the first character and the right hand print head will print the 67th character. To accomplish this, the 67th character is first stored in latch register stages **311–1** through **311–7,** then the characters in memory register **300** are recirculated so that the first character appears at the memory output. This occurs when sixty-seven consecutive shift operations have been performed.

		(A)		(B)
66		1		67

When the sequence counter **404–405** reaches the count of 67 (see gates **411** and **412** of FIG. 4*c*) the output of gate **414** goes high causing the generation of **500** nanosecond pulse LFFB. This pulse clocks the 67th character in the latch register **311–1** through **311–7** and resets bistable flip-flop **407** through gate **406***a* (see FIG. 4*b*). Since inputs **408***e* bistable flip-flop **408** are low the signal level at output **408***c* remains unaffected.

To now move the first character to the right-hand most stage of the shift register **300,** 67 more shifts are generated. When the sequence counter reaches a count of 133 (see gate **413** of FIG. 4*c*), corresponding to 66 shift pulses later, the output of gate **413** goes low causing gate **430** to generate signal RCGF. This high RCGF allows the next (i.e., the 67) 0SCA pulse to reset flip-flop **408** causing the signal CTRG to go low. The low CTRG resets the sequence counter and inhibits any further shift pulses. As a result, the first character is available at the right-hand most stage of shift register **300.**

		(B)		(A)
D		67		1

No further action occurs until the next DCW0 interval, at which time the 68th and second characters are retrieved in exactly the same way. This operation continues until the carriage reaches the right-hand limit switch (to be more fully described hereinbelow) which deactivates the FWD signal.

When printing in the reverse direction, i.e., when the print head assembly carriage is at the right-hand margin and a dummy character is detected in the right-hand most stage of the recirculating register **300,** signal REV goes high, indicating operation in the reverse print mode. As in the FWD mode, this allows subsequent 0SCA clock pulses to shift the recirculating register and to increment the sequence counter **404–405.** The memory timing in this reverse direction is different, however, than that for the forward timing.

When REV goes active, the memory format is the same as it was at the start of the FWD mode in that the dummy character is in the right-hand most stage of the register, the first character is in the next stage, etc. with the 132nd character being in the left-hand most stage of register **300.**

(B)			(A)			
131		67	66		1	D

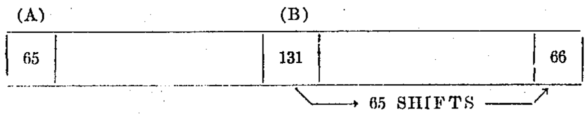
→ 132 SHIFTS →

In this case the left hand print head will print the 66th character and the right hand print head will print the 132nd character. To accomplish this, the memory is initially shifted 132 times. The logic condition REV and a count of 132 in sequence counter **404–405** enables gates **421** and **422** to cause the output of gate **422** to go low which ultimately generates a **600** nanosecond LFFB pulse at the output of gate **419** which clocks the 132nd character (which) is now at the memory output) into the latch register flip-flops **311–1** through **311–7** and further functions to reset flip-flop **407** through gate **406***a* (see FIG. 4*b*) which disables input **408***a* to the flip-flop **408.** As was previously the case, output **408***c* remains unaffected since both its inputs **408***a* and **408***e* are low at this time.

(B)		(A)			
131		66		D	132

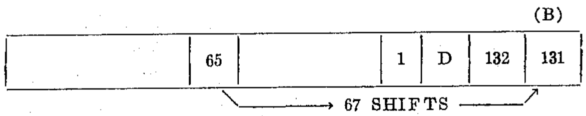
To move the 66th character to memory output, sixty-seven more shifts are generated. When the sequence counter therefore reaches a count of **198** (66 shift pulses later) gate **429** has its output go low which causes the generation of a high RCFG signal which allows the next (i.e., the 67th) 0SCA pulse to reset bistable flip-flop **408** and set the bistable flip-flop **431** causing the output **431***c* to go high to generate the ENABLE signal. The high CTRG output resets the sequence counter **404–405** and prevents any further shift pulses, keeping the 66th character at the memory output. The high ENABLE signal, which remains set for the remainder of the reverse line, indicates that the first set of characters has been retrieved from memory. This indication is needed since the memory timing for all other characters on that line is different than the timing for the first set of characters.

After the first two characters (i.e. the 132nd and 66th characters) are printed, DCW0 again goes high causing bistable flip-flop **407** to be set. The next 0SCA pulse triggers bistable flip-flop **408** again allowing the recirculating register **300** to shift and allowing the sequence counters **404–405** to be incremented. At this time the memory is organized such that the 66th character is in the right-hand most stage of recirculating register **300,** the 131st character is in the 66th stage of the register and the 65th character is in the left-hand most stage of the recirculating register as, shown below:



As a result, recirculating register is shifted 65 times bringing the 131st character required by the right-hand print head to the memory output. The simultaneous logic conditions of the high REV signal, the high ENABLE signal (appearing at gate **424** of FIG. 4*c*) and a count in the sequence counter **404–405** of **65** (see gate **425** and **426**) activate gate **426** again causing the generation of LFFB pulse which clocks the 131st character into the latch register flip-flop stages **311–1** through **311–7** and which further resets bistable flip-flop **407**.

To remove the 65th character to the memory output, 67 more shifts are generated.



When the sequence counter reaches a count of 131 (66 shift pulses later), the logic condition of high REV signal, a high ENABLE signal (see gate 424— FIG. 4*c*) together with a count in the sequence counter **404–405** of 131 (see gate **425** and gate **428** of FIG. 4*c*) activates the output of gate **428** generating a high RCGF pulse which allows the next (i.e., the 67th) 0SCA pulse to reset bistable flip-flop **408** which serves to clear the sequence counter **404–405** and to prevent the generation of any further shift pulses.

For the remainder of that line, until REV goes low, the bistable flip-flop **431** has its output **431***c* remaining high (ENABLE) allowing successive memory shifts of 65 and 67 oscillator pulses for each remaining pair of characters retrieved from memory.

Referring to the timing diagrams of FIGS. 4*e* and 4*f*, during the first 10 microseconds of STROBE intervals DCW1–DCW5 and during the first 10 microseconds of delay STROBE intervals DCW01–DCW05, a high LBD is generated by either the signal $\overline{\text{CRTSTB}}$ or $\overline{\text{STBDLY}}$. LBD gates the output of the latch register flip-flops **311–1** through **311–7** to character address lines $\overline{\text{CHADD1}}$ through $\overline{\text{CHADD7}}$ to character generators **320** and **325**. During STROBE intervals DCW1 through DCW5, only the full-step character generator is ENABLED. During delayed STROBE intervals DCW01 through DCW05, the half-step character generator is ENABLED.

On the trailing edge of LBD, the seven bit dot pattern from the ENABLED character generator is clocked into the output latch register flip-flop **334–1** through **334–7**.

During the remainder of each STROBE or delayed STROBE interval, the high CATCG signal (which is LBD inverted) gates the character in the right-hand most stage of the recirculating register **300** to the character generators. During this same STROBE or delayed STROBE interval, if neither of the two characters retrieved from the memory is a dummy character (i.e., DMCD and BLKSTB are both low), then signals TGSL1 and TGSL2 go high (see the output of gates **339** and **339***b* of FIG. 3*d*). This causes the seven outputs of the character generator to go to the seven solenoid drivers for the left-hand print head, the signals TGSL1 and TGSL2 enabling the gates **335–1** through **335–7**, and simultaneously therewith causing the seven outputs in the latch register flip-flops stages **334–1** throuth **334–7** to be gated through gates **336–1** through **336–7**, respectively, causing both print heads to be activated simultaneously. The outputs from gates **335–1** through **335–7** are the signals $\overline{\text{CG1A}}$ through $\overline{\text{CG7A}}$ for driving the A print head solenoids while the outputs of gates **336–1** through **336–7** are the signals $\overline{\text{CG1B}}$ through $\overline{\text{CG7B}}$ for driving the B print head solenoids.

This timing sequence is repeated nine times for each character (the intervals DCW1, DCW01, DCW2, . . . DCW04, DCW5). The character code in latch register stages **311–1** through **311–7** and at the output stage of memory **300** is changed only during interval DCW0 which corresponds to the space interval between characters. FIG. 4*g* illustrates the relationship between dot locations and timing intervals for the alphabetic character Y.

When an elongated character code is detected in a received line of data, the printer responds by printing all double width characters for that line. In this mode, only **66** characters may be printed on one line, the left-hand print head printing the first through the 33rd and the right-hand print head printing the 34th through the 66th characters. As a result, the organization of these characters in the shift register and, therefore, the order in which they must be received is as follows:

1. Characters one through 33,
2. Thirty-three "don't care" characters (since these 33 characters will not be printed),
3. Characters 34 through 66,
4. A carriage return code or 33 more characters which will not be printed.

The expended character code is detected by gate **236B** of FIG. 2*e* described hereinabove which generates the signal $\overline{\text{UPFC}}$.

If the print heads are currently at the extreme right-hand position (the signal EOP is high), the signals UPSC and EOP are Anded by gate **445** of FIG. 4*j* to clock the bistable flip-flop **456** to generate a low $\overline{\text{RTL}}$ signal at output **456***a* which generates a reverse clutch signal at the output of gate **457** which returns the print heads to the left-hand margin. During this time, the printer goes busy until the heads reach their left-hand margin and the clutch is deactivated. As a result a line of elongated characters is always printed from left to right.

The signal $\overline{\text{UPSC}}$ also sets latch circuit comprised of gates **514** and **515** shown in FIG. 5*d* which will be more fully described, which affects the timing inputs to the generator in the following manner:

A high UCC and a low $\overline{\text{UCC}}$ are respectively applied to gates **448**a and **448** which allow the $\overline{\text{ECSTB}}$ to clock the divide-by-six counter **446** and further allows the signal ECSTB applied to gate **454** to clock the divide-by-six counter **450**. The ECSTB signal is a divide-by-two output of the counter which is clocked by video STROBE signal $\overline{\text{CTRSTB}}$. As a result the timing signals $\overline{\text{DCW1B}}$ through $\overline{\text{DCW5B}}$, and $\overline{\text{DCWO1B}}$ through $\overline{\text{DCW05B}}$ are twice as long during elongated character mode as during normal printing. Since the timing inputs of the character generator are generated at every other STROBE (or delayed STROBE) pulse, each dot in the character matrix gets printed twice. An example of an elongated alphabetic character Y is shown in FIG. 4*j*.

The order in which the dot column patterns are printed can best be understood for example from a consideration of FIG. 4g. When the left-hand and right-hand print heads are printing by moving across the paper document from the left toward the right, the first dot column printed is the dot column DCW1. Thereafter the dot column patterns DCW01, DCW2, . . . , DCW04 and DCW5 are printed in succession. However, when the print heads are printing by moving across the paper document form the right to the left, the "full" and "half" step dot patterns must be reversed so that the order of printing is DCW5, DCW04, DCW4, . . . DCW01 and DCW1. IN order to obtain this reversal automatically, the circuits of FIGS. 4*k* and 4*l* are employed. Since these circuits are similar to one another a description of FIG. 4k will be given initially. Invertors **460** through **463** have their inputs coupled to the outputs **447–1, 447–5, 447–2** and **447–4**, respectively, of the decoder circuit **447** shown in FIG. 4*g*. The input of amplifier **478** is coupled to the output **447–3** of decoder **447** of FIG. 4g to directly produce the output signal $\overline{DCW3}$.

The outputs of invertors **460–463** are selectively coupled to respective inputs of the group of AND gates **464–471.** The remaining inputs of AND gates **464, 466, 468** and **470** are coupled in common to a line which receives the FWD signal to enable those gates when the printer is printing in the forward (i.e., left to right) direction. The remaining inputs of gates **465, 467, 469** and **471** are all coupled in common to a line which receives the REV signal which enables these gates when the printer is operating in the reverse (i.e. the right to left) printing direction. OR gates **472** through **475** adds outputs to the amplifiers **476, 477, 479** and **480,** respectively, to generate those signals $\overline{DCW1}$ through $\overline{DCW5}$ which are applied to the dot column input terminals **320*b*–1** through **320*b*–5** of the full-step character generator to read out the dot column patterns in the appropriate order. Since the signal $\overline{DCW3B}$ is always in the center of the five signals, this signal need not be gated through any of the gates that the remaining signals are gated through.

The circuitry for providing the dot column signals for the "half-step" generator **325** of FIG. 3*c* is shown in FIG. **41** and operates in substantially the same fashion except that the signal $\overline{DCW05B}$ is directly coupled to the input of amplifier **478′** while the remaining signals $\overline{DCW01B}$ through $\overline{DCW04B}$ are applied to the inputs of gates **460′** through **463′** and the gates groups **464′** through **475′**, respectively.

Considering the circuitry of FIG. 4*k*, in the forward printing mode it can be seen that the signals $\overline{DCW1B}$ through $\overline{DCW5B}$, when sequentially generated by decoder **447** of FIG. 4*g* are enabled to pass through gates **464, 466, 468** and **470** as well as amplifier **478,** in the same order in which they are produced when the signal FWD is high. In the reverse printing mode, only gates **465, 467, 469** and **471** are enabled so that signal $\overline{DCW1B}$ is passed by **471** and **475** and amplifier **480** to generate the signal $\overline{DCW5}$. It can be seen that the signals are thus generated in reverse order during the reverse printing mode.

Turning to consideration of FIG. **41** the outputs of decoder **451** shown in FIG. 4*g* are generated in the order $\overline{DCW01B}$, $\overline{DCW02B}$, . . . $\overline{DCW05B}$, which, in the forward printing mode, result in the generation of the signals $\overline{DCW01}$, $\overline{DCW02}$, . . . DCW05, respectively. In the reverse printing mode the $\overline{DCW01B}$ generates $\overline{DCW04}$ (through gates **469′, 474′** and amplifier **479′**); signal $\overline{DCWO2B}$ produces a signal $\overline{DCW03}$ (through gates **471′, 475′** and amplifier **480″**); $\overline{DCW03B}$ produces $\overline{DCW02}$; $\overline{DCW04B}$ produces $\overline{DCW01}$; and $\overline{DCW05B}$ directly produces $\overline{DCW05}$.

The order of operation of the full-step and half-step character generators **320** and **325** is such that the first column of pin positions for the **67**th character (assuming that printing has just begun for the forward direction) is developed by the full-step character generator **320** with the pin positions CG1 – CG7 being temporarily stored in the B head, bistables **334–1 – 334–7**, respectively. Immediately thereafter, the first character is decoded by full-step character generator **320** and in the presence of the signal $\overline{DCW1}$ the first column pin positions are applied to the driver circuits for the A head simultaneously to the first column pin positions of the 67th character being applied to the selective drive circuits for the B head. All of this occurs during the generation of the center strobe and strobe signals to be more fully described. Thus, the printing of the first dot column positions of the first and 67th characters are simultaneously performed. The half-step character generator **325** receives first the first half-step column signal $\overline{DCW01}$, together with the coded character representing the 67th character to be printed for developing the first half-step column pin position signals at outputs CG1 – CG7 which are temporarily stored in the bistable circuits **334–1** through **334–7.** Thereafter the shift register is again shifted to place the first character in the right-hand most position of shift register **300** which, together with the signal $\overline{DCW01}$, causes the first half-step pin position column signals to appear at the outputs CG1–CG7, which signals are simultaneously caused to pass to the A head driver circuitry together with the signals temporarily stored in bistable flip-flops **334** which are passed through driver circuits for the B head to simultaneously print the first half-step column pin positions, which printing occurs during the strobe delay signal.

These operations continue until all five full-step dot column positions and all four half-step dot column positions of the first and 67th characters are printed. Thereafter, the operation is repeated for the second and 68th characters, the third and 69th characters, . . . and the 66th and 132nd characters to complete a full line of characters. As soon as a full line of characters has been printed in the forward direction, the FWD signal is terminated and the REV signal is generated, whereby the column pin positions for both full-step and half-step columns are generated in reverse order to permit printing of the fifth full-step, fourth half-step, fourth full-step, third half-step, third full-step, second half-step, second full-step, first half-step and first full-step pin positions for the 132nd and 66th characters are printed in the above order. This operation is repeated for the 131st and 65th, 130th and 64th, . . . and 67th and first characters whereupon a full line of characters is thereby printed in the reverse print direction (i.e. with the dual heads moving from right to the left).

The output (STA) of gate **501** is ANDED with the signal UCC at gate **503,** while the output of gate **502** is ANDED with the complement signal $\overline{UCC}$ at gate **504.** The outputs of gates **503** and **504** are ORed at gate **505** to develop the signal ROME2 which is applied to gate **505** shown in FIG. 3*c*, together with the signal CHADD8 which causes gate **505** to control the half-step control generator through gate **507** to activate the character generator **325.** The output STA is ANDED with the signal CHADD8 at gate **506** in FIG. 3*c* which activates the full-step character.

FIG. 2*a* shows the printer interface circuitry **200** for electrically coupling the printer to a data source such as, for example, a computer. The data source provides up to eight data bits (DATA 1– DATA 8) in parallel together with a data strobe pulse. The DATA 1 – DATA 7 inputs are inverted at **201***a*–201g to develop the signals $\overline{\text{DS1}}$ – $\overline{\text{DS7}}$, respectively. The DATA 8 input is wired to inverter **201***h* (see dotted line jumper J) for applications requiring an enlarged capacity of characters or other symbols to be printed. In applications requiring the lesser amount of characters, the DATA 8 input is disconnected from inverter **201***h*. The data strobe signal is inputted to inverter **201***j* to develop the signal DSTA.

The inputted information derived from the data source (i.e., a computer) may be either data words representing characters or symbols to be printed or control words, depending upon their particular binary format. Prior to insertion of characters to be printed into the data register, gating circuitry is provided to detect the presence of control words in order to perform prescribed functions.

FIG. 2c shows the manner in which the signals DS1 – DS7 and $\overline{\text{DS8}}$ are derived. Each of the outputs $\overline{\text{DS1}}$ through $\overline{\text{DS7}}$ and $\overline{\text{IN8}}$ are applied to associated inputs of NOR gates **202***a* – **202***g* and NAND gate **203** (which receives the signal $\overline{\text{DS6}}$). NAND gate **204** receives the signals $\overline{\text{DMC1}}$ and the signal $\overline{\text{ZBCR}}$ to selective control the operation of gates **202***a* – **202***g* and **203.** When either a dummy character is present or a clearing of buffer operation is being performed at least one of the signals to gate **204** will go low causing its output to go high. The output of gate **204** is coupled in common to one input of all of the gates **202***a* – **202***g* and **203** causing the outputs of all of gates **202***a* – **202***g* to go low to prevent any character appearing at the remaining inputs of gates **202***a* – **202***g* from being loaded into the character register. Gate **203** is enabled to go high through the inversion action of inverter **205.** When no dummy character is present and when the character register is not being cleared, both inputs to gates **204** will be high causing its output to go low, thereby enabling gates **202***a* – **202***g* to develop the appropriate character at the outputs of these gates. For example, let it be assumed that the first data bit (DATA 1) is binary 1, this state will be inverted by inverter **201***a* of FIG. 2*a* whereby $\overline{\text{DS1}}$ will be binary 0. This condition is applied to one input of inverter 202a. Assuming that neither a priming operation nor a clearing operation of the data register is being performed, the other input of inverter **202***a* will be at binary 0 causing its output (DS1) to be at binary 1. Assuming the first data bit is a binary 0, $\overline{\text{DS1}}$ will be binary 1, which state will be inverted by gate **202***a* whereby DS1 will be at binary 0. The remaining gates **202***a* – **202***g* operate in a similar fashion.

NAND gate **203,** upon the occurrence of either a dummy character or a clear register signal, develops the first dummy character. Upon the occurrence of either a low $\overline{\text{DMC1}}$ or a clearing of the buffer, the output of NAND gate **204** will go high. This state is inverted by inverter **205** causing one input and NAND gate **203** to go low whereby the output of gate **203** which condition inverted first at gate **203***a* and then at inverter **203***b* to load a high condition into the shift register as the dummy character.

FIG. 2*e* shows the manner in which the printer circuitry is initialized or PRIMED. As soon as the printer is turned on, +5 volts is applied to one terminal of resistor R17. However, at this time capacitor C12 is discharged, preventing the voltage level at the input of inverter **225** from going high. Thus, the input of inverter **225** will be low upon energization of the printer causing its output to to high. Capacitor C11 maintains the output of NAND gate **226** at a low level which is inverted to a high level by inverter **227** to develop the signal PWR PRIME. These two high levels cause the output of NAND gate **226** to remain low. After a time delay, the input to inverter **225** goes high (due to the charging of capacitor C12) causing the output of inverter 225 to go low. The output of NAND gate **226** tries to go high, but it must first charge up capacitor C11 keeping PWR PRIME high for a somewhat longer period of time. The PWR PRIME signal is used to ensure that the SELECT bistable **296** (FIG. 2*q*) is held reset and that the EOP latch (gates **502–505** —FIG. 5*a*) is reset. PWR PRIME also creates PRIME which actuates the PRIME logic, to be more fully described.

One-shot multivibrator **224** may also be triggered by the absence of any one of the input signals to NAND gate **223** to cause it to go high. One input of NAND gate **223** is coupled to the output of NAND gate **222.** The inputs to NAND gate **222** consist of an input data word whose data bits DS1 – DS7 and DSTA are all high which is a control word from the data source indicating that any data sent up to the receipt of the control word should be deleted. This control words is employed, for example, when data may have been transitted to partially fill the character register and it is now desired to clear the character register. When all inputs to NAND gate **222** are high, its output goes low. So long as one input to NAND gate **223** is low, its output goes high to trigger oneshot multivibrator **224.** The signal IP which is also derived from the data source is detected by the printer as an initiate PRIME signal derived from the data source. The complement of this signal ($\overline{\text{IP}}$) causes the output of gate **223** to go high to develop a PRIME signal. The signal $\overline{\text{FWDREV}}$ is generated when either of the forward or reverse drive clutches are turned off which is indicative of the fact that a full line of characters has been printed.

The SEL signal which represents selection of the printer by an operator is generated by depressing the select switch SI (FIG. 2*q*) to generate the signal SEL from flip-flop **296** as will be more fully described. The signal $\overline{\text{SEL}}$ will also cause triggering of one-shot multivibrator **224.** The signal $\overline{\text{PRMOS}}$ sets up flip-flop **270** (FIG. 2*k*) and, on the occurrence of the next $\overline{\text{OSC}}$ pulse a prime is produced.

FIG. 2d shows the circuitry employed for acknowledging a request for access to the printer from the data source. The generation of the data strobe signal DSTA is applied to gate **211** whose output goes low when signal DSTA is high. This signal is inverted by inverter circuit **212** to generate the signal DSTB which is applied to input **206***a* of one-shot multivibrator **206.** Its output **206***b* goes low and after a predetermined delay goes high. This signal is applied to one input of NAND gate **213** whose output goes high during the time that the signal $\overline{AKDLY}$ is low to generate the signal $\overline{GNACK}$ (generate acknowledge). This signal is applied to input **207***a* of one-shot multivibrator **207** to cause its output **207***b* to generate a positive pulse which is inverted by inverter **208** to generate the acknowledge signal $\overline{ACKNLG}$, which signal is coupled to the external device to acknowledge the receipt of data and to initiate the external device that the printer is ready to accept additional data. This signal is applied to one input of gate **209** which functions with gate **210** as a bistable latch circuit to cause one input of gate **211** to go low and thereby terminate the signal DSTB. DSTA can be gated with ACKNLG to produce DSTB through Jumper **J1.** DTSB is used as the data strobe signal for the rest of the printer logic.

An acknowledge signal is prevented from being generated and a busy signal (BUSY) is generated in its place when any one of the functions represented by the signals applied to the inputs of gate **221** are being performed. The output of gate **221** goes high when any one of its inputs goes low, setting flip-flop **216** whereby its output **216***c* goes low causing gate **215** to go high to generate a high BUSY signal. OSC' clocks the output of inverter **218** into **216** and hence delays the trailing edge of BUSY to the external device by one clock interval after the busy state is terminated. The trailing edge of BUSY generates GNACK through gate **213** and inverter **214** to indicate completion of an operation.

FIG. **2***b* shows the circuitry for decoding the number of the control functions derived from the data source. The generation of the signal DSTA in either the simultaneous presence or absence of the signals SEL and DS2 causes one of the two gates **234, 235** to go low causing the output of gate **241** to go high. When the remaining inputs of gate **242** (one of which input is coupled to the output of gate **241**) goes high, this output goes low to generate the remote select signal $\overline{REMSEL}$. The remaining inputs of gate **242** are the seven data bits of the data word which must be in a prescribed binary form to develop a negative level at the output of gate **242.** For example, the signal format of data bits DS1–DS7 are 1X00100 (where X indicates that the signal DS2 may be either high or low). Similarly, gate **228** develops the signal CLGT when data bits TS6 and TS7 are both zero. The control word decoded by gate **233** is applied to one input of gate **231** through inverter **232** whereby gate **231** generates the decode bell ($\overline{DCBL}$) signal. When data bits DS4–DS7 are respectively 1000 and in the presence of the data strobe B signal (DSTB) gate **229** goes low, which condition is inverted by inverter **230** to develop a high input which is simultaneously applied to each of the gates **236***a*–**236***e* which decode the data bits DS1–DS3 to respectively detect the presence of a decoded strobe carriage return ($\overline{DSCR}$) at the output of gate **236***a*; an expanded character format ($\overline{UPSC}$) at the output of gate **236***b*; a form feed signal (**FF**) at the output of gate **236***c*; a vertical tab signal ($\overline{VT}$) at the output of gate **236***d* and a decoded line feed signal ($\overline{DCLF}$) at the output of gate **236***e*.

Oscillator **243** which is free running generates pulses at the 100 KC rate and has its output coupled to the inputs of inverters **244** and **245** which develop the signals OSCXT and OSC', respectively, at their outputs, which oscillator signals are employed in a manner to be described hereinbelow.

As was noted in FIG. **2***b*, a decode bell ($\overline{DCBL}$) may be transmitted from the data source to the printer. As shown in FIG. 2f, this signal is applied to gate **246** to trigger a bistable circuit **247** and generate the bell signal (BELL) and its complement $\overline{BELL}$. The signal BELL triggers an oscillator **248** which drives a speaker **249** to produce an audible signal. An audible signal may also be generated by a paper out indication which is identified by the signal $\overline{PE}$. The output of gate **246** goes to gate **250** whose other input receives the BELL signal to generate the signal $\overline{BSP}$.

The paper out signal is generated by the circuit of FIG. **2***g* which comprises a normally open switch S2 which closes when the paper roll is depleted to light lamp **251** to drive inverter **252** and inverter **253** to generate the signal $\overline{PE}$. The output of inverter **253** goes to inverter **254** to generate the signal PE.

Gate **255** receives the signals SEL : $\overline{PE}$ and $\overline{LD}$ to develop a signal whenever a select signal is generated or a paper out signal is generated or a light detector signal is generated to provide a signal to inverter **256** to generate the signal $\overline{FAULT}$ which is employed in a manner to be more fully described.

FIG. **2***h* shows the circuit employed for generating a paper motion signal and a delay line feed signal which is utilized in a manner to be more fully described to hold the printer in the "busy" state during the time that a line feed is being performed.

Gate **257** is coupled to signal $\overline{LF}$ and $\overline{VFD}$ to generate the signal PM (paper movement) and its complement $\overline{PM}$ after having passed through inverter **258.** The signal PM is used to trigger a one-shot multivibrator **259** to generate the signal DLYLF and its complement $\overline{DLYLF}$. One-shot multivibrator **259** generates a pulse of 80 milliseconds duration which is of sufficient length to permit the performance of a line feed operation.

FIG. **2j** shows the circuitry employed for operating the paper moving solenoid. Inverter **260** receives the signal PM (see FIG. 2h) which is applied to a time delay circuit comprised of capacitors **C18, C19** and resistors **R25** and **R26** for coupling the PM signal to one input of gate **261** and to the base of transistor **Q1.** The complement of the paper movement signal ($\overline{PM}$) is applied to one input of gate **262** together with the collector of transistor Q1. The output of gate **262** is applied to inverter **263** to generate the signal $\overline{PMSOL}$ which goes to the paper movement solenoid for advancing the paper and performing a line feed operation. A remotely controlled line feed operation signal may be applied at terminal **264.** Switch **S8** would be closed to perform such an operation and hence apply a signal to one input of gate **261,** the other input of which receives the decode line feed signal $\overline{DCLF}$ to activate gate **261.** The output of gate **261** is coupled to inverter **264** whose output triggers a one-shot multivibrator **265** which generates the signals LF and its complement $\overline{LF}$ for performing a line feed operation. A FWDREV signal may be applied to terminal **266** to trigger one-shot multivibrator **265** to generate the line feed signals.

FIG. **2k** shows a circuit employed for generating the PRIME signals for initializing the printer. As shown therein a signal $\overline{INPUT\ PRIME}$ derived from the data source is applied to one input of inverter **267** which, in turn, applies its output to inverter **268** to generate the signal $\overline{IP}$ which is applied to one input of gate **269** whose other input receives the signal $\overline{PWR\ PRIME}$. When either of these signals is present the output of gate 269 goes high to apply a high input to bistable flip-flop 270 and to apply its complement to the other input of bistable circuit 270 through inverter 271. At the occurrence of the next oscillator pulse ($\overline{OSC}$) developed at the output of oscillator 243 shown in FIG. 2*e*, bistable 270 is set to generate the signal $\overline{PRIME}$ and its complement PRIME. The signal $\overline{PRIME}$ is applied to one input of gate 272 whose other input receives the signal DMC which is employed to indicate a dummy character. The output of gate 272 is coupled to one input of gate 273 whose other input receives a signal $\overline{DS8}$ to generate the signal DS8 which is utilized in a manner to be more fully described.

FIG. 2*m* shows the manner in which a carriage return signal is decoded. The decoded strobe carriage return $\overline{DSCR}$ developed by gate 236*a* of FIG. 2*e* is applied to one input of gate 274 whose other input is coupled to the output of gate 275 to form a latch circuit. The output of gate 275 which is coupled to one input of gate 276 which together with the complement of the carriage return signal ($\overline{CR}$) receives the signal DSTB (data strobe B) developed at signal SCR. The remaining inputs to gate 275 are coupled to the signal FCCLK (first character clock) and $\overline{DB8}$. A high SCR allows the next OSC clock to set flip-flop 277. $\overline{ZBCR}$ goes low causing gate 204 (FIG. 2*c*) to force a space code on the shift register (300— FIG. 3*a*) input lines at the same time ZBCR ANDed with a high $\overline{TB8}$ at gate 279 of FIG. 2n allows OSC pulses to generate $\overline{CLKTB}$ pulses (set invert 285—FIG. 2*n*) for shift register 300. FIG. 2*m* shows the manner for generating the signal ZBCR and its complement $\overline{ZBCR}$ which is utilized to clear (i.e., "zero") the buffer during carriage return. The signal SCR developed at the output of gate 276 shown in FIG. 2m is applied to one input of a bistable flip-flop 277 which develops the signal ZBCR and its complement at its output terminals upon the occurrence of the next oscillator pulse OSC′ which is developed at the output of inverter 245 shown in FIG. 2*b*. Inverter 238 generates the complement $\overline{OSC}'$, which signal is utilized in a manner to be more fully described.

In FIG. 2*n* DSTB ANDed with CLGT (indicating a printable character has been received) at gate 283 also generates $\overline{CLKTB}$ through gates 284 and 285. The trailing edge of $\overline{CLKTB}$ shifts the input data into register 300. A latch comprised of gates 286 and 287 generates FCCLK (first character clock) which enables gate 275 (FIG. 2m) to generate $\overline{CR}$. When a carriage return has been detected ORBZ goes high (see gates 276*a*–276*b*—FIG. 2*m*) to generate a BUSY (see gate 221 and inverter 219—FIG. 2*d*).

The output of gate 276 is coupled to one input 277*a* of bistable flip-flop 277 and, upon the occurrence of the next OSC′ applied to the clock input 277*b*, causes output 277*c* to go high developing the signal ZBCR, as well as its complement $\overline{ZBCR}$ at output 277*d* which signal is low at this time.

The output ZBCR is applied to one input of gate 279 shown in FIG. 2*n* whose other input receives the signal $\overline{TB8}$, which is high when the dummy character is shifted to the right-hand most stage of the shift register 301 (FIG. 3a). The output of gate 279 is coupled to gate 280 whose remaining input receives the signal $\overline{DMC}$ which is generated by a PRIME signal and by bistable 299. The output of gate 280 is coupled to one input of gate 281 whose remaining input receives the oscillator signal OSC′ to develop an output which is applied to one input of gate 284 whose remaining inputs are the output of gate 282 and the output of gate 283. The input of gates 282 are the signals CTRG and OSCA. Gate 283 receives the signals DSTB and CLGT. The output of gate 284 is inverted by inverter circuit 285 to generate the signal $\overline{CLKTB}$. The output of gate 283 is also coupled to one input of gate 286 which is cross-coupled with gate 287 in the manner shown. Gate 287 has its remaining input coupled to the output of gate 288 which receives the signals $\overline{PRIME\ 2}$ and CATCG. The signals $\overline{CLKTB}$ and FCCLK are respectively utilized for clocking data in the shift register 300 and for generating a BUSY signal.

FIG. 2*p* shows the manner in which a light detect (LD) signal is generated. An end of print switch, to be more fully described, develops a signal EOPSW applied to one input of inverter 290. The presence of a ready-to-print signal RTP (generated in a manner to be more fully described) is applied to input 291*a* of bistable flip-flop 291. Upon the occurrence of the signal EOPS at the clock pulse input 291*b*, output terminal 291c goes low to generate the signal $\overline{LD}$, which signal is inverted by inverter circuit 292 to generate the high signal LD.

FIG. 2*q* shows the manner in which the select clock signal is developed. Signals from the select switch and the select switch return are selectively applied to gates 293 and 295 which are cross-coupled to form a latch in the manner shown. The output of gate 293 being coupled to one input of gate 294 whose remaining input receives the remote select signal $\overline{REMSEL}$ to generate the select clock signal SELCLK at the output of gate 294 when either of the inputs thereto is low. This signal is applied to the clock input of bistable flip-flop 296 to generate the select signal SEL at output 296*b* and its complement at 296*c*. The select signal is amplified by amplifier A to light the select lamp L. Flip-flop 296 is reset by a power PRIME signal applied through inverter 298 to the reset input 296*b*.

FIGS. 5*a*–5*c* show the circuitry employed to control the direction of movement of the heads and the time at which printing may occur, i.e., the time at which the heads are in position to begin printing.

FIG. 5*a* shows the limit switches S2 and S3 in schematic form. These limit switches are preferably reed switches and are located respectively at the left and right-hand ends of the paper document. Permanent magnets mounted on the print head carriage selectively activate switches S1 and S2.

When the ready-to-print switch S2 closes, a signal RTPSW is applied simultaneously to one input of gate 501 and gate 502. The output of gate 501 is coupled to one input of gate 503 whose other input is coupled to the output of gate 504 which goes high when there is no center strobe signal $\overline{CTRSTB}$ and when there is no power PRIME signal ($\overline{POWER\ PRIME}$). The ready-to-print signal RTPSW is low when closed, causing the output of gate 501 to go high. The two high outputs cause a low signal to appear at the output of gate 503 (signal $\overline{RTP}$). This output is coupled into the remaining input of gate 501 whose output is further utilized as the ready-to-print signal RTP.

Switch S3 is coupled to one input of gate 505 whose other input is coupled to the output of gate 502. The remaining input of gate 502 is coupled to receive the signal $\overline{POWER\ PRIME}$. The closure of switch S3 causes the output of gate 505 to go high. If switch S2 is open at this time a high signal will be applied to the second input of gate **502** from the five volt source to resistor of R4. In the absence of a power PRIME signal (i.e. the signal $\overline{\text{POWER PRIME}}$, the output of gate **502** will be low to develop the end-of- print complementary signal $\overline{\text{EOP}}$ to provide a second low input to gate **505** to maintain its output at a high level which is further utilized as the end-of-print signal EOP. Thus, even though switch S3 opens the end-of-print signal is maintained.

FIG. 5*b* shows the circuit for controlling the forward motion of the heads. Gate **506** receives the inputs TB8, RTPL and FCCLK which causes the output of gate **506** to go low when all of these signals are high (RTPL is high when S2—FIG. 5*a*, is closed). This low signal is coupled to one input of gate **507** whose output is coupled to one input of gate **508** and whose remaining input is coupled to the output of gate **508** to form a latch circuit. When the output of gate **506** goes low, the output of gate **507** goes high. The remaining inputs of gate **508** are high when the POWER PRIME and end-of-print signals are absent (i.e., signals $\overline{\text{EOP}}$ and $\overline{\text{POWER PRIME}}$ are high). This causes the output of gate **508** to go low to generate the complement of the forward signal $\overline{\text{FWD}}$ which is inverted at inverter **509** to generate the forward signal FWD.

FIG. 5*c* shows the circuitry for generating the reverse signal. When the signals TB8, EOP and FCCLK are all high, the output of gage **510** goes low. This signal is applied to one input of gate **512** causing its output to go high and develop the reverse signal REV. This also occurs in the absence of a POWER PRIME signal ($\overline{\text{POWER PRIME}}$) to return the carriage to the extreme left-hand portion. The output of gate **512** is coupled to one input of gate **513** whose remaining input receives the complement of the ready-to-print signal ($\overline{\text{RTP}}$) to generate the complement of the reverse signal $\overline{\text{REV}}$. The output of gate **513** is coupled to the remaining input of gate **512** to cause the output of gate **512** to go low when the output of gate **513** is high.

FIG. 5*d* shows a circuit which may be employed for generating expanded characters. When the request for expanded characters is detected by gate **236*b*** as shown in FIG. 2*e*, this signal $\overline{\text{UPSC}}$ is applied to one input of gate **514**. This signal is low, causing the output of gate **514** to go high and generate the signal UCC. This high signal is applied to one input of gate **515** causing its output to go low which serves as the complementary signal $\overline{\text{UCC}}$. The output of gate **515** is applied to the remaining input of gate **514** to form a latch circuit. A PRIME signal is applied to inverter **516** whose output goes low when the PRIME signal is present to cause the output of gate **515** to go high which, in turn, causes the output of gate **514** to go low, thereby clearing an expanded character signal. The output of inverter **516** is applied to bistable flip-flop circuit **517** to generate the signal DMC and its complement $\overline{\text{DMC}}$ which is utilized for creating a dummy character.

Advancement of the paper document in the printer is controlled by the circuits of FIGS. 6*a* and 6*b*. Turning first to FIG. 6*a*, a form feed operation is controlled by gate **518**. Gate **236*c*** of FIG. 2*e* decodes a form feed code which causes the signal $\overline{\text{FF}}$ to go low. This causes the output of gate **518** to go high to generate the form feed flip-flop signal LFF. Gates **518** and **519** form a latch circuit. When this signal goes high it causes the output of gate **519** to go low generating complementary signal $\overline{\text{LFF}}$. This maintains the output of gate **518** high. The signal $\overline{\text{LFF}}$ is applied to one input of gate **520**, causing its output to go high and thereby causing bistable flip-flop circuit **521** to cause its outputs **521*c*** and **521*d*** to go high and low, respectively, to generate the vertical feed drive signal and its complement (VFD and $\overline{\text{VFD}}$ respectively). This signal is utilized to actuate a clutch mechanism provided between the printer motor and the form feed mechanism to cause the form to feed to a top of form position. When the top of form switch S4 is closed the same operation occurs.

Detection of the request for a vertical tab operation, which is detected by gate **236*d*** of FIG. 2*b* causes generation of the signal $\overline{\text{VT}}$ which is low at this time to cause the output of gate **522** to go high thereby generating the signal LVT. The output of gate **522** is coupled to one input of gate **523** whose output is coupled to the remaining input of gate **522**. With the output of gate **522** high, and the remaining input of gate **523** high, the signal $\overline{\text{LVT}}$ is low to cause the output of gate **520** to go high and thereby generate the VFD signal to perform a vertical feed operation.

Gate **524** has its output simultaneously coupled to remaining inputs of gates **519** and **523** to maintain these inputs high in the absence of either a PRIME signal or a delay line feed (DLYLF) signal.

FIG. 6*b* shows the circuitry for the paper tape reader which is a device for receiving a pre-punched paper tape which may be in the form of a closed loop having paper tape punches in selected positions of its two channels. The paper tape is advanced one incremental step per each line stepping operation which the paper document experiences. The detection of a punched hole in channel 1, for example, causes a sensing device shown schematically in the form of a switch S5 to close and thereby raise the voltage applied to the base of Q1. This causes Q1 to conduct, thereby applying substantially zero volts at the base of Q2 causing its output to go high. The output of Q2 is applied to one input of gate **525** whose other output receives the latch form feed signal LFF which is high during a form feed operation. The output of gate **525** which is high at this time is applied to one input of gate **526** causing its output to go low. This signal $\overline{\text{HL}}$ is applied to one input of gate **527** shown in FIG. 6*a* whereupon bistable flip-flop **521** is reset during the ocurrence of the next oscillator pulse OSC' to remove the drive signal from the paper feed clutch and hence terminate the line feed operation. The extent of the line feed operation is controlled by appropriate positioning of the punched holes in channel 1 of the punch paper tape.

Channel 2 of the punch paper tape is sensed in a similar fashion wherein switch S6 schematically shows the hole sensing means for operating the circuitry comprised of transistors Q3 and Q4 in a manner similar to that described hereinabove with reference to transistors Q1 and Q2. When a hole is sensed, the output of Q4 goes high, which high output is coupled to one input of gate **528** whose other input receives the vertical tag signal LVT to cause the output of gate **528** to go high when a hole is sensed in channel 2 of the punch paper tape to generate the $\overline{\text{HL}}$ signal in the same manner as was previously described for resetting the bistable flip-flop **521**.

The reception of a form feed code on the input data lines D51–D57 causes generation of a low $\overline{\text{FF}}$ signal at gate 236c (FIG. 2*e*), which sets gate **518** to generate a high LFF (and a low $\overline{\text{LFF}}$). LFF allows the next $\overline{\text{OSC}}$

clock to set flip-flop 521 causing $\overline{VFD}$ to go low which: (1) generates a high PM signal (gate 257–FIG. 2*h*) which causes a low $\overline{PMSOL}$ (see inverter 263–FIG. 2*j*) to activate the line feed solenoid; and (2) causes the next $\overline{OSC}$ clock to set the "hole-sense" flip-flop 531 (FIG. 6*b*). When the paper tape channel No. 1 reaches the next hole position, the tape output is amplified by Q1 and Q2 to generate a high input to gate 525. This input is ANDed with LFF causing $\overline{HL}$ (gate 526) to go low. With $\overline{HS}$ and $\overline{HL}$ both low the output of gate 527 (FIG. 6*a*) goes high allowing the next $\overline{OSC}$ clock to reset bistable 521. The high $\overline{VFD}$ deactivates PM and PMSOL, deactivating the line feed solenoid. The high $\overline{VFD}$ also triggers one-shot 259 (FIG. 2*h*) generating a high DLYLF which is applied to gate 524 to reset the LFF latch comprised of gates 518–519, terminating the form feed operation. After the DLYLF interval is terminated the BUSY line goes inactive (FIG. 2*d*) allowing the printer to receive more data. A vertical tab is used to advance the paper and paper tape to the next hole position in channel 2 of the reader. Receipt of a vertical tab code is decoded by gate 236*d* (FIG. 2*e*) generating a low $\overline{VT}$ which sets a latch comprised of gates 522 and 523, causing the next $\overline{OSC}$ clock to set bistable 521. The remaining logic sequence is the same as that for form feed, except that paper tape channel 2 is used instead of channel 1.

Summarizing the operation of the printer in connection with the flow diagram 700 of FIG. 7, the data and control codes are inputted at 701 from the external source. The control codes are decoded at 702. If a control code is present its code format is determined by 703–710. Form feed, vertical tab or line feed control codes result in a paper motion operation 711 which causes an ACK signal to let the external device know that the printer is ready to receive either data or a carriage return code. If a carriage return code or a dummy character is detected (712) and the RTp switch 713 is closed, the forward clutch 714 is activated to effect carriage motion 715 and generate an acknowledge 716.

If the carriage is not on the left margin this condition is detected (727) and the reverse clutch is activated (728) to effect the movement of the carriage to the left-hand most position.

When the external device places data at input 701, the data is entered (719) until a dummy character is detected, indicating that 132 characters have been loaded into the register (720). If the carriage is in the left-hand most position (713) the forward clutch is activated (714) and the carriage is moved in the forward direction (715) causing the video signals to be generated. If the carriage is in the right-hand most position (717) the reverse clutch is activated (718). The video signals initiate operation of the column counter (722) and the character generators (723). The shift counter (724) controls the pairs of dot columns shifted out of the shift register (725) so that simultaneous operation of the left and right-hand print heads is effected through the print solenoids.

In the forward print direction, the 67th and 1st characters are respectively placed in the latch registers and recirculating memory output stage and shifting of the recirculating register is terminated. The LBD signal (FIG. 4*e*) gates the latch registers to the full-step character generator and the output of the character generator to the output latch registers, and the CATCG signal (FIG. 4*e*) gates the memory output stage to the character generator 300, and simultaneously couples the first dot column output of the character generator to the A head solenoids and the first dot column output of the latch registers 334 to the B head solenoids. The same operation is repeated for the half-step generator during one video time. The cycle is repeated five times until nine dot column patterns have been printed.

The recirculating memory is then shifted to retrieve the 68th and second characters; the 69th and third characters and so forth until the 132nd and 66th characters are retrieved and printed. At this time the EOP signal is generated, register 300 is loaded with the next line of characters, the carriage is moved in the reverse print direction and the 132nd and 66th characters are retrieved to drive the right and left-hand print heads to begin printing the next line.

Although there has been described a preferred embodiment of this novel invention, many variations and modifications will now be apparent to those skilled in the art. Therefore, this invention is to be limited, not by the specific disclosure herein, but only by the appending claims.

What is claimed is:

1. Control means for operating a printer having at least first and second printer heads each of said heads having a plurality of print wire solenoids for selectively generating dot column patterns;

said control means comprising first means for storing and recirculating binary coded data words each representing an alphanumeric character to be printed including means for reinserting the word at the output stage of the first means back into the input stage to cause said first means to operate as a recirculating memory;

second means for shifting said words in said first means;

third means coupled to said second means for counting the number of shift operations performed;

fourth means for temporarily storing a data word;

fifth means coupled to said third means for writing the data word appearing at the output stage of said first means into said fourth means without removing the data word from said first means when said third means reaches a predetermined count;

character generator means for generating signals representing a dot column pattern for the data word in said fourth means;

sixth means responsive to a second predetermined count in said third means for coupling the output of said first means to said character generating means;

seventh means for temporarily storing the dot column pattern signals generated by said character generator means when coupled to said fourth means;

eighth means coupled to said third means for terminating operation of said second means when said third means reaches a predetermined count, said eighth means including means for coupling the data word in the output stage of said first means to the input of said character generating means;

ninth means responsive to said eighth means for simultaneously coupling the outputs of said seventh means and said character generating means to said first and second print heads to print dot column patterns.

2. The control means of claim 1 further comprising registration means for generating registration signals each representative of the positions at which dot column patterns are to be printed;

means for counting said registration signals to generate signals representative of the number of registration signals counted;

said character generating means comprising first input means for receiving a data word and second input means for receiving the output of said registration signal counting means for generating a selected one of a plurality of dot column patterns which collectively represent the alphanumeric character to be printed, the dot column pattern being selected being controlled by the count of said timing signal counting means.

3. The control means of claim 2 further comprising means coupled to said registration signal counting means for resetting said registration signal counting means for activating said second means to shift the next succeeding characters into the output stage of said first means when a third predetermined count is completed and before the next third predetermined count is initiated.

4. The control means of claim 1 further comprising carriage means for receiving said printer heads, said printer heads being mounted at spaced intervals along said carriage means;

means for moving said carriage means in a forward direction;

means for moving said carriage means in a reverse direction;

first limit means for generating a first limit signal when said carriage means is in its left-hand most position;

means for generating a second limit signal when said carriage means is in its right-hand most position.

5. The control means of claim 4 further comprising means for clearing the first means when either said first or said second limit signal is generated;

means for activating said fifth means and seventh means only when said first limit signal is generated.

6. The control means of claim 5 further comprising 10th means coupled to said third means and responsive to said second limit signal for transferring the data word in the output stage of the first means to the input of said fourth means when a fourth predetermined count is accumulated;

11th means coupled to said third means and responsive to said second limiting signal for disabling said second means and coupling the output stage of said first means to the input of said character generating means when said third means accumulates a fifth predetermined count.

7. A dot matrix printer capable of printing 2N characters per line where N is a real integer comprising a platen;

a reciprocating carriage;

means for selectively moving said carriage and in a forward and a reverse direction across said platen;

first and second print head means arranged at spaced intervals along the carriage whereby each print head means is adapted to print one-half of the characters on each line of characters;

each print head means having a plurality of print wire actuating means for generating dot column patterns upon a paper document supported by the platen as the carriage moves across the platen;

a recirculating register having 2N+1 stages for storing 2N binary words each word representing a character to be printed, the N+1 stage of said register being the output stage;

means for loading said register with a start character word and 2N character words;

means for shifting said binary words through said register;

means for counting the number of shift operations;

first stage means;

first decoding means being enabled responsive to a count of N+1 in said counting means for transferring the word in the said output stage to said first storage means;

character generating means having first and second input means and an output for generating successive dot column pattern signals which cooperatively represent a character responsive to the character responsive to the character word coupled to the first input means and responsive to a dot column position signal coupled to said second input means;

second storage means for storing one dot column pattern;

said first decoding means further including means for enabling said character generating means to transfer the dot column pattern of the character stored in said first storage means to said second storage means;

second decoding means being enabled responsive to a count of 2N+1 in said counting means for disabling said shifting means, said second decoding means including print initiating means for coupling the output stage of said recirculating register to said character generating means first input means and for simultaneously coupling the outputs of said character generating means and said second storage means respectively to said first and second print head means to print the dot column patterns for the first and (N+1)st characters on a line of characters.

8. The printer of claim 7 further comprising registration means for generating position pulses responsive to the movement of said carriage means;

means for counting said position pulses;

the output of said position pulse counting means being coupled to the character generating means second input means whereby the dot column pattern generated at the output of the character generating means is altered as the counting in said second counting means is incremented.

9. The printer of claim 7 further comprising means responsive to the operation of said print initiating means for restarting said shifting means.

10. A method for operating a printer of the dot matrix type having left-hand and right-hand print heads movable in a first direction by single carriage means for simultaneously printing dot column patterns of the left-hand and right-hand halves respectively of a line of characters comprising the steps of:

a. loading groups of binary signals into a recirculating register, each of said groups representing a character to be printed;

b. shifting the signal groups in said register until the signal group representing the first character to be printed by the right-hand print head is shifted into the output stage of the register;

c. temporarily storing the aforesaid signal group in a latch register;

d. shifting the signal groups in the register until the signal group representing the first character to be printed by the left-hand print head is shifted into the output stage of the register;

e. converting the signal group in the latch register into dot column pattern signals for forming the character represented by the binary signals in said latch register and storing the dot column signals in an output latch register;

f. immediately thereafter, converting the signal group in the output stage of the recirculating register into dot column pattern signals for forming the character represented by the binary signals in the output stage of the recirculating register;

g. simultaneously applying the dot column pattern signals to their respective print heads for simultaneously operating the heads.

11. The method of claim **10** further comprising the steps of:

h. linearly moving the print heads during the printing operation;

i. monitoring the movement of the print heads for generating position signals representing the position of the heads relative to the paper document upon which the dot matrix characters are being printed;

j. controlling the dot column pattern being formed during each converting step by said position signals to sequentially produce N dot column pattern signals for each character where N is a real integer greater than 1.

12. The method of claim **10** further comprising the steps of:

h. shifting the binary groups in the recirculating register until the binary signal group representing the second character to be printed by the right-hand print head is shifted into the output stage of the recirculating register;

i. temporarily storing the aforesaid signal group in a latch register;

j. shifting the signal groups in the register until the signal group representing the second character to be printed by the left-hand print head is shifted into the output stage of the register;

k. converting the signal group in the latch register into dot column pattern signals for forming the character represented by the binary signals in said latch register, and storing the dot column signals in an output latch register;

l. immediately thereafter, converting the signal group in the output stage of the recirculating register into dot column pattern signals for forming the character represented by the binary signals in the output stage of the recirculating register;

m. simultaneously applying the dot column pattern signals to their respective print heads for simultaneously operating the heads.

13. The method of claim **12** further comprising the steps of:

n. clearing the recirculating register when the printing of the line of characters is completed;

shifting groups of binary signals into the recirculating register which groups represent the next line of characters to be printed;

moving the carriage means in the reverse direction to print the next line of characters thereby eliminating the need for a carriage return operation and whereby alternate lines of characters are printed when the carriage moves in a forward direction and intervening lines of characters are printed when the carriage moves in the reverse direction.

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