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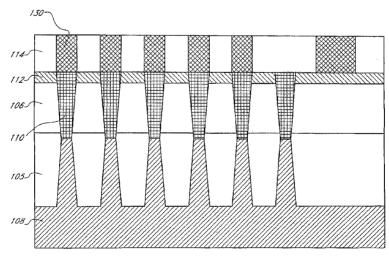
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(54) Title: INTEGRATED CIRCUIT FABRICATION

102 104



(57) Abstract: A method for defining patterns in an integrated circuit (100) comprises defining a plurality of features in a first photoresist layer using photolithography over a first region (102) of a substrate (108). The method further comprises using pitch multiplication to produce at least two features (120) in a lower masking layer (116) for each feature in the photoresist layer. The features in the lower masking layer (116) include looped ends (124). The method further comprises covering with a second photoresist layer (126) a second region (104) of the substrate (108) including the looped ends (124) in the lower masking layer (116). The method further comprises etching a pattern of trenches in the substrate (108) through the features in the lower masking layer without etching in the second region (104). The trenches have a trench width.

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A. CLASSIFICATION OF SUBJECT MATTER INV. H01L21/311 H01L2 H01L21/033 According to International Patent Classification (IPC) or to both national classification and IPC **B. FIELDS SEARCHED** Minimum documentation searched (classification system followed by classification symbols) HOllDocumentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data C. DOCUMENTS CONSIDERED TO BE RELEVANT Category* Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. Α US 5 328 810 A (LOWREY TYLER A [US] ET AL) 1 - 7312 July 1994 (1994-07-12) cited in the application the whole document Α US 6 010 946 A (HISAMUNE YOSIAKI [JP] ET 1-73 AL) 4 January 2000 (2000-01-04) column 8, line 14 - column 9, line 26; figures 5A-6D Α US 6 632 741 B1 (CLEVENGER LAWRENCE A [US] 1 - 73ET AL) 14 October 2003 (2003-10-14) column 1; figure 2 Α US 2003/230234 A1 (NAM DONG-SEOK [KR] ET 1 - 73AL) 18 December 2003 (2003-12-18) the whole document Further documents are listed in the continuation of Box C. See patent family annex. Special categories of cited documents: *T* later document published after the international filing date or priority date and not in conflict with the application but "A" document defining the general state of the art which is not cited to understand the principle or theory underlying the considered to be of particular relevance "E" earlier document but published on or after the international *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to filing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) involve an inventive step when the document is taken alone document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such docu-"O" document referring to an oral disclosure, use, exhibition or ments, such combination being obvious to a person skilled in the art. other means document published prior to the international filing date but later than the priority date claimed "&" document member of the same patent family Date of the actual completion of the international search Date of mailing of the international search report 14 November 2006 21/11/2006 Name and mailing address of the ISA/ Authorized officer European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Szarowski, Anne Fax: (+31-70) 340-3016

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Information on patent family members

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