



(51) International Patent Classification:

H01L 21/20 (2006.01) H01L 49/02 (2006.01)

H01L 27/108 (2006.01)

(21) International Application Number:

PCT/US2019/068590

(22) International Filing Date:

26 December 2019 (26.12.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/786,165 28 December 2018 (28.12.2018) US

(71) Applicant: **3D GLASS SOLUTIONS, INC.** [US/US];
5601-B Balloon Fiesta Parkway NE, Albuquerque, New
Mexico 87113 (US).

(72) Inventor: **FLEMMING, Jeb, H.**; 2817 Santa Monica SE,
Albuquerque, New Mexico 87106 (US).

(74) Agent: **CHALKER, Daniel, J.** et al.; Chalker Flores, LLP,
14951 North Dallas Parkway, Suite 400, Dallas, TX 75254
(US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,

MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: ANNULAR CAPACITOR RF, MICROWAVE AND MM WAVE SYSTEMS

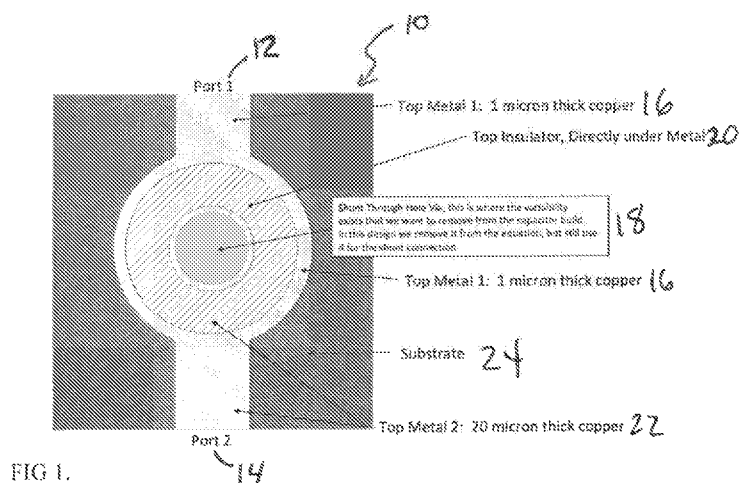


FIG. 1.

(57) Abstract: The present invention includes a method for creating an annular capacitor adjacent to via or imbedded metal structure allowing for device to be made in close proximity to the via connecting to a ground plane. The annular capacitor in close proximity to the metal filled via or imbedded metal structure allows the construction of capacitors, filters, or active devices enabling a smaller RF device and/or to shunt a signal to the integrated ground plane. This reduces the RF, Electronic noise and results in a reduced device size.



ANNULAR CAPACITOR RF, MICROWAVE AND MM WAVE SYSTEMS**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This PCT International Patent Application claims priority to U.S. Provisional Patent Application Serial No. 62/786,165 filed December 28, 2018, the contents of which is
5 incorporated by reference herein in its entirety.

STATEMENT OF FEDERALLY FUNDED RESEARCH

[0002] None.

TECHNICAL FIELD OF THE INVENTION

[0003] The present invention relates in general to the field of creating a planar surface
10 between via(s) and other structures and the substrate used for RF microwave and millimeter wave applications reducing device/system size and lowering parasitic noise and signals.

SUMMARY OF THE INVENTION

[0004] Without limiting the scope of the invention, its background is described in connection with creating a planar surface between vias and other structures and the substrate used for RF,
15 microwave, and millimeter wave applications. The fundamental problem is the metals that fill a via or other metal structures in/on a substrate. Planarizing generally uses a form of chemical mechanical polishing (CMP) of the substrate and structure on/in the substrate to bring the surface to be flat and parallel. The challenge is that the substrates are quite hard relative to the other material on or in the substrate. As an example, boron silicate quartz and silicon have a
20 hardness between 6 to 7 Mohs while typical metals (copper, gold and silver) used in high frequency application have a hardness of 2.5 to 3 Mohs. This hardness differential creates a fundamental problem when using CMP to planarize the surface. The softer metal structures are removed at a higher rate than the harder substrate. This creates a lower surface in the metal structure relative to the surface of the harder substrate. The transition from substrate to
25 metal structure can be as great as 0.5 μm . In general, the magnitude of the depth of this transition is not uniform across a wafer. This transition or step creates a random thinning of structures/devices that are made on top of, or that cross the substrate metal transition.

[0005] At low frequencies, that solution is to simply create the device in the planar field of the substrate and run a metal interconnected to the metal structure such as a via or imbedded metal
30 structure. Unfortunately, at RF, millimeter, and microwave frequencies this metal run creates

to a via or imbedded metal structure, which creates additional inductive parasitic inductance and damages the performance of the circuit. Moving the device over the physical transition means that the device will have a random thickness variation, often referred to as necking of passive devices thickness as the device transitions from the substrate to the via or imbedded metal structure. One example of this is the creation of a capacitor where the metal electrodes and dielectric layer are thinner over the substrate metal transition. Variations in the thickness results in random capacitors across the die/substrate, creating random capacitance and filters RF, millimeter, and microwave circuits making the circuit/device. Placing a filter, capacitor, other passive device or/or active device adjacent and greater than 250 μm from the via induces parasitic inductance from the metal trace between the passive device and the via/imbedded metal structure.

[0006] The passive device can be placed in conjunction with active devices and can be combined to make a wide array of RF systems and subsystems including: antennas with gain, RF Circulators, RF Isolators, RF Combiners, RF Couplers, RF Splitters, Transformers, Switches, Multiplexors, Duplexers, and/or Diplexers that are connected by via as well as metal lines and via to each other and ground planes.

[0007] Constructing passive devices as close as possible to the via that shunts parasitic and electrical noise to a ground plane dramatically improves performance and reduces the die size for RF, microwave, and millimeter electronic systems. This invention provides a general solution to the constructing passive device in intimate proximity to metalized via or buried structure eliminating connecting to a ground plane and eliminating the random device performance and parasitic across the device substrate metal transition.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying figures and in which:

FIG. 1 shows a schematic of an annular RF shunt capacitor.

FIG. 2 shows a schematic of an annular RF shunt capacitor with dimensional information between the adjacent annular element and the via.

FIG. 3 shows a schematic of a cross section for annular RF shunt capacitor.

FIGS. 4A to 4F show a step-by-step method of making the device of the present invention. FIGS. 4A and 4B show cross-sectional side views of two of the steps of the method. FIGS. 4C to 4F show the remained of the steps for making the annular capacitor RF, microwave and millimeter (MM) wave systems of the present invention.

5

DETAILED DESCRIPTION OF THE INVENTION

[0009] While the production and use of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable, inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make
10 and use the invention and do not delimit the scope of the invention. To facilitate the understanding of this invention, a number of terms are defined below. Terms defined herein have meanings as commonly understood by a person of ordinary skill in the areas relevant to the present invention.

[0010] In one embodiment, the present invention includes a method for creating a substrate,
15 an annular capacitor structure where the adjacent edge of the capacitive structure less than 250 μm of the via or imbedded metal structure in the substrate eliminates or minimizes the inductance associated with the metal line.

[0011] FIG. 1 shows an example of the device 10, that includes ports 12 and 14 that connect to a top metal 16, which can be a copper layer that connected to, or shunted, to a through-via
20 hole 18. The design of the present invention reduces the variability from the capacitor build. In this design, the through-via hole is formed but does not affect the capacitor, thus eliminating that variable from design consideration(s). A top insulator 20 is positioned between the top metal 16 at the via 18, and a second metal layer 22 is deposited on the insulator 20. The structure is formed in a substrate 24.

25 [0012] FIG. 2 shows an internal view of the device 10, that shows the gap 26, between the through-hole via 18 and the first metal layer 16. Ports 12 and 14 that connect to a top metal 16, which can be a copper layer that connected to, or shunted, to a through-via hole 18.

[0013] FIG. 3 is a cross-section side view of the device 10. Ports 12 and 14 are shown in this configuration as being on opposite sides of the through-hole via 18, which is isolated from the
30 top metal layer 16 and the second top metal layer 22, by insulator 20. A bottom metal ground plane 28 is depicted connected to through-hole via 18.

[0014] Table 1 and FIGS. 4A to 4F show a step-by-step method of making the device 10 of the present invention. The process flow to create a planarized surface in a substrate with dissimilar materials to eliminate vertical transitions from a substrate to an added material is as follows:

Step 1. Lap and polish a substrate with the metal structures.

Step 2. Machine or etch a via or trench in the substrate, as shown in FIG. 4A as a cross-sectional side view that includes the substrate 24 into which the trench or via 18 is cut or etched.

Step 3. Fill the via, ground plane or trench with copper using any of a number of processes including chemical vapor deposition (CVD), silkscreen, atomic layer deposition (ALD) or other, as shown in cross-sectional side view in FIG. 4B that shows the substrate 24 into which the trench or via 18 is cut or etched, and the metal filled through-hole via 18 and a ground plane 28. One example is to selectively deposit tantalum on the sidewalls of the via or trench structures and then deposit copper organometallic by a silkscreen deposit. The filled substrate is then heated in argon to drive off /decompose the organic material and densify the copper. For the copper deposited, the adhesion layer is a few hundred angstroms of tantalum. The adhesion layer may be removed over the metal. The thickness of the metal/non substrate material needs to be between two times and ten times the transition step. The thickness of the deposited material can be measured in real time using a variety of techniques including, e.g., a crystal oscillator during a vacuum deposition processes, where one side of the via is connected to a ground plane.

Step 4. Coat the front side of the substrate with a photoresist and expose and develop an annular shape that circumscribes the via.

Step 5. Using a DC sputtering system, coat the photoresist with a copper adhesion layer of a few hundred angstroms of tantalum. Coat the substrate with 2 μm of copper to form the bottom electrode, as shown in FIG. 4C, which is a top-view of the device 10. The substrate 24 is shown with through-hole via 18, on which a bottom metal annular patter 30 is shown.

Step 6. Remove the photoresist to form a bottom electrode connected to the via.

Step 7. Coat the front side of the substrate with a photoresist and expose and develop an annular shape that circumscribes the via, where the inner radii is between 2 μm and 300 μm from the outer edge of the metal filled via and external radii of the pattern is between 10 μm and 500 μm respectively.

Step 8. Using ALD or other deposition, deposit between 0.1 μm and 10 μm of a dielectric

material, where the dielectric material has a dielectric constant between 2 and 2,000, as shown in FIG. 4D, which is a top view of the device 10. The substrate 24 is shown in which a gap 32 is depicted between the through-hole via 18 and the second metal layer 22. Also depicted is the insulator 20 (also referred to as a dielectric material).

Step 9. Remove the photoresist to form a dielectric region that is at least 1 μm larger than the bottom electrode.

Step 10. Coat the front side of the substrate with a photoresist and expose and develop an annular shape that is at least 2 μm greater than the dielectric layer and where one side transitions to other active or passive devices in the circuit.

Step 11. Using a DC sputtering system, coat the photoresist with a copper adhesion layer is a few hundred angstroms of tantalum. Coat the substrate with 2 μm of copper to form the top electrode.

Step 12. Remove the photoresist to form a top electrode for the capacitor structure, which is depicted in FIG. 4E, which shows the device 10, that now includes top metal layer 22, disposed on the insulator 20, and includes the gap 26, the bottom metal layer 16, the through-hole via 18, and the first metal layer 16.

Step 13. Coat the front side of the substrate with a photoresist and expose and develop a connecting metal line to both sides of the bottom metal of the annular structure.

Step 14. Using a DC sputtering system, coat the photoresist with a copper adhesion layer is a few hundred angstroms of tantalum. Coat the substrate with 2 μm of copper to form the top electrode. FIG. 4F shows the device 10, which now includes all the layers and ports 12 and 14.

[0015] It will be understood that particular embodiments described herein are shown by way of illustration and not as limitations of the invention. The principal features of this invention can be employed in various embodiments without departing from the scope of the invention. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, numerous equivalents to the specific procedures described herein. Such equivalents are considered to be within the scope of this invention and are covered by the claims.

[0016] All publications and patent applications mentioned in the specification are indicative of the level of skill of those skilled in the art to which this invention pertains. All publications and patent applications are herein incorporated by reference to the same extent as if each

individual publication or patent application was specifically and individually indicated to be incorporated by reference.

[0017] The use of the word “a” or “an” when used in conjunction with the term “comprising” in the claims and/or the specification may mean “one,” but it is also consistent with the meaning of “one or more,” “at least one,” and “one or more than one.” The use of the term “or” in the claims is used to mean “and/or” unless explicitly indicated to refer to alternatives only or the alternatives are mutually exclusive, although the disclosure supports a definition that refers to only alternatives and “and/or.” Throughout this application, the term “about” is used to indicate that a value includes the inherent variation of error for the device, the method being employed to determine the value, or the variation that exists among the study subjects.

[0018] As used in this specification and claim(s), the words “comprising” (and any form of comprising, such as “comprise” and “comprises”), “having” (and any form of having, such as “have” and “has”), “including” (and any form of including, such as “includes” and “include”) or “containing” (and any form of containing, such as “contains” and “contain”) are inclusive or open-ended and do not exclude additional, unrecited elements or method steps. In embodiments of any of the compositions and methods provided herein, “comprising” may be replaced with “consisting essentially of” or “consisting of”. As used herein, the phrase “consisting essentially of” requires the specified integer(s) or steps as well as those that do not materially affect the character or function of the claimed invention. As used herein, the term “consisting” is used to indicate the presence of the recited integer (e.g., a feature, an element, a characteristic, a property, a method/process step or a limitation) or group of integers (e.g., feature(s), element(s), characteristic(s), property(ies), method/process steps or limitation(s)) only.

[0019] The term “or combinations thereof” as used herein refers to all permutations and combinations of the listed items preceding the term. For example, “A, B, C, or combinations thereof” is intended to include at least one of: A, B, C, AB, AC, BC, or ABC, and if order is important in a particular context, also BA, CA, CB, CBA, BCA, ACB, BAC, or CAB. Continuing with this example, expressly included are combinations that contain repeats of one or more item or term, such as BB, AAA, AB, BBC, AAABCCCC, CBBAAA, CABABB, and so forth. The skilled artisan will understand that typically there is no limit on the number of items or terms in any combination, unless otherwise apparent from the context.

[0020] As used herein, words of approximation such as, without limitation, “about”, “substantial” or “substantially” refers to a condition that when so modified is understood to not

necessarily be absolute or perfect but would be considered close enough to those of ordinary skill in the art to warrant designating the condition as being present. The extent to which the description may vary will depend on how great a change can be instituted and still have one of ordinary skilled in the art recognize the modified feature as still having the required characteristics and capabilities of the unmodified feature. In general, but subject to the preceding discussion, a numerical value herein that is modified by a word of approximation such as “about” may vary from the stated value by at least $\pm 1, 2, 3, 4, 5, 6, 7, 10, 12$ or 15%.

[0021] All of the compositions and/or methods disclosed and claimed herein can be made and executed without undue experimentation in light of the present disclosure. While the compositions and methods of this invention have been described in terms of preferred embodiments, it will be apparent to those of skill in the art that variations may be applied to the compositions and/or methods and in the steps or in the sequence of steps of the method described herein without departing from the concept, spirit and scope of the invention. All such similar substitutes and modifications apparent to those skilled in the art are deemed to be within the spirit, scope and concept of the invention as defined by the appended claims.

What is claimed is:

1. A method for creating a capacitor for RF, millimeter or microwave device that at least partially circumscribes a metal filled via or trench based transmission line that connects a passive device or an active device and one or more ground planes using the steps of:
 - 5 cutting a trench or via in a first surface of a substrate;
filling the trench or via with a first metal layer, and optionally form on a second surface of the substrate opposite the first surface a ground plane;
coating, exposing, and developing photoresist into a first annular shape that circumscribes the trench or via on the first surface of the substrate;
 - 10 depositing a first metal layer on the first surface of the substrate;
coating, exposing, and developing photoresist into a second annular shape that circumscribes the trench or via on the first surface of the substrate, where an inner radii of the second annular shape is between 2 μm and 300 μm from an outer edge of the metal filled via or trench, and an external radii of the second annular shape is between 10 μm and
15 500 μm ;
depositing a dielectric material on the first surface of the substrate to form a dielectric layer;
coating, exposing, and developing photoresist in third annular shape on the first surface of the substrate, wherein the third annular shape is at least 2 μm greater than the
20 dielectric layer and wherein at least a portion of the third annular shape transitions to one or more active or passive devices of a circuit;
depositing a second metal layer on the first surface of the substrate;
coating, exposing, and developing photoresist to connect the second metal between the first and second surfaces of the substrate; and
 - 25 depositing a metal to connect the first metal layer and a ground plane on the second surfaces of the substrate to form an electrode on the first surface of the substrate.
2. The method of claim 1, further produces a transition less than 0.1 μm .
3. The method of claim 1, further comprising an adhesion layer between at least one of a side or bottom on the trench or via in the substrate prior to depositing the first metal layer.

4. The method of claim 1, further comprising depositing an adhesion layer prior to depositing the second metal layer.
5. The method of claim 1, wherein the metal is copper, silver, gold, aluminum, or a metal alloy.
- 5 6. The method of claim 1, wherein the one or more active or passive devices is at least one of: RF Filters, RF Circulators, RF Isolators, Antenna, Impedance Matching Elements, 50 Ohm Termination Elements, Integrated Ground Planes, RF Shielding Elements, EMI Shielding Elements, RF Combiners, RF Splitters, Transformers, Switches, power splitters, power combiners, Duplexer, or Diplexers on the first surface of the substrate to one or more
10 input/output ports.
7. The method of claim 6, wherein the device is a RF Circuit that eliminates at least 95% of the RF parasitic signal associated with the transition from a substrate to the embedded metal.
8. The method of claim 6, wherein the device is a RF Circuit that eliminates at least 85%
15 of the RF parasitic signal associated with the packaging a mount elements to a substrate.
9. The method of claim 6, wherein the device is a RF Circuit that eliminates at least 75% of the RF parasitic signal associated with the packaging a mount elements to a substrate.
10. The method of claim 1, wherein the substrate or the dielectric is a photodefinable glass.
- 20 11. The method of claim 1, wherein the electrode comprises a first and a second port.
12. An electrode comprising a capacitor for RF, millimeter or microwave device that at least partially circumscribes a metal filled via or trench based transmission line that connects a passive device or an active device and one or more ground planes, wherein the electrode is made by a method comprising:
- 25 cutting a trench or via in a first surface of a substrate;
- filling the trench or via with a first metal layer, and optionally on a second surface of the substrate opposite the first surface;
- coating, exposing, and developing photoresist into a first annular shape that circumscribes the trench or via on the first surface of the substrate;
- 30 depositing a first metal layer on the first surface of the substrate;

coating, exposing, and developing photoresist into a second annular shape that circumscribes the trench or via on the first surface of the substrate, where an inner radii of the second annular shape is between 2 μm and 300 μm from an outer edge of the metal filled via or trench, and an external radii of the second annular shape is between 10 μm and 500 μm ;

depositing a dielectric material on the first surface of the substrate to form a dielectric layer;

coating, exposing, and developing photoresist in third annular shape on the first surface of the substrate, wherein the third annular shape is at least 2 μm greater than the dielectric layer and wherein at least a portion of the third annular shape transitions to one or more active or passive devices of a circuit;

depositing a second metal layer on the first surface of the substrate;

coating, exposing, and developing photoresist to connect the second metal between the first and second surfaces of the substrate; and

depositing a metal to connect the first metal layer and a ground plane on the second surfaces of the substrate to form the electrode on the first surface of the substrate.

13. The method of claim 1, further produces a transition less than 0.1 μm .

14. The method of claim 1, further comprising an adhesion layer between at least one of a side or bottom on the trench or via in the substrate prior to depositing the first metal layer.

15. The method of claim 1, further comprising depositing an adhesion layer prior to depositing the second metal layer.

16. The method of claim 1, wherein the metal is copper, silver, gold, aluminum, or a metal alloy.

17. The method of claim 1, wherein the one or more active or passive devices is at least one of: RF Filters, RF Circulators, RF Isolators, Antenna, Impedance Matching Elements, 50 Ohm Termination Elements, Integrated Ground Planes, RF Shielding Elements, EMI Shielding Elements, RF Combiners, RF Splitters, Transformers, Switches, power splitters, power combiners, Duplexer, or Diplexers on the first surface of the substrate to one or more input/output ports.

18. The method of claim 6, wherein the device is a RF Circuit that eliminates at least 95% of the RF parasitic signal associated with the transition from a substrate to the embedded

19. The method of claim 6, wherein the device is a RF Circuit that eliminates at least 85% of the RF parasitic signal associated with the packaging a mount elements to a substrate.
20. The method of claim 6, wherein the device is a RF Circuit that eliminates at least 75% of the RF parasitic signal associated with the packaging a mount elements to a substrate.
- 5 21. The method of claim 1, wherein the substrate or the dielectric is a photodefinable glass.
22. The method of claim 1, wherein the electrode comprises a first and a second port.

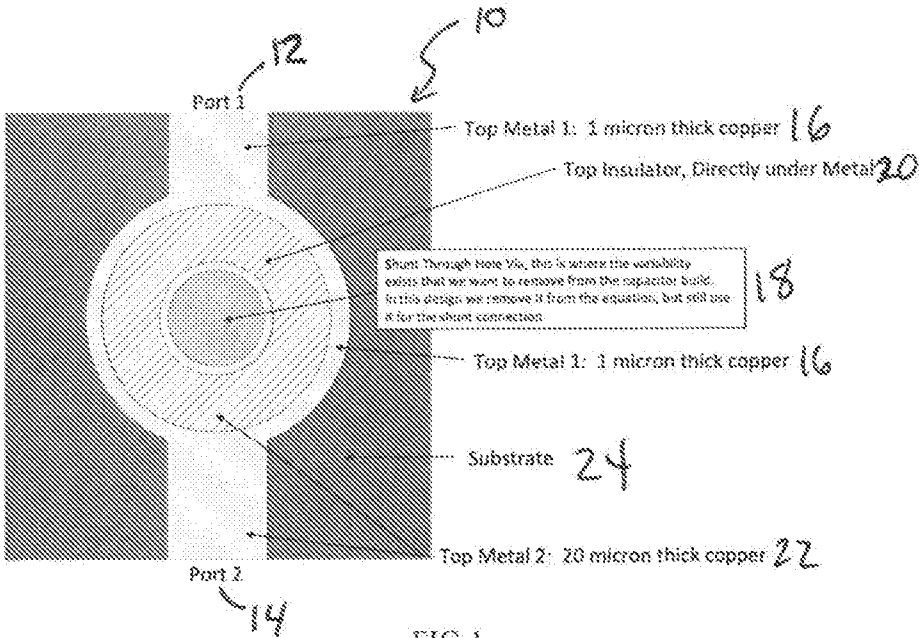


FIG 1.

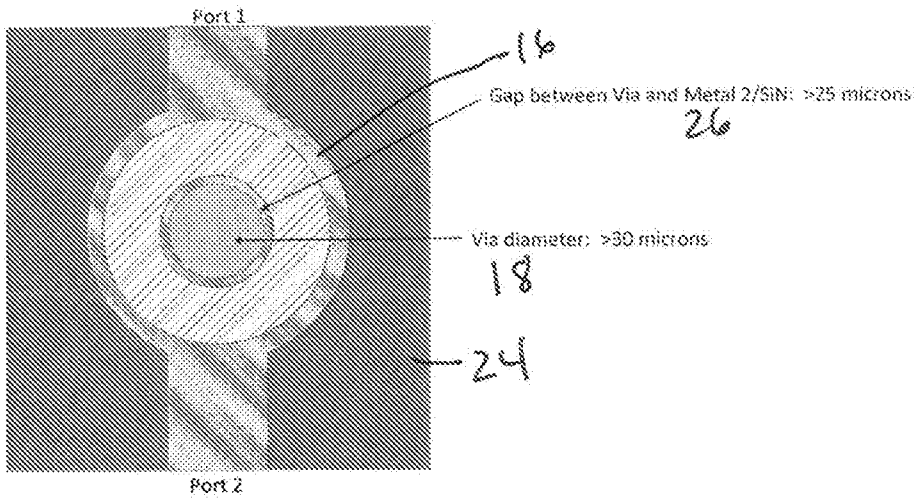


FIG 2.

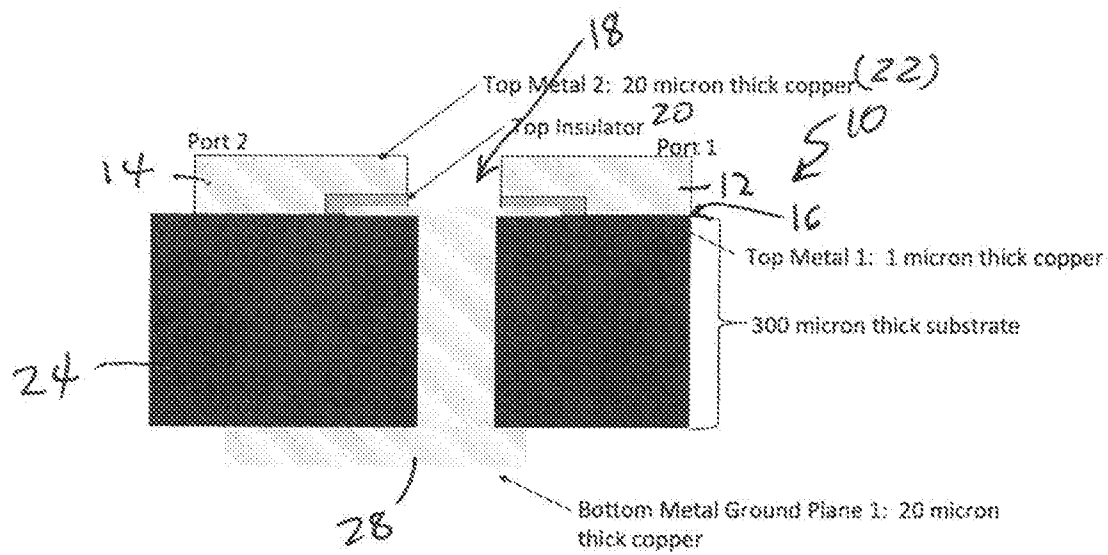


FIG. 3.

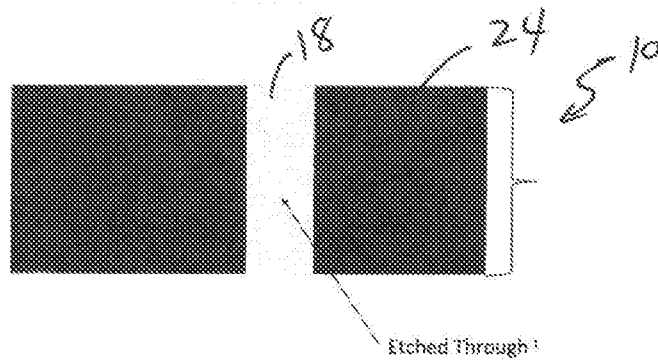


FIG. 4A

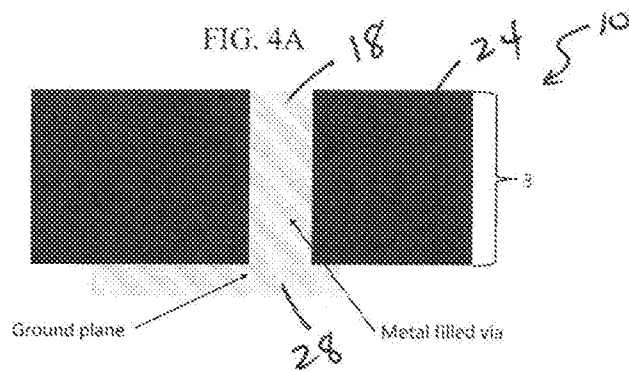


FIG. 4B

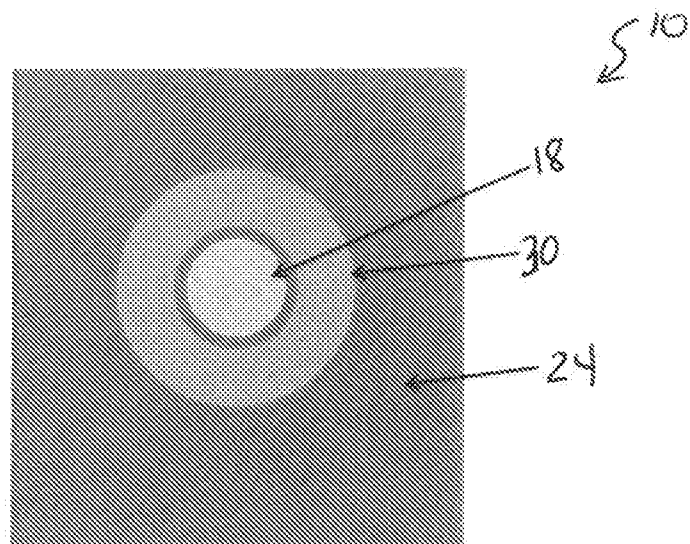


FIG. 4C

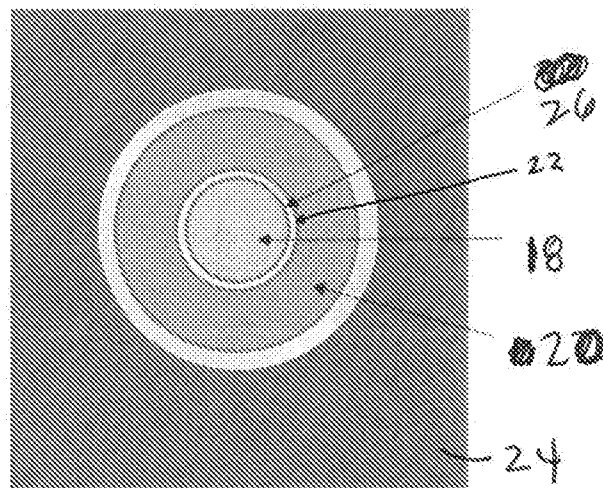


FIG. 4D

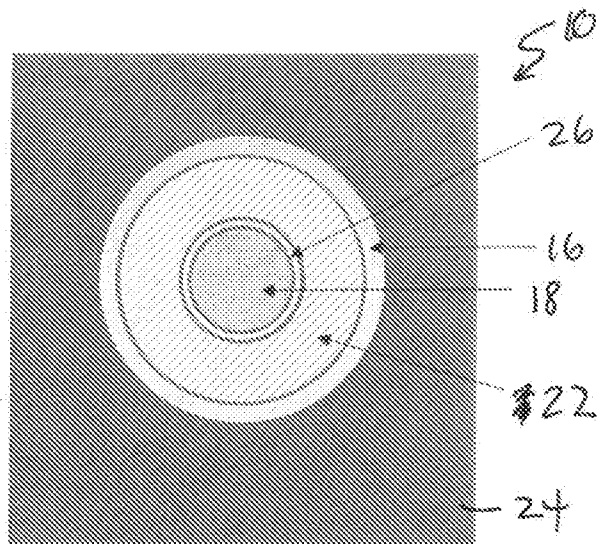


FIG. 4E

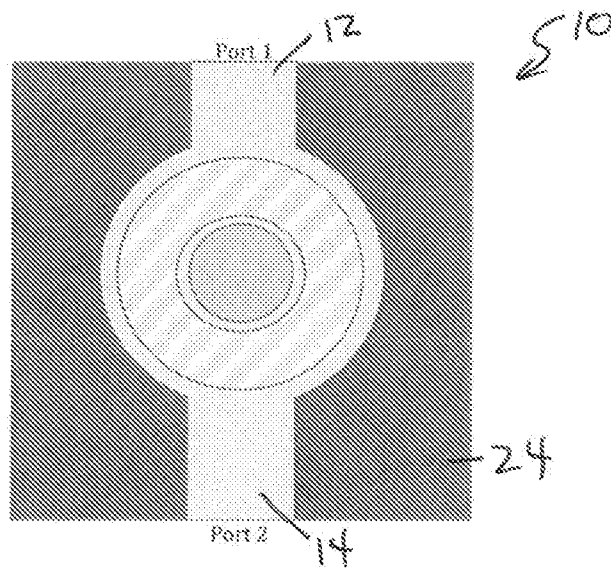


FIG. 4F

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2019/068590

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/20; H01L 27/108; H01L 49/02 (2020.01)

CPC - H01L 27/10861; H01L 27/10864; H01L 27/10867; H01L 28/40; H01L 29/945 (2020.02)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 257/301; 438/243; 438/244; 438/386; 438/387 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7,439,128 B2 (DIVAKARUNI et al) 21 October 2008 (21.10.2008) entire document	1-22
A	US 2013/0183805 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION et al) 18 July 2013 (18.07.2013) entire document	1-22
A	US 2012/0161330 A1 (HLAD et al) 28 June 2012 (28.06.2012) entire document	1-22
A	US 5,779,521 A (MUROYAMA et al) 14 July 1998 (14.07.1998) entire document	1-22

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 February 2020

Date of mailing of the international search report

05 MAR 2020

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Facsimile No. 571-273-8300

Authorized officer

Blaine R. Copenheaver

PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774