

Sept. 6, 1966

K. L. SMITH ET AL

3,270,850

RECORDING DEVICE

Filed Aug. 29, 1961

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CHANNEL

FIG. 1A

TIME	0	1	2	3	4	5	6	7	8
		+	.	:	"	@	,	*	o
12.00	20.63	34.62	63.32	76.17	81.18	51.34	09.32	938.0	
12.01	20.63	34.43	64.28	76.49	81.99	51.71	09.31	914.9	
12.02	20.64	34.34	64.32	76.98	82.92	52.61	10.93	884.0	
12.03	20.64	34.19	64.64	76.45	82.78	52.48	10.47	874.0	
12.04	20.64	34.42	65.64	76.92	83.57	48.44	10.91	835.2	
12.05	20.63	34.14	66.42	75.36	83.60	46.56	10.28	817.7	
12.06	20.65	33.72	68.43	75.79	83.31	46.92	11.57	751.7	
12.07	20.63	33.66	67.29	75.19	83.93	46.58	10.78	707.4	
12.08	20.64	32.10	67.10	76.56	83.10	47.59	09.92	654.9	
12.09	20.64	31.51	67.32	76.90	82.15	47.01	08.78	604.5	
12.10	20.65	31.47	67.33	76.20	81.79	47.87	07.57	566.5	
12.11	20.62	31.62	68.27	76.46	80.98	48.21	06.28	521.3	
12.12	20.64	30.68	66.28	77.67	80.28	48.07	05.91	479.1	
12.13	20.64	29.41	64.80	77.84	81.57	49.48	04.47	430.4	
12.14	20.65	30.61	62.68	77.95	81.78	49.46	03.93	385.7	
12.15	20.63	30.10	61.24	76.99	81.92	50.04	02.20	353.6	
12.16	20.64	30.75	60.18	76.00	82.99	51.25	01.29	301.1	
12.17	20.63	31.42	60.90	76.92	83.00	52.10	01.88	259.2	
12.18	20.63	31.02	60.32	76.78	85.95	53.61	02.35	228.0	
12.19	20.64	32.45	60.27	76.57	87.84	53.81	03.72	207.6	
12.20	20.63	32.62	59.30	75.28	89.67	53.69	04.97	198.3	
12.21	20.63	33.40	59.10	75.91	90.46	53.29	05.11	180.0	
12.22	20.64	34.95	58.86	75.47	91.20	52.62	05.13	173.2	
12.23	20.62	35.99	58.53	76.93	92.90	52.68	05.03	139.0	
12.24	20.65	35.53	58.49	76.31	92.56	52.06	05.81	103.1	
12.25	20.65	35.55	58.30	76.60	92.19	52.40	03.48	079.3	
12.26	20.64	35.00	58.12	76.80	92.79	51.52	03.03	044.7	
12.27	20.62	34.85	57.80	76.29	92.36	50.43	02.36	079.1	
12.28	20.64	34.07	57.90	76.88	91.92	49.13	03.92	102.8	
12.29	20.65	33.63	58.22	76.35	91.45	48.64	03.80	135.7	
12.30	20.64	32.50	58.34	77.38	90.98	48.96	02.67	154.5	

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Sept. 6, 1966

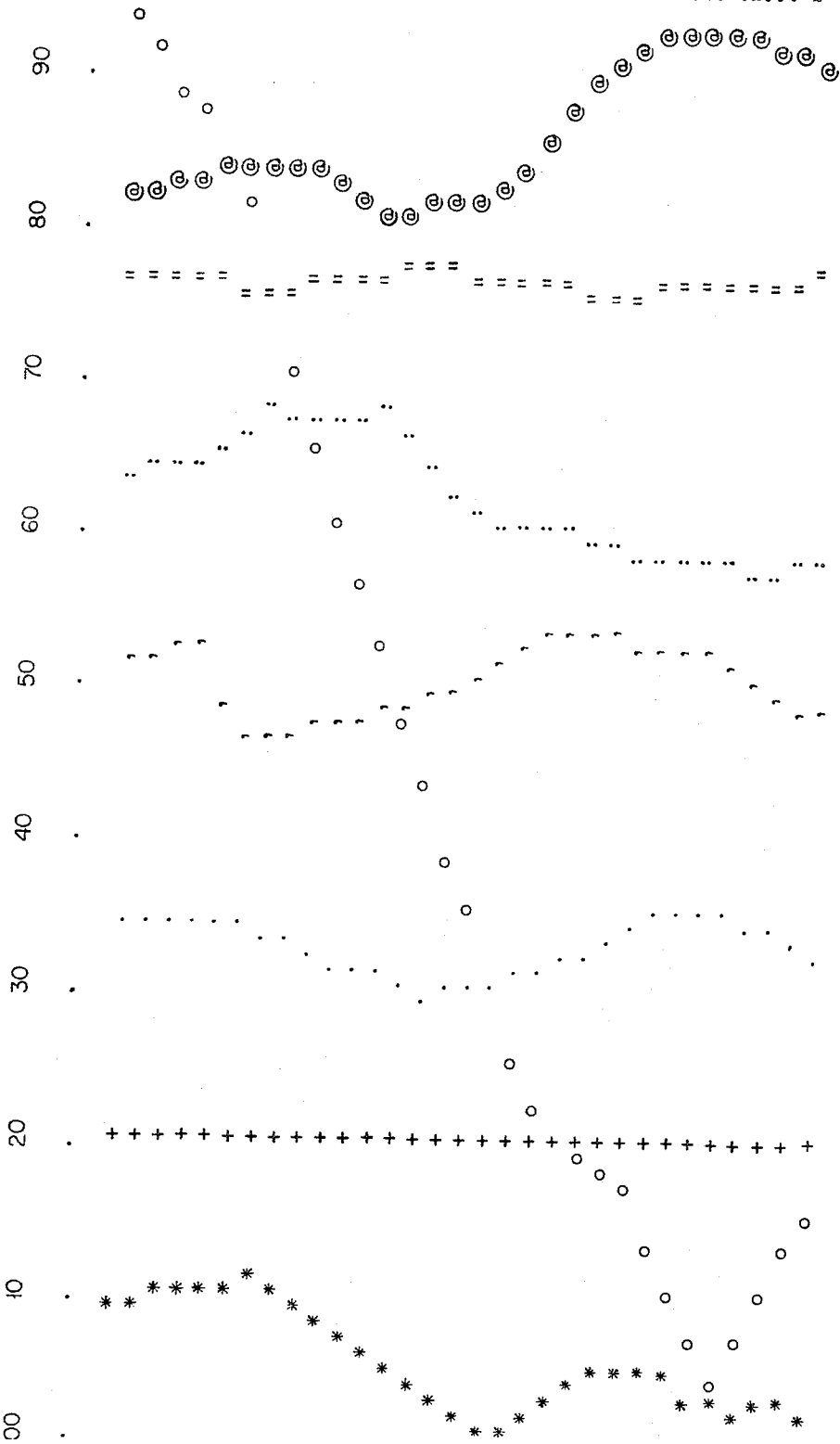
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FIG. 1B



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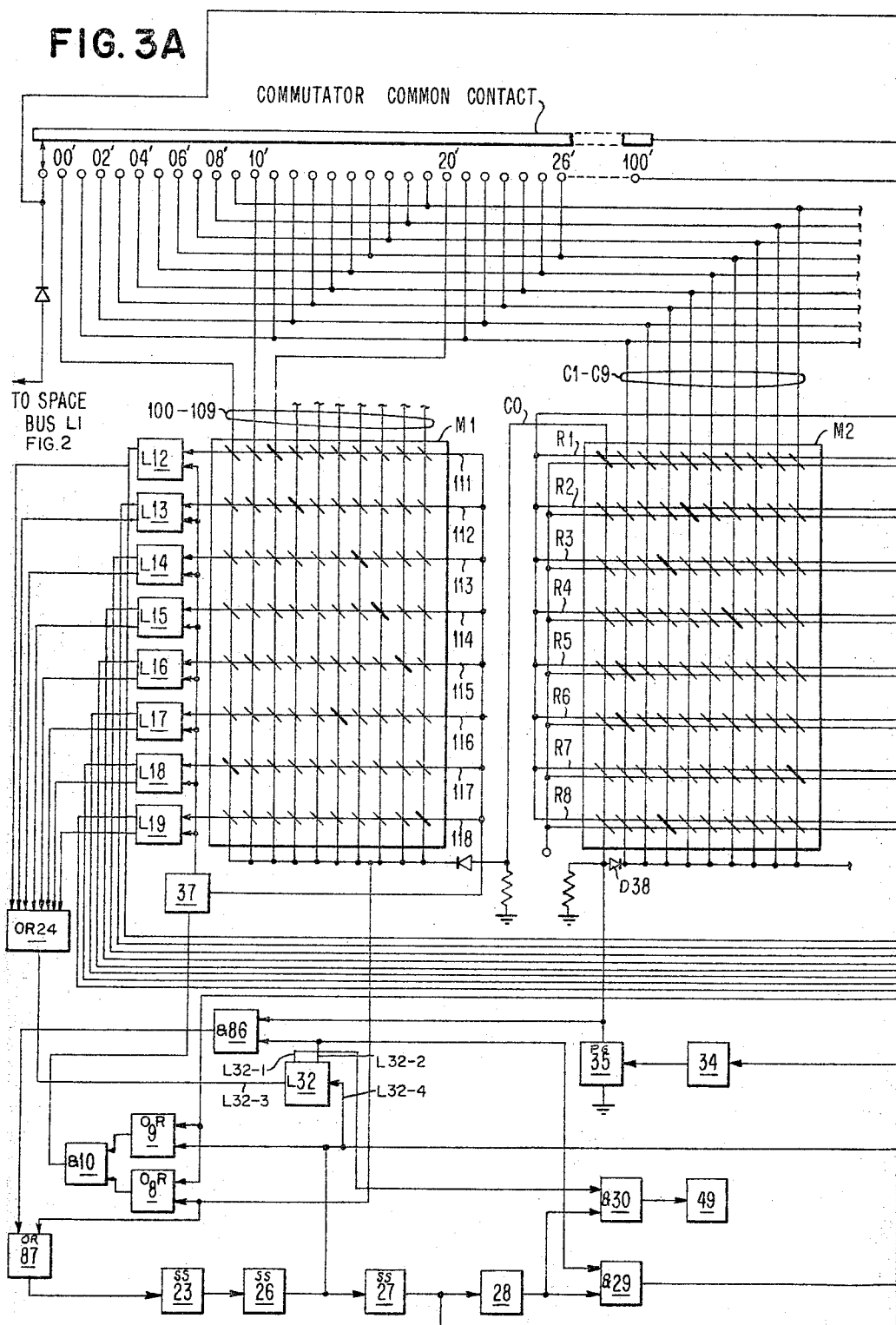
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FIG. 3A



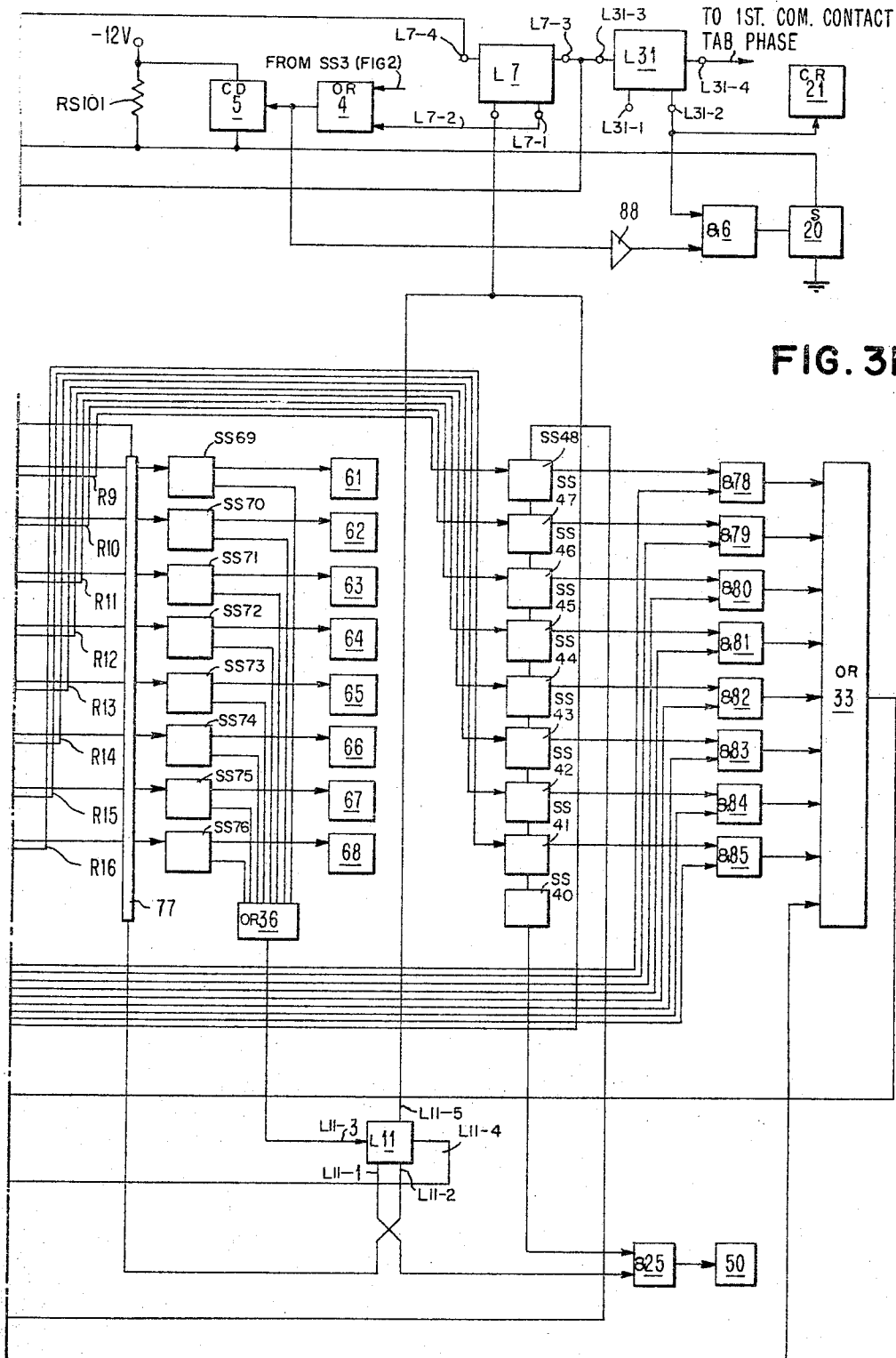
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RECORDING DEVICE

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Filed Aug. 29, 1961, Ser. No. 134,687

2 Claims. (Cl. 197-19)

This invention relates to record-controlled accounting machines and more particularly to a printing device for printing tabular and graphical representations of a plurality of variable data.

According to the present invention a tabulator is provided having a print mechanism for printing on a record medium the value of an input variable applied to said tabulator in digitized form and for printing a symbol representing the source of said variable at a position on said medium determined by the value of said variable, including means for applying said digitized value to said print mechanism to print the value representative thereof on said record medium, a store for storing the digitized value of the input variable, means for scanning said store and reading out the stored value therefrom and means for applying said read out value to the print mechanism to print said symbol in said position.

It is, therefore, an object to provide a printing apparatus, which in response to digital signals manifestive of the magnitude of a variable data reported on a plurality of data input channels produces a printed table of the respective digital data values, as well as graphical symbols displaced with respect to an index to graphically represent the magnitude of the respective variables.

A further object of this invention is to provide a printing device of the typewriter variety with a digital storage device and control circuits such that the printing device will produce a record in accordance with the foregoing object.

Still another object is to provide a printing apparatus in accordance with the foregoing objects wherein the digital data is stored in a matrix storage device of bistable elements during the printing of the tabular digital values and read out in ascending order under control of the columnar position of the printing device to select and print the respective graphical symbols in the appropriate columnar positions.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

FIGS. 1A and 1B taken together show a chart produced by the tabulator of the present invention in which FIG. 1A shows the digital values and FIG. 1B shows the corresponding graphical plot of the same data.

FIG. 2 shows the electronic circuits used during the tabulating phase.

FIGS. 3A and 3B, taken together, and joined from left to right show the electronic circuits used during the graph plotting phase.

The tabulator can conveniently be considered to comprise two sections. The first, a mechanical section, including an electric typewriter having its digital, and certain of its functional and symbol keys, arranged for solenoid operation, and having a commutator adapted to indicate the print position of the typewriter carriage. The second section is predominantly electronic, consisting of circuits adapted to scan a number of data sources and, in conjunction with typewriter carriage position information supplied by the commutator, to energize the

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typewriter solenoids in such a manner that the input data is printed in accordance with a specified format.

In the preferred embodiment to be described, the electronic section is adapted to scan eight data sources and the typewriter carriage has 164 print positions, the commutator being in the form of an insulating strip carrying 164 independent contacts mounted on the frame of the typewriter and a common contact strip. A wiper contact is mounted on the carriage so as to bridge in turn each independent contact and the common contact strip as the carriage is stepped along. The following keys of the typewriter are adapted for solenoid operation:

Digits 0-9
Carriage Return
Decimal Point
Tabulate
Space Bar

Eight selected symbol keys are also adapted for solenoid operation, each one representing a different data source.

The tabulator operates in two distinct phases during each complete traverse of the typewriter carriage:

(a) The tabulation phase, during which the data sources are scanned and the various data values are printed in assigned positions and at the same time the two most significant digits of each value are stored in a magnetic memory.

(b) The plotting phase, during which the values stored in memory during the tabulation phase are read out in ascending order of magnitude and plotted by appropriate energization of the tabulate, space and symbol solenoids in positions corresponding to their magnitudes, each point being printed by the symbol key associated with that data source from which the stored value has been derived.

The record produced by the machine is thus in the form shown in FIG. 1A, in which data appearing on eight channels, 1-8, have been tabulated and plotted over a period of 31 minutes, as indicated by the output of a digital clock which has been applied to channel 0.

In order to simplify the description of the electronic circuits of the machine, the two phases will be dealt with separately in the following description.

Printing phase

The operation of the tabulator during the printing phase when the values of all the variable quantities are sequentially fed thereto will now be described with reference to FIG. 2.

The values of the variable quantities to be recorded may be derived from sources which produce an analogue of a quantity being measured, for example temperature, the analogue value being digitized and set up on a plurality of switches which in the preferred embodiment comprise four ten position switches. Similarly the output from the digital clock is set up on a four bank ten position switch which is connected to channel 0. Since the output of the digital clock is only required to indicate the time at which the other eight channels are sampled, no further description of its function is deemed necessary as the printing-out of the time follows the same sequence of operations as the following description of the tabulation of the values derived from the eight sources of data with the exception that none of the digits of the time value is stored.

Before the initiation of the printing phase, the carriage of the typewriter is positioned so that contact 1 of the commutator is connected to the common contact thereof. This position corresponds to the carriage being moved to the right of the typewriter.

When tabulation of the values set up on each channel switch is required, a start relay (not shown) is energized

closing the start relay contact RL1, thus connecting RS2 between the commutator contact 1 and earth.

Since the commutator is normally returned to -12 v. via a 2.2K resistor RS101, a positive pulse of almost 12 v. amplitude is produced when the contact 1 of the commutator makes with the common contact firing a 10 ms. single shot SS1. The leading edge of the output pulse from SS1 fires a 5 ms. single shot SS2 and the trailing edge of the output pulse therefrom initiates a 100 microsecond single shot SS3. Thus a 100 microsecond output pulse occurs 5 ms. after a positive pulse is applied to the input, and cannot occur again until a further 5 ms. has elapsed. This arrangement ensures that the system cannot be re-triggered either by contact bounce of the start relay or by any subsequent pulses occurring on the trigger line within the 10 ms. period provided by SS1.

The 100 microsecond pulse is fed via an OR gate OR4 to the current driver circuit CD5; the circuit CD5 includes an NPN transistor, the collector load of which is switched by the commutator. In the first position of the commutator, its load consists of the 33 ohms resistor RS2, and a 12 v. negative pulse of 100 microsecond duration will therefore appear across this resistor. Since the live end of this resistor is connected, via the space bus bar L1, to the input of a space solenoid drive circuit 50, the space key is actuated and the carriage steps on one position. The 100 microsecond pulse developed across resistor RS2 occurs only 5 ms. after the initiating pulse so that the 10 ms. single shot SS1 is still in a fired condition and cannot be re-triggered.

Since the mechanical inertia of the typewriter introduces a delay of more than 5 ms., the single shot SS1 can be triggered by the application of a positive pulse as the commutator moves to the next contact. The commutator contacts are arranged to have a break before make action and, as the wiper is returned to -12 v. via the 2.2K resistor RS101, contact 1 will jump to -12 v. as the wiper leaves the contact 1 and then back to approximately earth as contact 2 is made, thereby producing the necessary positive pulse to fire SS1 and supply a 100 microsecond pulse to commutator contact 2 after the 5 ms. delay introduced by SS2.

When the carriage is stepped to a position corresponding to contact 2, a 100 microsecond pulse is applied by the driver CD5 via the first plot digit switch SW-1 to one of the solenoid drive circuits 51 to 60 by sensing the increase in potential drop across the resistors RS3-RS12 thus energizing the solenoid operating the character corresponding to the position of the switch SW-1 and causing printing of that character of the digitized value set up on channel 1. Printing of this first character escapes the carriage one character position to commutator contact 3, and a further 100 microsecond pulse resulting from the application of a positive pulse to the 10 ms. single shot SS1 caused by the stepping action of the carriage is applied to the second plot digit switch SW-2. Printing of the next highest order digit of the value set up on channel 1 is effected by one of the solenoids 51 to 60 that is connected to the switch contact of the second plot digit switch corresponding to that value.

In the case of channel 1, the decimal point of the value set up on the four switches SW1-4 occurs between the second and third digits and thus the commutator position contact 4 is connected to a decimal point bus bar L2, which is connected to a solenoid 22 operable to cause print out of a decimal point, and a 33 ohms resistor RS13. Thus, when the carriage is escaped a further position after printing out the second digit of the value set up on channel 1, the next 100 microsecond pulse is effective to energize the solenoid 22 and print out a decimal point in the required position. It will be understood that the decimal point can be printed in any position by connecting the decimal point bus bar to the appropriate one of the five commutator contacts allocated to each channel. For example in channel 8 (FIG. 1) the decimal point occurs

between the third and fourth digits and hence the commutator contact 4 of the group of five contacts assigned to channel 8 on the commutator is connected to the decimal point bus bar L2.

After the decimal point has been printed, the carriage escapes a further print position and the third digit of the value set up on channel 1 is printed followed by printing of the fourth character in the same manner as described above with reference to the printing of the first two digits.

Contacts 7 and 8 of the commutator are connected to the space solenoid 50, the latter position being connected to the commutator via a relay contact RL2. When the carriage is stepped on to the 7th contact of the commutator by the printing out of the fourth digit, a 100 microsecond pulse causes the carriage to step on one digit position to the 8th commutator contact.

The relay contacts RL2 are provided between the 8th commutator position and the space solenoid 50 so that print out of the values set up on channel 2 is not initiated until a signal is received indicating that the values to be printed are set up on the four bank ten position switch of that channel. This signal is effective to energize a relay (not shown) closing the contacts RL2 to cause energization of the space solenoid 50 stepping the carriage on to commutator contact 9 which is connected to the first plot digit switch of the 4 bank 10 position switch of channel 2. Thus the value set up on the 4 bank switch of channel 2 is printed out in the same manner as the value set up on the 4 bank switch SW1-4 of channel 1. If no interruption between printing out of the values set up on the switches of each channel is required, then the relay and its associated contacts can be omitted and commutator contact 9 and the other corresponding commutator contacts between each set of contacts assigned to each channel can be connected direct to the space bus bar L1 and to the space solenoid 50.

A specific example of the printing of the first value 20.63 set up in channel 1 (see FIG. 1) will now be given together with a description of how the two most significant digits 2 and 0 are stored in the magnetic core memory. The magnetic core memory comprises two core matrices M1 and M2, the first or tens matrix M1 having 8 row conductors connected to the movable contacts of the first plot digit switches SW-1 of the 8 input channels. The column conductors of the tens and units matrix are connected in series by the wires collectively labelled 0.9, each conductor being connected between a solenoid drive unit and the corresponding fixed contact of the input channel switches. All the corresponding fixed contacts of all the input channel switches are connected in parallel. Each matrix comprises 80 cores located at the intersections of the row and column conductors, a predetermined magnetic state of a core indicating storage of a value designated by the column in which that core is located and assigned to the channel designated by the intersecting row conductor. To set a core to a predetermined magnetic state coincident energization of the row and column conductors threading the core is required; a current through either the column or row conductor is not sufficient to set the core.

As hereinbefore described, the tabulation of the first non-plot digit is effected by a 100 microsecond pulse from the single shot SS3 being routed via driver CD5, commutator contact 2, contact 2 of the first plot digit switch SW-1, channel 1 row conductor of the tens matrix M1 and the column 2 conductor of the tens and units matrix M1 and M2 respectively to energize the solenoid 53 to cause print out of the digit 2. Thus coincident energization of the column conductor 2 and the channel 1 row conductor of the tens matrix M1 is effective to set the core at the intersection thereof to a predetermined magnetic state. After printing out the digit 2, the carriage is stepped one position to the commutator contact 3 when a further 100 microsecond pulse is routed via channel 1 row conductor of the units matrix M2 con-

tact 0 of the second plot digit switch SW-2 and the column conductor 0 of the tens and units matrices M1 and M2 to energize solenoid 51 to print out the digit 0. Thus coincident energization of the column conductor 0 and the channel 1 row conductor of the units matrix M2 is effective to set the core at the intersection thereof to a predetermined magnetic state. The cores set to a predetermined magnetic state in column 2 on channel 1 row of the tens matrix M1 and in column 0 on channel 1 row of the units matrix M2 indicates a stored value of 20 for channel 1. The carriage is then stepped to the commutator contact 4 position at which the decimal point is printed as hereinbefore described. After printing of the decimal point, the carriage steps to commutator contact 5 at which a further 100 microsecond pulse is routed via the 6 contact of the first non-plot digit switch SW-3 and the 6 column conductor of the tens and units matrices M1 and M2 to energize the solenoid drive 57 effecting print-out of the digit 6. The carriage is then stepped to commutator contact 6 at which a further 100 microsecond pulse is routed via the 3 contact of the second non-plot digit switch SW-4 and the 3 column conductor of the tens and units matrices M1 and M2 to energize the solenoid 54 and effect print-out of the digit 3. Since the channel 1 row conductors of the tens and units matrices are connected only to the first and second plot digit switches SW-1 and SW-2, the value set up on the two non-plot digit switches SW-3 and SW-4 will not be stored in either matrix, as the currents passed through the column conductors, when the first and second non-plot digits are printed, will not be effective to change the state of any of the cores in these columns.

The two most significant digits of each of the values set up in the other seven input channel switches are stored in the magnetic memory in the same manner as described above. The movable contacts of the first and second plot digit switches of channel 2 are connected to a channel 2 row conductor of the tens matrix and a channel 2 row conductor of the units matrix respectively, and the first and second plot digit switches of subsequent channels are connected to the corresponding channel row conductors of the tens and units matrices M1 and M2.

In the foregoing description of the tabulation of the values derived from each of the 8 channels, the two most significant digits of each value were stored in the matrices M1 and M2. It will be understood that any other two digits of a value can be stored by appropriate wiring of the 4 bank 10 position switches SW-1 to SW-4 of each channel. This facility can be used for scale expansion, for example, if a range of temperatures varied between 101.3° C. and 102.3° C. then to obtain a useful graph only the last two digits of each value would be stored. Taking the value 101.6, the digit 1 would be stored in the tens matrix and the digit 6 in the units matrix; in this instance, the fourth commutator contact of the 5 contacts assigned to the value 101.6 would be wired to the decimal point bus bar so that on tabulating the decimal point would be printed in the correct position.

The number of commutator contacts assigned to each channel is 7, comprising four contacts for each of the four digital values, one contact for the decimal point and 2 contacts for spacing. Thus the total number of commutator contact positions is 56 plus 7 contacts for the value set up on the digital clock, making a total of 63 contacts. The plotting phase commences at the 64th commutator contact and continues to the 164th commutator contact, but for convenience these contact positions will be referred to in the following description by their positions relative to the graphical answer produced by plotting the digital values of each channel. Therefore contacts 64 and 164 will be referred to as contacts 00' and 100' respectively.

Thus at the end of the tabulating phase all the most significant digits of each of the values derived from the eight channels are stored in the tens and units matrices

M1 and M2, and the carriage is stepped on two spaces to the commutator position at which plotting of the stored values commences.

Plotting phase

All the 8 points representing the stored values (i.e. the two most significant digits) derived from the 8 channels are plotted during one traverse of the carriage across one line of that part of the record medium known as the plotting field. The eight points so plotted are those values derived from the 8 channels at the time indicated by the digital clock, whose output is first printed on the record medium before each of the 8 values are tabulated. Since only 8 points are to be plotted over 100 printing positions of the typewriter carriage, it is desirable to minimize the movement time of the carriage as much as possible. This is achieved by setting the tab stops of the typewriter at every 10th position of the carriage from the 00' position and arranging energization of the tabulate key solenoid when there are no points to be plotted in the next decade; this facility will be described in more detail in the following description.

The 8 points are plotted in ascending order of magnitude, which is determined by suitable interrogation of the tens and units matrix core stores M1 and M2, the interrogation being synchronized with the movement of and controlled by the carriage.

So that the matrices M1 and M2 can be interrogated, additional row and column conductors which are used only during the plotting phase are provided in both matrices. In the tens matrix M1 each column of cores is threaded by two wires connected in series. These wires, which are additional to those used during the tabulating phase, are so arranged with respect to the cores in a column that only a half current select pulse is sufficient to produce a magnetic field to switch the core from one magnetic state to another. In FIG. 3A the two wires of each column are shown as one wire and are numbered 100 to 109. Each pair of these interrogate column wires 100 to 109 are connected to the respective commutator contacts 00', 10', 20' . . . 100'. Coincident current selection of the cores in the tens matrix M1 is not used. Instead, the matrix is interrogated by a half current applied to the two serially connected column conductors. Resetting of any core in a column will produce an output pulse on one of the row conductors 111 to 118 of the matrix M1 which are additional to those employed during the tabulating phase. The units matrix M2 is interrogated by the half current coincident selection principle. In the matrix M2 for each row of cores there is a further pair of interrogate row conductors R1 to R8 and R9 to R16, and an additional ten column conductors C0 to C9. Each column conductor is connected to the appropriate one of the commutator contacts 01' to 09', which are wired in parallel with the commutator contacts, 11' to 19', 21' to 29' etc. The interrogate row conductors R9 to R16 (FIG. 3B), are connected to single shot serially connected circuits SS41 to SS48, and the row conductors R1 to R8 are connected to matrix single shot circuits SS69 to SS76.

Coincident application of half current pulses to a particular column and to one of the rows R9 to R16 of matrix M2 will cause a core at the intersection thereof that has been set during the tabulating phase to be reset, and an output pulse on one of the rows R1 to R8 will cause the associated matrix single shot circuit to fire. The output from this single shot circuit is utilized to energize one of the solenoids 61 to 68 to print out a symbol representative of the source from which the plotted value has been derived.

Each of the single shot circuits SS48 to SS41 is adapted to apply a 300 microsecond pulse to one of the two inputs of AND gates &78 to &85. Outputs from each of these AND gates are applied to OR gate OR33, the output from which is applied to a 100 microsecond delay unit 34 which

is connected to a 10 microsecond pulse generator PG35.

The row conductors 111 to 118 of the tens matrix M1 are connected to a set of matrix latches L12 to L19. Each of the aforementioned latches L12 to L19 comprises a bistable circuit having two output terminals and two input terminals, one of which input terminals is connected to a reset circuit 37 and the other to one of the tens matrix row conductors 111 to 118. The bistable circuit is adapted to provide static voltage outputs of two different magnitudes at the output terminals depending on the state in which the latch has been set either by an input signal from one of the row conductors 111 to 118 or by the reset circuit 37. One output from each of the latches L12 to L19 is applied to the other input of the corresponding AND gates &78 to &85, and each of the other outputs from the matrix latches L12 to L19 are applied to an OR circuit OR24, the output of which is connected to terminal L32-3 of a latch-tab/scan circuit L32. A set of matrix single shot circuits SS69 to SS76 are connected to the row conductors R1 to R8 of the units matrix M2. The circuits SS69 to SS76 are monostable circuits adapted to provide a pulse output on each of their output terminals on receipt of an input pulse. A bias circuit 77 is provided to inhibit firing of any further one of the single shot circuits SS69 to SS76 after one of the circuits has been fired by a core resetting in any one of the rows of the units matrix. This condition can only occur when two identical values from different channels have been stored during the tabulating phase. The bias circuit 77 is provided to prevent energization of two different symbol keys in the same printing position of the typewriter carriage and to prevent any of the solenoids 61 to 68 being energized by random pulses when the carriage returns from the 100' commutator contact, as will become apparent in the ensuing description. One output from each of the circuits SS69 to SS76 is connected to symbol solenoid drives 61 to 68, and the other output from each of the circuits SS69 to SS76 is applied to an OR gate OR36, the output of which is connected to terminal L11-3 of a latch print-inhibit circuit L11. An output L11-1 from L11 is connected to one input of a two-input AND gate &25, the other input of this AND gate being connected to a 300 microsecond single shot circuit SS40, SS40 being serially connected to the 300 microsecond single shot circuit SS41. An output from the AND gate &25 is connected to the space solenoid drive 50.

The half current pulses required to interrogate the units matrix M2 are supplied by the 10 microsecond pulse generator PG35 in conjunction with the current driver CD5. As shown in FIG. 3B, the current driver CD5 is connected to one of the column conductors C0 to C9 of the units matrix M2 via the commutator contact at which the carriage has stopped. Thus it will be seen that a row of cores in the units matrix is connected between the 10 microsecond pulse generator PG35 and the current driver CD5. A pulse applied to generator PG35 switches it on, earthing the current driver CD5 via one of the column conductors C0 to C9. Earthing of driver CD5 causes it to conduct for 10 microseconds, the period provided by the generator PG35. This generator PG35 is switched by a 1 ms. single shot circuit SS27 via OR gate OR33 and the 100 microsecond delay circuit 34; SS27 is in turn fired by a 15 ms. single shot circuit SS26. A pulse supplied by the -12 v. source connected to resistor RS10 via a commutator contact position on which the typewriter carriage has stopped is effective to fire the 30 ms. single shot circuit SS23 and thus initiate the other single shot circuits SS26 and SS27. The 30 ms. single shot circuit SS23 is fired at each of the tens commutator contact positions by the negative pulse from the -12 v. source being routed via one of the column conductors 100' to 109' and OR gate OR87. Firing of SS23 when the carriage is at one of the units commutator contacts 00' to 09', 11' to 19', etc., is effected by the negative pulse being applied via the one of the column conductors

C0 to C9 of the units matrix M2, AND gate &86 and the OR gate OR87. A further 1 ms. single shot circuit SS28 is connected to circuit SS27, the output of SS28 being connected to one input of a two-input AND gate &30 and one input of a two-input AND gate &29. The output of the AND gate &30 is connected to a tabulate solenoid drive 49. The output of the other AND gate &29 is connected to SS48, the first of the series of serially connected 300 microsecond single shot circuits SS48 to SS41. The other input of the AND gate &30 is connected to terminal L32-1 of the latch L32, and the other input of the two-input AND gate &29 is connected to terminal L32-2 of latch L32 and to one input of the two-input AND gate &86. The common connection of the column conductors 100 to 109 of the tens matrix M1 is connected to one input of the two-input OR gate OR87 and to one input of a two-input OR gate OR8. The output from OR gate OR8 is connected to one input of a two-input AND gate &10. The output of AND gate &10 is connected to the reset circuit 37. The output from the 15 ms. single shot circuit SS26 is connected to one input of an OR gate OR9 whose output is connected to the other input of the two-input AND gate &10. The other input of the OR gates OR8 and OR9 are connected to terminal L7-2 of a print/plot latch L7 which is also connected to terminal L11-5 of the latch L11. Terminal L7-3 of latch L7 is connected to a terminal L31-3 of CR latch L31 and to the commutator contact 100' and the terminal L7-4 of latch L7 is connected to contact 63' of the commutator which is the last contact of the commutator used in the tabulating phase. The terminal L7-1 of latch L7 is connected to one input of a two-input OR gate OR4, whose other input is connected to the 100 microsecond single shot circuit SS3 shown in FIG. 2. The output of the OR gate OR4 is connected to one input of a two-input AND gate 6 via an inverting circuit 88 and to the current driver CD5, whose output is connected to the common commutator contact. The terminal L31-2 of CR latch L31 is connected to a carriage return solenoid drive CR21, and to the other input of the two-input AND gate &6. The output of AND gate &6 is connected to a transistor switch S20 which serves to hold the commutator common contact at earth potential when energized by an output signal from AND gate &6.

Each of the aforementioned latches L7, L11, L31 and L32 comprises a bistable circuit having two input terminals 3 and 4 (with appropriate prefixes) and two output terminals 1 and 2; the latch L11 includes a further input terminal L11-5. Assuming that the bistable circuit of the latch is in an initial state in which the output terminal 2 has a static voltage level higher than that of output terminal 1, then a pulse applied to input terminal 4 is effective to change the state of the latch to provide a higher static voltage at terminal 1 than terminal 2. Conversely, a pulse applied to input terminal 3 is effective to change the state of the bistable circuit back to its initial stable state. The input terminal L11-5 of latch L11 is provided to allow switching of the bistable circuit of the latch to the state in which a static voltage output appears on output terminal 2 higher than that on output terminal 1.

So that a clear understanding of the operation of the preferred embodiment of the invention may be obtained, the following description is related to the plotting of the values tabulated at time 1200 hours as shown in FIG. 1. As stated in the description of the printing phase, only the two most significant digits of the tabulated values are stored for subsequent plotting and these values are as follows:

Channel.....	1	2	3	4	5	6	7	8
Value.....	20	34	63	70	81	51	09	93
Channel Symbol.....	+	.	:	"	@	,	*	°

When the carriage is moved by the last stepping operation performed during the printing phase to a position at which the commutator contact 00' makes with the common contact, a negative signal is applied to the 30 ms. single shot circuit SS23 via the column conductor 100' of the matrix M1 and OR gate OR87, AND gate &86 being deconditioned as will be explained hereinafter. The magnitude of the negative signal applied to the column conductor 100' of the tens matrix M1 is insufficient to reset any cores in that column that were set during the tabulating phase. The leading edge of the output pulse from the single shot circuit SS23, resulting from the application of the negative signal, fires the 15 ms. single shot circuit SS26, thus the output pulses produced by the circuits SS26 and SS23 commence at the same instant of time. The trailing edge of the 15 ms. output pulse from circuit SS26 fires 1 ms. single shot circuit SS27 and the trailing edge of the output pulse from circuit SS27 fires the 1 ms. single shot circuit SS28. The output pulse from circuit SS27 causes the ten microsecond pulse generator PG35 to switch on current driver CD5, this output pulse being applied to generator PG35 via OR circuit OR33 and the 100 microsecond single shot delay circuit 34. The pulse produced by driver CD5 has a fast rise time and an amplitude equal to half the current required to switch any core of the matrix M2 from one magnetic state to another. As hereinbefore described, the column conductors 100', 101', etc., of the tens matrix comprise two wires for the plotting phase so that the half current interrogate pulse from CD5 switches the core at the intersection of column 100 and row 117 of the tens matrix M1. Referring to the table of significant digits above, it will be seen that the switching of this core corresponds to the first significant digit 0 of the value 09 from channel 7. The switching of this core sets the matrix latch L18 connected to row 117 of the tens matrix M1, to condition AND gate &84. The other output of latch L18 is applied to the OR gate OR24 whose output is connected to terminal L32-3 of tab/scan latch L32. The latch L32 has previously been set in its "tab" state by application to terminal L32-4 of the output pulse from circuit SS26, which is effective to produce a voltage on terminal L32-1 higher than that on terminal L32-2 to condition one input of AND gate &29 and decondition AND gate &86. Thus the latch L32 will switch to its "scan" state on application of the pulse from OR24 to terminal L32-3 producing a higher voltage output on terminal L32-2 than terminal L32-1. This is effective to condition AND gate &86, AND gate &29 and decondition AND gate &30.

Interrogation of the tens matrix M1 by a pulse from driver CD5 is now followed by interrogation of the units matrix M2.

The output from the circuit SS28 is applied to the other input of the AND gate &29, which having both of its inputs energized applied an output pulse to the first of the serially connected 300 microsecond single shot circuits SS40 to SS48, the first circuit referred to being SS48. The circuits SS41 to SS48 apply a 300 microsecond pulse to each of the 8 rows R9 to R16 of the units matrix M2 sequentially and also to one input of the two input AND gates &78 to &85. Since the circuit SS28 fires 1 ms. after circuit SS27, the 300 microsecond single shot circuits are fired after the conditioning of AND gate &84. Thus, when the circuit SS42 is fired by the trailing edge of the output pulse from circuit SS43, 1500 microseconds after the firing of circuit SS48 AND gate &84 supplies an output pulse to the OR circuit OR33 which is effective to fire again the 10 microsecond pulse generator PG35 to produce a pulse from driver CD5. The output pulse from driver CD5 is applied to the column conductor C0 of the units matrix M2 and the column conductor 100 of the tens matrix via commutator contact position 00' and resistor RS101 to -12v. Since there is a delay of 100 microseconds in firing PG35, then the half current

10 microsecond interrogate pulse occurs on the column conductor C0 of the units matrix M2 100 microseconds after the firing of circuit SS42. Thus, there is a coincidence of half current select pulses on the 0 column conductor C0 and the R15 conductor of the units matrix M2. However, since the core at the intersection thereof was not set during the tabulating phase, then no output pulse appears on the conductor R7.

The 300 microsecond pulses provided by the circuits SS48 to SS41 have a slow rise time. This is necessary to prevent an output pulse appearing on row conductors R1 to R8 whenever a 300 microsecond pulse is applied to the row conductors R9 to R16, as both sets of row conductors are run through the cores in parallel relationship. The 100 microsecond circuit 34 is provided to ensure that the steep-sided pulse produced by the 10 microsecond pulse generator PG35 occurs at a time when the 300 microsecond pulse applied to any of the row conductors R9 to R16 has achieved its maximum amplitude.

At the same time that the latch circuit L32 was set to its "tab" state, the latch L11 was set to a print state by application of the output pulse from circuit SS26 to terminal L11-4 of the latch L11 which produced a voltage output on its terminal L11-1 higher than that on its output terminal L11-2. The voltage on terminal L11-2 is effective to condition one input of an AND gate &25, the other input of AND gate &25 being connected to the output of the last of the 300 microsecond single shot circuits SS40.

After coincident pulses have been applied to the C0 column conductor and the R15 row conductor of matrix M2, the next 300 microsecond single shot circuit SS41 is fired by the trailing edge of circuit SS42 sending a 300 microsecond pulse along the row conductor R16. The 300 microsecond pulse produced by circuit SS41 is also applied to one input of the two-input AND gate &85. However, the other input of the AND gate &85 is not conditioned and therefore a 10 microsecond pulse from current driver CD5 is not produced. The trailing edge of the 300 microsecond pulse from circuit SS41 fires the next sequential circuit SS40. The two inputs of the AND circuit &25 are now conditioned and an output signal therefrom energizes a space solenoid drive circuit 50 to step the carriage on to the next commutator contact 01'.

The carriage arriving at commutator contact 01' causes a negative signal to be applied to the 30 ms. single short circuit SS23 via diode D38, the conditioned AND gate &86 and OR gate OR87 thus re-initiating a sequence of events as described above with reference to the interrogation of matrix M2 when the carriage is at contact 00'. It will be remembered that the switching of the core at the intersection of the column conductor 100 and the row conductor 117 of matrix M1 has set the latch L18 to condition one input of the AND gate &84. The circuits SS48 to SS41 are again fired by an input pulse to circuit SS48 from the AND gate &29 as described above, and 300 microsecond pulses are sequentially applied to the row conductors R9 to R16 of the matrix M2. The column conductor C1 of the matrix M2 is energized by a 10 microsecond pulse from current driver CD5 and generator PG35, 100 microseconds after the application of the 300 microsecond pulse from circuit SS42 to row R15. Again, since no core has been set at the intersection of the column conductor C1 and the row conductor R15, no output pulse is sensed on the row conductor R7 and the space solenoid drive 50 is again energized as hereinbefore described, stepping the carriage on to commutator contact 02'.

Referring now to the table of significant digits, it will be seen that the only core that has been set on row R15 of matrix M2 during the printing phase is the core at the intersection of the column conductor C9 and that row conductor. Consequently, the carriage steps on to commutator contact 09' without any of the solenoid drives 61 to 68 being energized.

On arrival at the commutator contact 09', a negative signal is applied to circuit SS23 to initiate the single shot circuits SS26, SS27 and SS28 as described with reference to the arrival of the carriage at commutator contact 01'. The single shot circuits SS48 to SS41 will be fired sequentially by a pulse from the output of the AND gate &29. When the circuit SS42 is fired by the output pulse from circuit SS43, a 300 microsecond pulse is applied to row conductor R15 and to one input of the conditioned AND gate &84. An output pulse from AND gate &84 through OR circuit OR33 fires the 10 microsecond pulse generator PG35 to induce a pulse from driver CD5 on the C9 column conductor of M2. Thus, there will be a coincidence of pulses on conductors R15 and C9 switching the core at the intersection thereof which has been set during the printing phase. The switching of this core produces an output pulse on R7 to set the matrix single shot circuit SS75. An output from circuit SS75 energizes the solenoid drive 67 to print out a symbol *, representing channel 7. A further output from the circuit SS75 is applied to the OR gate OR36, an output from which is applied to terminal L11-3 of the print/inhibit latch L11 which changes its state to produce a voltage output on terminal L11-2 higher than that on terminal L11-1. This is effective to energize the bias circuit 77 which inhibits all inputs to the single shot circuits SS69 to SS76, preventing any further pulses which might occur on the row conductors R1 to R8 firing any of the circuits SS69 to SS76. The plotting of the symbol * causes the carriage to step on to the 10' commutator contact by the normal mechanical escapement mechanism of the typewriter.

On arrival at the 10' commutator contact, a negative signal is applied via the column conductor 101' of the tens matrix M1 to one input of the OR gate OR8 and via OR gate OR87 to the 30 ms. single shot circuit SS23. The firing of the 15 ms. single shot circuit SS26 by an output pulse from circuit SS23 produces a pulse on one input of OR gate OR9. As both OR gates OR8 and OR9 have one of their inputs energized, an output pulse from both these OR gates is applied to both inputs of the AND gate &10. An output from the AND gate &10 is applied to the reset circuit 37 to reset all the matrix latch circuits L12 to L19. However, since only latch L18 was set during the interrogation of the tens matrix M1 at the 00' to 09' contact positions, only that latch will be reset thus deconditioning AND gate &84. It will be appreciated that if more than one core in a particular column of the tens matrix is set during the tabulating phase, then on interrogation more than one of the matrix latches L12 to L19 would be set to condition the appropriate AND gates &78 to &85, and on energizing the reset circuit 37 all those latches would be reset.

A pulse applied from circuit SS27 fires the 10 microsecond pulse generator PG35 which causes driver CD5 to produce an output pulse which is routed via the C0 column conductor of the units matrix M2 and the 101 column conductor of the tens matrix M1. Referring again to the table of significant digits, it will be seen that no core has been set in the 101 column of the tens matrix M1 since this column represents the tens digits of any of the values printed during the tabulating phase. In consequence, no output pulse will be produced on any of the row conductors 111 to 118 by a core changing its magnetic state and thus, none of the latches L12 to L19 are set to condition any of the AND gates &78 to &85. On firing of SS26 an output pulse is applied to terminal L32-4 of latch L32 which is effective to cause the output voltage on terminal L32-1 to be higher than that on terminal L32-2, deconditioning the AND gate &29 to prevent the circuits SS48 to SS41 from being fired; thus no interrogation of the units matrix M2 is effected. The higher voltage produced on terminal L32-1 conditions one input of the AND gate &30, the other input thereof being energized by the output pulse from circuit SS28.

Both inputs of AND gate &30 being energized, an output pulse therefrom energizes the tabulate solenoid drive 49 to step the carriage on 10 positions to the next commutator contact 20'.

When the carriage arrives at commutator contact 20', a negative signal is again applied via the column conductor 102 of the tens matrix M1 and OR gate OR87 to fire the circuits SS23, SS26, SS27 and SS28. The firing of circuit SS27 fires the 10 microsecond pulse generator PG35 and SS26, applies a pulse to terminal L32-4 of latch L32 and sets the latch in its "tab" state. However, the latch L32 is already in its tabulate state from the previous operation. The 10 microsecond pulse from driver CD5 is applied to the C0 column conductor of M2 and the 102 column conductor of M1. Since a core at the intersection of row 111 and column 102 has been set during the tabulating phase, the applied 10 microsecond pulse is effective to switch this core and produce an output pulse on row 111 to set the latch L12. The setting of the latch L12 conditions one input of the AND gate &78.

Interrogation of the units matrix M2 now proceeds in the same manner as described with reference to the 00' commutator contact position of the carriage.

Briefly, the interrogation of M2 is as follows: The circuit SS28 fires 1 ms. after SS27 to initiate firing of the 300 microsecond single shot circuits SS48 to SS40 through the conditioned AND gate &29. Firing of SS48 conditions the other input of AND gate &78 and applies a 300 microsecond pulse to row conductor R9. Since AND gate &78 has now both its inputs conditioned, an output therefrom, through OR gate OR33, fires the generator PG35 which causes driver CD5 to apply a 10 microsecond pulse to column conductor C0 of M2.

As the 10 microsecond pulse applied to the C0 column conductor of M2 is coincident with the 300 microsecond pulse applied to row conductor R9, the core at the intersection thereof, representing the digit 0 of the value 20 of channel 1, is switched. The switching of this core in the units matrix M2 produces an output pulse on row conductor R1 to fire the matrix single shot circuit SS69, an output from which energizes the solenoid drive 61. An output from circuit SS69 produces an output from OR gate OR36 to switch latch L11 to its inhibit state in which the higher voltage output from terminal L11-2 causes the circuit 77 to inhibit any further inputs to the matrix single shot circuits SS69 to SS76. The energizing of 61 causes a symbol "+" representing channel 1 to be printed out. The plotting of this symbol steps the carriage to commutator contact 21' by the normal mechanical escapement mechanism of the typewriter.

It should be noted here that while the bias circuit 77 inhibits further firing of any of the single shot circuits SS69 to SS76, due to, say, two identical values derived from different channels being stored during the tabulating phase, the interrogation of the matrix by sequential firing of circuits SS48 to SS41 will still proceed. For example, should a core have been set at the intersection of column C0 and row R8, R16, then that core will be reset on firing of circuit SS41, but the output pulse developed on R8 will be ineffective to fire the single shot circuit SS76. The incorporation of the bias circuit 77 ensures that all cores that have been set during the tabulating phase are reset during the plotting phase, thus obviating the need for separate erase circuitry.

On arrival at commutator contact 21' the units matrix M2 is again interrogated, but since no other core has been set on row R9 of M2 the carriage will step on contact position by contact position to commutator contact 30'. It will be appreciated that during the time that the carriage is stepped from commutator contact 20' to contact 30', the AND circuit &78 remains conditioned.

The reset circuit 37 is energized on the carriage arriving at commutator contact position 30' to reset the matrix latch L12 and decondition AND gate &78. The negative signal produced when the carriage arrives at contact 30'

fires the circuits SS23, SS26, SS27 and SS28 to switch on generator PG35 causing driver CD5 to supply a 10 microsecond pulse to interrogate first the tens matrix M1 and then by subsequent firing of circuits SS23, SS26, SS27, SS28, PG35 and CD5 to interrogate the units matrix M2 in the manner described with reference to the arrival of the carriage at the 20' commutator contact position.

Referring now to the table of values stored during the tabulating phase, it will be seen that a core has been set at the intersection of column 103 and row 112 of the tens matrix M1 and at the intersection of column C4 and rows R2 and R10 of units matrix M2. This represents the tens and units digits respectively of the value 34 received from channel 2. Thus the carriage will be stepped from commutator contact 30' to contact 34' at which position the core at the intersection of column C4 and rows R2 and R10 will be reset to its original magnetic state energizing solenoid 62 to print out the symbol "." representing channel 2 at a position 34 print positions away from contact 00'. After plotting of the symbol "." the carriage steps on to commutator contact 40'.

At commutator contact 40' the negative signal is applied to the column conductor 104, but since no core in this column has been set during the tabulating phase, none of the latches L12 to L19 will be set. The latch L32 which was set to its "scan" state on the carriage arriving at commutator contact 30' resets to its "tab" state when the negative signal produced at commutator contact 40' fires circuits SS23 and SS26. The latch L32, on being set in its "tab" state, produces a voltage at its output terminal L32-1 higher than that at its output terminal L32-2 to condition the AND gate &30. Thus, when the 1 ms. single shot circuit SS28 fires an output from AND gate &20 energizes the tabulate solenoid drive 49 to cause the carriage to step on 10 positions to commutator contact 50'.

At commutator contact 50', the tens matrix will again first be interrogated followed by interrogation of the units matrix as hereinbefore described. It will be seen from the table of values stored during the tabulating phase that the next value to be read out of the tens and units matrices will be 51, that is, the value received from channel 6 during the tabulating phase. The symbol "." representing channel 6 will be plotted 51 print positions away from contact 00' when the units matrix M2 is interrogated and the core at the intersection of column C1 and rows R6 and R14 has been reset, this core representing the units digit of the value 51.

Thus it will be seen that the stored values are read out in ascending order and the next symbol to be plotted after interrogation of the matrices M1 and M2 represents the value 63, the value received from channel 3 during the tabulating phase. The subsequent values 76, 81 and 93 received from channels 4, 5 and 8 respectively will subsequently be plotted in the same manner.

After the symbol "o" representing channel 8 has been plotted at commutator contact 93, the carriage steps on to commutator contact 94' by the normal mechanical escapement mechanism of the typewriter. When the carriage arrives at commutator contact 94' the C4 column conductor of the units matrix M2 is interrogated, but since no core has been set at the intersection of that column and the rows R8 and R16, the single shot SS76 will not be fired and there will be no input to the OR gate OR36. Thus, the latch L11 will be set by firing of SS26 so that a voltage output from terminal L11-1 higher than that of terminal L11-2 conditions AND gate &25. The other input of AND gate &25 receives a pulse from the last 300 microsecond single shot circuit SS40 which energizes the space solenoid drive 50 stepping the carriage on to commutator contact 95'. As no other core has been set on row 8 and R16 of units matrix M2, the carriage will step on as described above to the last commutator contact position 100'.

When the carriage arrives at commutator contact 100', a negative signal is applied to reset the latch L7 and

the CR latch L31. The latch L31 on being reset produces a voltage output at its terminal L31-2 higher than that at terminal L31-1, thus energizing the carriage return solenoid drive CR21. The energization of CR21 returns the carriage to the commutator contact position 1 as shown in FIG. 2. The output from terminal L31-2 of latch L31 also conditions AND gate &6. The latch L7 on being reset produces a voltage at its terminal L7-2 higher than that its terminal L7-1, deconditioning OR gate OR4 and conditioning AND gate &6 through the inverter circuit 88. The circuit 88 serves to invert the voltage applied from OR circuit OR4 so that an output from OR gate OR4 deconditions AND gate &6 and no output from OR gate OR4 conditions AND gate &6.

As there is now a coincidence of inputs on AND gate &6, an output therefrom switches on transistor circuit S20 which holds the commutator common contact at earth potential. This is effective to prevent any random pulses from being developed when the carriage returns to the first commutator position.

During return of the carriage and during the tabulating phase, setting of any of the latches L12 to L19 and firing of the matrix single shot circuits SS69 to SS76 by any random pulses are prevented by applying the output voltage from terminal L7-2 of latch L7 to the terminal L11-5 of latch L11 causing the bias circuit 77 to inhibit the inputs of circuits SS69 to SS76 and to the OR gates OR9 and OR8 causing AND gate &10 to energize reset circuit 37 houlding the circuits L12 to L19 in their reset state.

The return of the carriage causes the print-receiving medium to be moved up to a position at which the next series of values from 8 channels can be printed and plotted at time 12.01 hours. The carriage on arriving at the first commutator position deconditions AND gate &6 and switching off the transistor circuit S20.

With the exception of the OR gate OR33, the various AND and OR gates shown in FIGS. 2 and 3 may be of any type that are well known to those skilled in the art, and in consequence detailed circuit descriptions of these are deemed unnecessary. To reduce the size of the electronic circuits we prefer to use transistors in the latch and single short circuits, and in the current driver circuit CD5, but it will be appreciated that ordinary vacuum tubes may equally well be used.

The OR gate OR33 has a differentiating circuit on each of its inputs. This is necessary to separate any two consecutively applied 300 microsecond pulses from the circuits SS48 to SS41, since the trailing edge of a 300 microsecond pulse from one of the single shot circuits SS48 to SS41 is coincident with the rise of the 300 microsecond pulse from the next circuit in the series. A condition which would give rise to such a situation would be when, say, values of 25 and 28 from channels 3 and 4 respectively had been stored during the tabulating phase. Thus, when plotting these values, latches L14 and L15 of the tens matrix would be set conditioning AND gates &80 and &81 at the carriage position contact 20'. On stepping to each subsequent contact 21', 22', . . . 29', the single shot circuits SS48 to SS41 would be sequentially fired and two consecutive pulses applied to the inputs of OR gate OR33 connected to AND gates &80 and &81. Apart from the incorporation of a differentiating circuit in each input of OR gate OR33, the gate may be of any type well known in the art.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

What is claimed is:

1. Apparatus operable under the control of digital signals representative of the values of a plurality of separate input variables for printing on a record medium the respective digital values of the input variables in assigned

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columns thereof as well as a distinctive graphical symbol for each said variable at a position on said record medium determinative of the value of the variable, comprising a first storage device storing the respective digital values of said variables; a typewriter type of printing device having a moving carriage, electrically operated numeral and symbol printing instrumentalities, and function controls including carriage space and tabulate devices; an emitter on said typewriter for emitting signals which manifest the displacement of the typewriter carriage; means under control of said first storage device and said emitter for controlling the sequential operation of said numeral printing instrumentalities and said function controls to print the respective digital values of said input variables in predetermined columns on said record medium; a second storage device; means under control of said first storage device and said emitter for entering the digital values stored in said first storage device in said second storage device; and means under control of said emitter and said second storage device for reading out the data stored in said second storage device in ascending order of magnitude and controlling the carriage tabulating and spacing controls as well as the symbol printing instrumentalities to print the graphical symbols representative of the respective variables at positions on said record medium manifestive of the values thereof.

2. Apparatus for controlling the operation of a typewriter type of printing device to print a distinctive symbol for each one of N input variables in displaced positions on a record medium determinative of the respective values of the variables, the said printing device including a movable carriage, signal-operated carriage tabulating and spacing controls, and signal operated symbol printing instrumentalities, comprising an emitter having a plurality of fixed contacts, one for each successive carriage position, and a movable contactor connected to said carriage and operable to produce successive signals on said fixed contacts to measure the position of the carriage; a first and a second storage matrix each having ten columns and N rows of bistable storage elements selectively set in one of their stable states to manifest the respective first and second decimal digital values of each of said N input variables; interrogating means controlled by the signals appearing on each tenth one of said fixed contacts for interrogating the stability states of the storage ele-

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ments of said first matrix in the respective columns whose ordinal positions correspond with the ordinal positions of the every tenth contacts; means responsive to said interrogating means for registering the respective rows in which the storage elements manifest the storage of a digit; means initiated by the registering of a digit storage in said first matrix for interrogating the stability states of the elements in said second matrix in rows corresponding to the rows of said first matrix registering a digital storage, and in columns controlled by signals appearing on the respective correspondingly ordered fixed contacts intervening said every tenth contact; means responsive to the means for interrogating the stability states of the elements in said second matrix for operating corresponding ones of said symbol printing instrumentalities when an interrogated element in said second matrix manifests a digit, storage; means responsive to the operation of said means for interrogating the stability states of the elements of said second matrix for operating said spacing control to space said carriage upon the completion of each such interrogation; and means responsive to the means for registering the respective rows of said first matrix in which the elements manifest the storage of a digit for operating the carriage tabulate control to tabulate the said carriage ten spaces upon the absence of a digital storage in a column of said first matrix.

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