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(54) **Title**: COOLING OF COPLANAR ACTIVE CIRCUITS

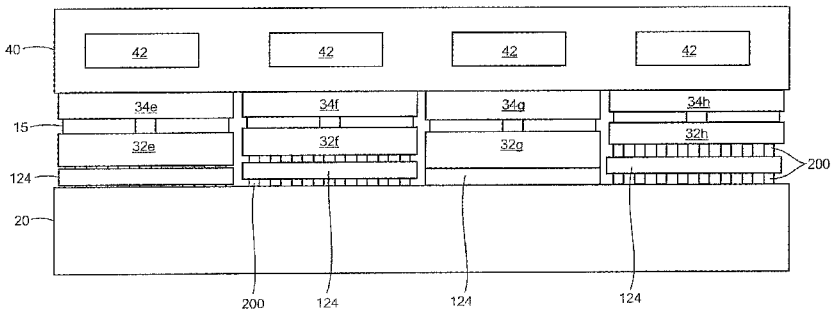

FIG. 3

(57) **Abstract**: In one aspect, a system includes a first circuit board that includes integrated circuits, a first thermal spreader coupled to the integrated circuits of the first circuit board, a first compliant board coupled to the first circuit board, a second circuit board that includes integrated circuits and a second thermal spreader coupled to the integrated circuits of the second circuit board. The first circuit board and the first thermal spreader have a first thickness. The second daughter board and the second thermal spreader have a second thickness. The system includes a second compliant board coupled to the second circuit board, a board assembly coupled to first and second compliant boards and a cold-plate assembly in contact with the first and second thermal spreaders. Either of the first or the second compliant boards is configured to expand or contract to account for the differences between the first and second thicknesses.

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COOLING OF COPLANAR ACTIVE CIRCUITS

BACKGROUND

As is known in the art, a phased array antenna includes a plurality of active circuits spaced apart from each other by known distances. Each of the active circuits is coupled through a plurality of phase shifter circuits, amplifier circuits and/or other circuits to either or both of a transmitter and receiver. In some cases, the phase shifter, amplifier circuits and other circuits (e.g., mixer circuits) are provided in a so-called transmit/receive (T/R) module and are considered to be part of the transmitter and/or receiver.

The phase shifters, amplifier and other circuits (e.g., T/R modules) often require an external power supply (e.g., a DC power supply) to operate correctly. Thus, the circuits are referred to as "active circuits" or "active components." Accordingly, phased array antennas which include active circuits are often referred to as "active phased arrays."

Active circuits dissipate power in the form of heat. High amounts of heat can cause active circuits to be inoperable. Thus, active phased arrays must be cooled. In one example heat-sink(s) are attached to each active circuit to dissipate the heat.

SUMMARY

In one example, an active, electronically scanned array (AESA) panel architecture system includes a first daughter board that include active circuits, a first thermal spreader coupled to the active circuits of the first daughter board, a first compliant board coupled to the first daughter board, a second daughter board that includes active circuits, a second thermal spreader coupled to the active circuits of the second daughter board, a second compliant board coupled to the second daughter board, a mother board assembly coupled to first and second compliant boards and a cold-plate assembly in contact with the first thermal

spreader and the second thermal spreader. The first daughter board and the first thermal spreader have a first thickness and the second daughter board and the second thermal spreader have a second thickness different from the first thickness. Either of the first or second compliant boards is configured to expand or contract to account for the differences between the first and second thicknesses.

In another aspect, an active, electronically scanned array (AESA) panel architecture system includes a first daughter board that includes active circuits, a first thermal spreader coupled to the active circuits of the first daughter board, a first RF interface board coupled to the first daughter board, a second daughter board that includes active circuits, a second thermal spreader coupled to the active circuits of the second daughter board, a second RF interface board coupled to the second daughter board, a mother board assembly coupled to first and second RF interface boards, and a cold-plate assembly in contact with the first and second thermal spreaders. The first daughter board and the first thermal spreader have a first thickness and the second daughter board and the second thermal spreader have a second thickness different from the first thickness. The first and second RF interface boards each include compliant elements on at least one side of the first RF interface board. The first and second RF interface boards are configured to expand or contract to account for the differences in thicknesses between the first thickness and the second thickness. The first RF interface board provides electrical coupling between the active circuits of the first daughter board and the mother board and the second RF interface board provides electrical coupling between the active circuits of the second daughter board and the mother board.

In a further aspect, a system includes a first circuit board that includes integrated circuits, a first thermal spreader coupled to the integrated circuits of the first circuit board, a first compliant board coupled to the first circuit board, a second circuit board that includes

integrated circuits and a second thermal spreader coupled to the integrated circuits of the second circuit board. The first circuit board and the first thermal spreader have a first thickness. The second daughter board and the second thermal spreader have a second thickness. The system further includes a second compliant board coupled to the second circuit board, a board assembly coupled to first and second compliant boards and a cold-plate assembly in contact with the first and second thermal spreaders. Either of the first or the second compliant boards is configured to expand or contract to account for the differences between the first and second thicknesses.

One or more of the aspects above may include one or more of the following features. 2. A fastener secures the mother board assembly to the cold-plate assembly and extending through one of the first or second daughter board. A fastener secures the mother board assembly to one of the first or the second thermal spreader. The first or second compliant board includes an RF interface board. The first or second compliant board includes conductive elastomeric contacts on at least one side of the first compliant board. The conductive elastomeric contacts include a silver-filled elastomer. The elastomer has a Shore A durometer of about 90. The first or second compliant board and the conductive elastomeric contacts are electrically conductive and configured to provide an RF insertion loss of less than 0.1dB. The first thermal spreader includes a boss that interfaces with the first daughter board to control gaps between the active circuits of the first daughter board and the first thermal spreader. The first thermal spreader includes a first boss that interfaces with the mother board to control a gap between the cold-plate assembly and the first thermal spreader. The first thermal spreader further includes a second boss that interfaces with the board assembly to control a gap between the cold-plate assembly and the first thermal spreader.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of an array antenna formed from a plurality of tile sub-arrays.

FIG. 2A is a partially exploded perspective view of an example of a tile sub-array.

FIG. 2B is a cross-sectional view of the tile sub-array of FIG. 2A taken along lines 2B-2B.

FIG. 2C is a cross-sectional view of the tile sub-array of FIG. 2B with a cold plate.

FIG. 3 is a cross-sectional view of a tile sub-array with the cold plate and a compliant member.

FIG. 4A is a cross-sectional view of an example of a single daughter board/ thermal spreader assembly mounted to a mother board.

FIG. 4B is a cross-sectional view of a thermal spreader of FIG. 4B.

FIG. 5A to 5F are cross-sectional views of single daughter board/ thermal spreader assembly of FIG. 4A with different tolerance stack-ups.

DETAILED DESCRIPTION

A "panel array" (or more simply "panel") refers to a multilayer printed wiring board (PWB) which includes an array of active circuits (or more simply "radiating elements" or "radiators"), as well as RF, logic and DC distribution circuits in one highly integrated PWB. A panel is also sometimes referred to herein as a tile array (or more simply, a "tile").

An array antenna may be provided from a single panel (or tile) or from a plurality of panels. In the case where an array antenna is provided from a plurality of panels, a single one of the plurality of panels is sometimes referred to herein as a "panel sub-array" (or a "tile sub-array").

Reference is sometimes made herein to an array antenna having a particular number of panels. It should of course, be appreciated that an array antenna may be comprised of any number of panels and that one of ordinary skill in the art will appreciate how to select the particular number of panels to use in any particular application.

It should also be noted that reference is sometimes made herein to a panel or an array antenna having a particular array shape and/or physical size or a particular number of active circuits. One of ordinary skill in the art will appreciate that the techniques described herein are applicable to various sizes and shapes of panels and/or array antennas and that any number of active circuits may be used.

Similarly, reference is sometimes made herein to panel or tile sub-arrays having a particular geometric shape (e.g., square, rectangular, round) and/or size (e.g., a particular number of active circuits) or a particular lattice type or spacing of active circuits. One of ordinary skill in the art will appreciate that the techniques described herein are applicable to various sizes and shapes of array antennas as well as to various sizes and shapes of panels (or tiles) and/or panel sub-arrays (or tile sub-arrays).

Thus, although the description provided herein below describes the inventive concepts in the context of an array antenna having a substantially square or rectangular shape and comprised of a plurality of tile sub-arrays having a substantially square or rectangular-shape, those of ordinary skill in the art will appreciate that the concepts equally apply to other sizes and shapes of array antennas and panels (or tile sub-arrays) having a variety of different sizes, shapes, and types of elements. Also, the panels (or tiles) may be arranged in a variety of different lattice arrangements including, but not limited to, periodic lattice arrangements or configurations (e.g., rectangular, circular, equilateral or isosceles

triangular and spiral configurations) as well as non-periodic or other geometric arrangements including arbitrarily shaped array geometries.

Reference is also sometimes made herein to the array antenna including an antenna element (active circuit) of a particular type, size and/or shape. For example, one type of radiating element is a so-called patch antenna element having a square shape and a size compatible with operation at a particular frequency (e.g., 10 GHz) or range of frequencies (e.g., the X-band frequency range). Reference is also sometimes made herein to a so-called "stacked patch" antenna element. Those of ordinary skill in the art will recognize, of course, that other shapes and types of antenna elements (e.g., an antenna element other than a stacked patch antenna element) may also be used and that the size of one or more active circuits may be selected for operation at any frequency in the RF frequency range (e.g., any frequency in the range of about 1 GHz to about 100 GHz). The types of radiating elements which may be used in the antenna of the present invention include but are not limited to notch elements, dipoles, slots or any other antenna elements (regardless of whether the antenna element is a printed circuit element) known to those of ordinary skill in the art.

It should also be appreciated that the active circuits in each panel or tile sub-array can be provided having any one of a plurality of different antenna element lattice arrangements including periodic lattice arrangements (or configurations) such as rectangular, square, triangular (e.g., equilateral or isosceles triangular), and spiral configurations as well as non-periodic or arbitrary lattice arrangements.

Applications of at least some examples of the panel array (sometimes referred to as a "tile array") architectures described herein include, but are not limited to, radar, electronic warfare (EW) and communication systems for a wide variety of applications including ship based, airborne, missile and satellite applications. It should thus be appreciated that the

panel (or tile sub-array) described herein can be used as part of a radar system or a communications system.

At least some examples as described herein are applicable, but not limited to, military, airborne, shipborne, communications, unmanned aerial vehicles (UAV) and/or commercial wireless applications.

The tile sub-arrays to be described herein below can also utilize embedded circulators; a slot-coupled, polarized egg-crate radiator; a single integrated monolithic microwave integrated circuit (MMIC); and a passive radio frequency (RF) circuit architecture. For example, as described further herein, technology described in the following commonly assigned United States Patents can be used in whole or in part and/or adapted to be used with at least some embodiments of the tile subarrays described herein: U.S. Patent Number 6,611,180, entitled "Embedded Planar Circulator"; U.S. Patent Number 6,624,787, entitled "Slot Coupled, Polarized, Egg-Crate Radiator"; and/or U.S. Patent Number 6,731,189, entitled "Multilayer stripline radio frequency circuits and interconnection methods." Each of the above patents is hereby incorporated herein by reference in their entireties.

Referring now to FIG. 1, an array antenna 10 is comprised of a plurality of tile sub-arrays 12a-12N. It should be appreciated that in this example, N total tile sub-arrays 12 include the entire array antenna 10. In one particular example, the total number of tile sub-arrays is sixteen tile sub-arrays (i.e., N = 16). The particular number of tile sub-arrays 12 used to provide a complete array antenna can be selected in accordance with a variety of factors including, but not limited to, the frequency of operation, array gain, the space available for the array antenna and the particular application for which the array antenna 10

is intended to be used. Those of ordinary skill in the art will appreciate how to select the number of tile sub-arrays 12 to use in providing a complete array antenna.

As illustrated in tiles 12b and 12i, in the example of FIG. 1, each tile sub-array 12a-12N includes eight rows 13a-13h of active circuits 15 (also known as antenna elements) with each row containing eight active circuits 15. Each of the tile sub-arrays 12a-12N is thus said to be an eight by eight (or 8 x 8) tile sub-array. It should be noted that each active circuit 15 is shown in phantom in FIG. 1 since the active circuits 15 are not directly visible on the exposed surface (or front face) of the array antenna 10. Thus, in this particular example, each tile sub-array 12a-12N includes sixty-four (64) active circuits. In the case where the array 10 includes sixteen (16) such tiles, the array 10 includes a total of one-thousand and twenty-four (1,024) active circuits 15.

In another example, each of the tile sub-arrays 12a-12N includes 16 active circuits. Thus, in the case where the array 10 includes sixteen (16) such tiles and each tiles includes sixteen (16) active circuits 15, the array 10 includes a total of two-hundred and fifty-six (256) active circuits 15.

In view of the above examples, it should thus be appreciated that each of the tile sub-arrays can include any desired number of active circuits 15. The particular number of active circuits to include in each of the tile sub-arrays 12a-12N can be selected in accordance with a variety of factors including but not limited to the desired frequency of operation, array gain, the space available for the antenna and the particular application for which the array antenna 10 is intended to be used and the size of each tile sub-array 12. For any given application, those of ordinary skill in the art will appreciate how to select an appropriate number of radiating active circuits to include in each tile sub-array. The total number of active circuits 15 included in an antenna array such as antenna array 10 depends

upon the number of tiles included in the antenna array and as well as the number of active circuits included in each tile.

Each tile sub-array is electrically autonomous (except any mutual coupling which occurs between active circuits 15 within a tile and on different tiles). Thus, the RF feed circuitry which couples RF energy to and from each radiator on a tile is incorporated entirely within that tile (i.e., all of the RF feed and beamforming circuitry which couples RF signals to and from active circuits 15 in tile 12b are contained within tile 12b). In one example, each tile includes one or more RF connectors and the RF signals are provided to the tile through the RF connector(s) provided on each tile sub-array.

Also, signal paths for logic signals and signal paths for power signals which couple signals to and from transmit/receive (T/R) circuits are contained within the tile in which the T/R circuits exist. RF signals are provided to the tile through one or more power/ logic connectors provided on the tile sub-array.

The RF beam for the entire array 10 is formed by an external beamformer (i.e., external to each of the tile subarrays 12) that combines the RF outputs from each of the tile sub-arrays 12a-12N. As is known to those of ordinary skill in the art, the beamformer may be conventionally implemented as a printed wiring board stripline circuit that combines N sub-arrays into one RF signal port (and hence the beamformer may be referred to as a 1:N beamformer).

It should be appreciated that the examples of the tile sub-arrays described herein (e.g., tile sub-arrays 12a-12N) differ from conventional array architectures in that the microwave circuits of the tile sub-arrays are contained in circuit layers which are disposed in planes that are parallel to a plane defined by a face (or surface) of an array antenna (e.g., surface 10a of array antenna 10) made up from the tiles. In FIG. 1, for example, the circuits

15 provided on the layers of circuit boards from which the tiles 12a-12N are provided are all parallel to the surface 10a of array antenna 10. By utilizing circuit layers that are parallel to a plane defined by a face of an array antenna, the tile architecture approach results in an array antenna having a reduced profile (i.e., a thickness which is reduced compared with the thickness of conventional array antennas).

Advantageously, the tile sub-array embodiments described herein can be manufactured using standard printed wiring board (PWB) manufacturing processes to produce highly integrated, passive RF circuits, using commercial, off-the-shelf (COTS) microwave materials, and highly integrated, active monolithic microwave integrated circuits (MMIC's). This results in reduced manufacturing costs. Array antenna manufacturing costs can also be reduced since the tile sub-arrays can be provided from relatively large panels or sheets of PWBs using conventional PWB manufacturing techniques.

Referring to FIGS. 2A to 2C, in one particular example of the tile sub-arrays 12a-12N is a tile sub-array 12'. The tile sub-array 12' includes a mother board 20, an RF interface board 24, eight daughter boards (e.g., a daughter board 32a-32h) with active circuits 15 on each daughter board and eight thermal spreaders (e.g., a thermal spreader 34a-34h) attached to active circuits 15 of a corresponding daughter board. In one example, the active circuits 15 are secured to the thermal spreaders 34a-34h using solder techniques described in U.S. patent application number 12/580,356 entitled "Cooling Active Circuits" which is incorporated herein in it entirety.

In one example, each daughter board 32a-32h includes sixteen active circuits 15. Instead of having one large daughter board with active circuits 15 connected to one thermal spreader, this configuration increases yield during manufacturing by reducing the size of the daughter board into smaller pieces. In addition, it is easier to rework problems with smaller

daughter boards as opposed to larger one piece daughter boards. For example, it is more cost effective to throw away sixteen active circuits 15 because of an active circuit failure than one hundred twenty-eight active circuits.

Cooling a number of substantially coplanar active circuits 15 (e.g., integrated circuits) with a single cold plate in direct contact with top surfaces of the thermal spreaders 34a-34h is difficult because of the many tolerances that exist resulting from height variations (thicknesses). In particular, a cold plate 40 with channels 42 for receiving coolant is unable to make contact with all of the thermal spreaders 34e-34h (FIG. 2C) leaving spaces 76a-76c between the thermal spreaders 34e, 34f, 34h and the cold plate 40. By not being in direct contact with the cold plate 40, the thermal spreaders 34e, 34f, 34h do not efficiently transfer heat away from the active circuits 15.

In one example, the active circuits 15, the thermal spreaders 34 and the daughter boards 32 may have different thicknesses. With respect to FIG. 2B, the thickness, T_h, which includes thicknesses of the thermal spreader 34h, the daughter board 32h and active circuits 15 is different from the thickness, T_e, which includes thicknesses of the thermal spreader 34e,the daughter board 32e and active circuits 15. In one particular example, the daughter boards 32a-32h, which are about .100 inches thick have thickness tolerances of +/- .01 inches and the thermal spreaders 34a-34h have thickness tolerances of +/-.001 inches resulting in a total thickness tolerance of +/- .011 inches. As described herein, a compliant member may be used to compensate for varying thicknesses between the daughter board and thermal spreader subassemblies, e.g., a compliant member that compensates for the .011 inches in the previous example. While this disclosure describes cooling active circuits in an environment of an active, electronically scanned array (AESA) panel architecture system,

the techniques described herein may be used in any environment to cool multiple objects of varying thicknesses and/or are substantially coplanar.

Referring to FIG. 3, one technique to eliminate the air spaces 76a-76c (FIG. 2C) between the thermal spreaders 34a-34h and the cold plate 40 is to use the compliant member between the mother board 20 and the active circuits 15. In one example, an RF interface board 124 is the compliant member. For example, the air spaces 76a-76c (FIG. 2C) between the thermal spreaders 34e-34h and the cold plate 40 are substantially eliminated (e.g., reduced to less than .002 inches) because the RF interface board 124 can compensate for the variances in the thicknesses of the different thermal spreader/daughter board assemblies. In one particular example, each side of the RF interface board 124 includes a plurality of conductive elastomeric contacts 200 capable of providing an adequate RF interconnect and having elastic properties such to minimize compression set over extended time and temperature ranges. The RF interface board 124 including the conductive elastomeric contacts 200 is also electrically conductive so that RF signals generated by the actives circuits 15 can be transmitted to the circulator/radiator assembly 150 (see FIG. 4). In one example, the conductive elastomeric contacts 200 include a compliant material such as a silver-filled elastomer with a Shore A durometer of about 90. In another example, the interface board 124, including the conductive elastomeric contacts 200, is also electrically conductive and configured to provide an RF insertion loss of less than 0.1dB. In other examples, only one side of the RF interface board 124 includes the conductive elastomeric contacts 200 and the opposite side is either integrated with the daughter board 32 or the mother board 20.

Referring to FIGS. 4A and 4B, the thermal spreaders/daughter board subassemblies may be configured in other ways. In particular, unlike FIG. 3, which depicts a simplistic

thermal spreader 34e, FIGS. 4A and 4B depict a thermal spreader 234e, which is a more complex thermal spreader configuration. The thermal spreader 234e/daughter board 32e is coupled to the compliant RF interface board 124, the mother board 20, an RF interface board 24 and to a circulator/radiator assembly 150. As used herein an RF panel assembly includes the circulator/radiator assembly 150, an interface 174, the mother board 20, the compliant RF interface board 124, the daughter board 32e, and the thermal spreader 234e.

The thermal spreaders (e.g., the thermal spreader 234e shown in FIG. 4) include bosses (e.g., a boss 210a, a boss 210b, a boss 212a and a boss 212b). The bosses 210a, 210b are configured to control any gaps between the thermal spreader 234e and the cold plate 40 (not shown in FIG. 4). The bosses 212a, 212b are configured to control any gaps between the active circuits 15 and the thermal spreader 234e.

In one example, either of the bosses 210a, 210b have a thickness tolerance, T_B, of about +/- .001 inches and either of the bosses 212a, 212b have a thickness tolerance, T_A, of about +/- .001 inches. If the daughter board 32e has a thickness tolerance of about +/- .010 inches, then the compliant RF interface board 124 is configured to have an adjustable thickness of at least +/-.012 inches.

Screws 214a, 214b are used to mount the thermal spreader 234e/daughter board 32e subassembly to the mother board 20 and the circulator/radiator assembly 150. The screws 214a, 214b extend through the bosses 210a, 210b respectively and through the mother board 20, the interface 174 and the circulator/radiator assembly 150. In one example, the screws 214a, 214b pass through a clearance hole (not shown) in the respective bosses 210a, 210b and the mother board 20, RF interface board 124 and engage threads (not shown) in the circulator/radiator assembly 150.

Screws 202a, 202b are used to mount the RF panel assembly to the cold plate 40 (not shown in FIG. 4A). In one example, the screws 202a, 202b pass through clearance holes (not shown) in the circulator/radiator assembly 150, the interface 74, the mother board 20, the compliant RF interface board 124, the daughter board 32e, the thermal spreader 234e and engage threads (not shown) in the cold plate 40 (not shown in FIG. 4A). The screws 202a, 202b, 214a, 214b perform a clamping function ensuring that the RF interface board 124 has adequate compression for RF transmission and control the gap between the thermal spreader 234e and the cold plate 40 to ensure efficient transfer of heat.

FIG. 5A depicts a minimum tolerance stack-up with the RF interface board 124 under minimum compression. FIG. 5B depicts a nominal tolerance stake-up with the RF interface board 124 under nominal compression. FIG. 5C depicts a maximum tolerance stake-up with the RF interface board 124 under maximum compression.

While screws 202a, 202b, 214a, 214b have been described one of ordinary skill in the art would recognize that the screws 202a, 202b, 214a, 214b may be replaced with fasteners (e.g., standoffs and so forth) or other clamping structures. Also, one of ordinary skill in the art would recognize other known methods or techniques to ensure contact between the cold plate and the thermal spreaders and to ensure compression between the daughter board 234e, mother board 20 and the compliant RF interface board 124.

The processes described herein are not limited to the specific embodiments described. Elements of different embodiments described herein may be combined to form other embodiments not specifically set forth above. Other embodiments not specifically described herein are also within the scope of the following claims.

What is claimed is:

1. An active, electronically scanned array (AESA) panel architecture system comprising:

a first daughter board comprising active circuits;

a first thermal spreader coupled to the active circuits of the first daughter board, the first daughter board and the first thermal spreader having a first thickness;

a first compliant board coupled to the first daughter board;

a second daughter board comprising active circuits;

a second thermal spreader coupled to the active circuits of the second daughter board, the second daughter board and the second thermal spreader having a second thickness different from the first thickness;

a second compliant board coupled to the second daughter board;

a mother board assembly coupled to first and second compliant boards; and

a cold-plate assembly in contact with the first thermal spreader and the second thermal spreader,

wherein either of the first compliant board or the second compliant board is configured to expand or contract to account for the differences in thicknesses between the first thickness and the second thickness.

2. The system of claim 1, further comprising a fastener securing the mother board assembly to the cold-plate assembly and extending through one of the first or second daughter board.

3. The system of claim 1, further comprising a fastener securing the mother board assembly to one of the first or the second thermal spreader.

4. The system of claim 1 wherein the first or second compliant board comprises an RF interface board.

5. The system of claim 1 wherein the first or second compliant board comprises conductive elastomeric contacts on at least one side of the first compliant board.

6. The system of claim 1 wherein the conductive elastomeric contacts comprises a silver-filled elastomer.

7. The system of claim 1 wherein the elastomer has a Shore A durometer of about 90.

8. The system of claim 1 wherein the first or second compliant board and the conductive elastomeric contacts are electrically conductive and configured to provide an RF insertion loss of less than 0.1dB.

9. The system of claim 1 wherein the first thermal spreader comprises a boss that interfaces with the first daughter board to control gaps between the active circuits of the first daughter board and the first thermal spreader.

10. The system of claim 1 wherein the first thermal spreader comprises a first boss that interfaces with the mother board to control a gap between the cold-plate assembly and the first thermal spreader.

11. An active, electronically scanned array (AESA) panel architecture system comprising:

a first daughter board comprising active circuits;

a first thermal spreader coupled to the active circuits of the first daughter board, the first daughter board and the first thermal spreader having a first thickness;

a first RF interface board coupled to the first daughter board, the first RF interface board comprising compliant elements on at least one side of the first RF interface board;

a second daughter board comprising active circuits;

a second thermal spreader coupled to the active circuits of the second daughter board, the second daughter board and the second thermal spreader having a second thickness different from the first thickness;

a second RF interface board coupled to the second daughter board, the second RF interface board comprising compliant elements on at least one side of the second RF interface board;

a mother board assembly coupled to first and second RF interface boards; and

a cold-plate assembly in contact with the first thermal spreader and the second thermal spreader,

wherein the first and second RF interface boards are configured to expand or contract to account for the differences in thicknesses between the first thickness and the second thickness,

wherein the first RF interface board provides electrical coupling between the active circuits of the first daughter board and the mother board, and

wherein the second RF interface board provides electrical coupling between the active circuits of the second daughter board and the mother board.

12. The system of claim 11, further comprising a first fastener securing the mother board assembly to the cold-plate assembly and extending through one of the first or second daughter board.

13. The system of claim 12, further comprising a second fastener securing one of the first or the second thermal spreader to the mother board assembly.

14. The system of claim 11 wherein the first thermal spreader comprises a first boss that interfaces with the first daughter board to control gaps between the active circuits of the first daughter board and the first thermal spreader.

15. The system of claim 11 wherein the first thermal spreader comprises a second boss that interfaces with the mother board to control a gap between the cold-plate assembly and the first thermal spreader.

16. A system comprising:

a first circuit board comprising integrated circuits;

a first thermal spreader coupled to the integrated circuits of the first circuit board, the first circuit board and the first thermal spreader having a first thickness;

a first compliant board coupled to the first circuit board;

a second circuit board comprising integrated circuits;

a second thermal spreader coupled to the integrated circuits of the second circuit board, the second circuit board and the second thermal spreader having a second thickness different from the first thickness;

a second compliant board coupled to the second circuit board;

a board assembly coupled to first and second compliant boards; and

a cold-plate assembly in contact with the first thermal spreader and the second thermal spreader,

wherein either of the first compliant board or the second compliant board is configured to expand or contract to account for the differences in thicknesses between the first thickness and the second thickness.

17. The system of claim 16, further comprising a fastener securing the board assembly to the cold-plate assembly and extending through one of the first or second circuit board.

18. The system of claim 16, further comprising a fastener securing the board assembly to one of the first or the second thermal spreader.

19. The system of claim 16 wherein the first or second compliant board comprises conductive elastomeric contacts on at least one side of the first compliant board.

20. The system of claim 16 wherein the first thermal spreader comprises a first boss that interfaces with the first circuit board to control gaps between the integrated circuits of the first circuit board and the first thermal spreader.

wherein the first thermal spreader further comprises a second boss that interfaces with the board assembly to control a gap between the cold-plate assembly and the first thermal spreader.

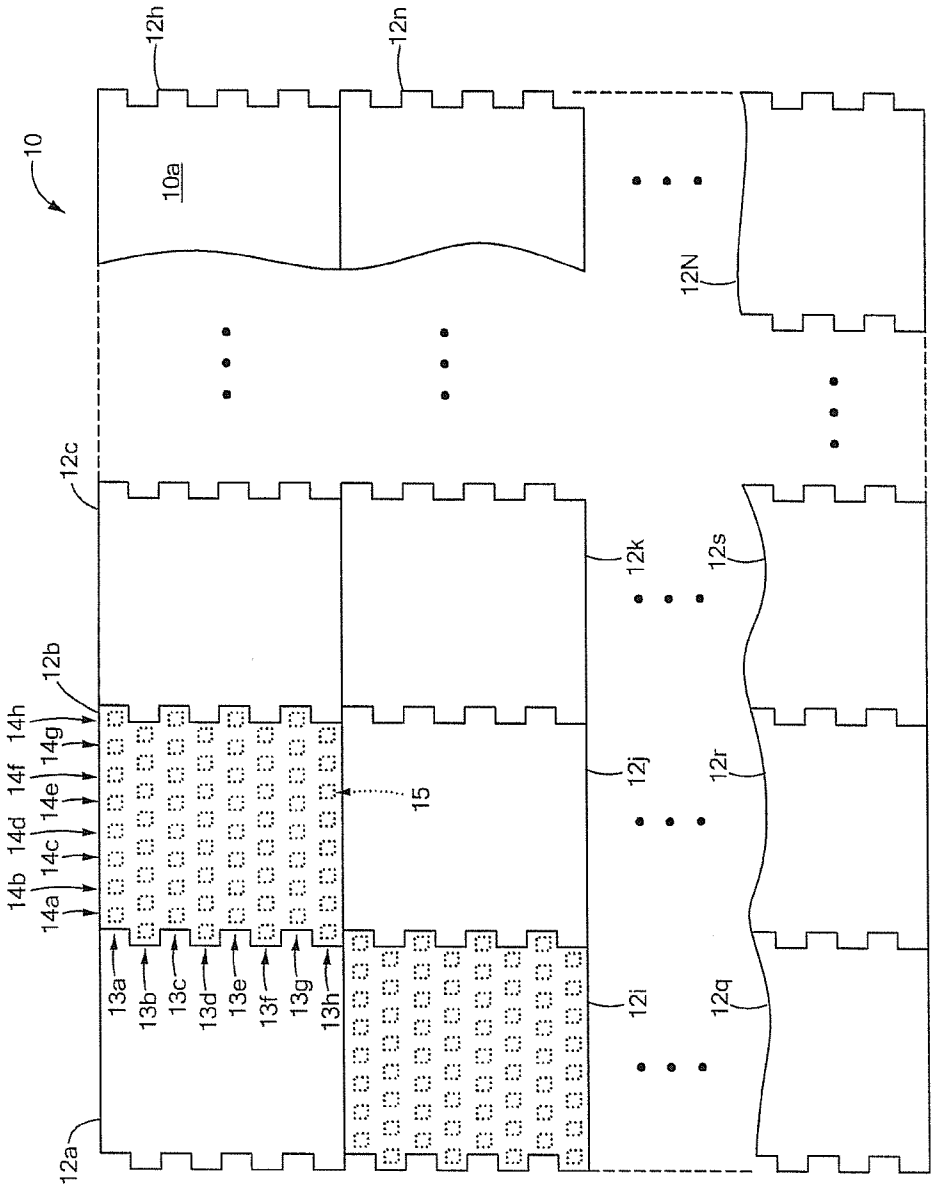
10
10a
12a
12b
12c
12h
12n
12N
12i
12j
12k
12q
12r
12s
13a
13b
13c
13d
13e
13f
13g
13h
14a
14b
14c
14d
14e
14f
14g
14h
15

FIG. 1

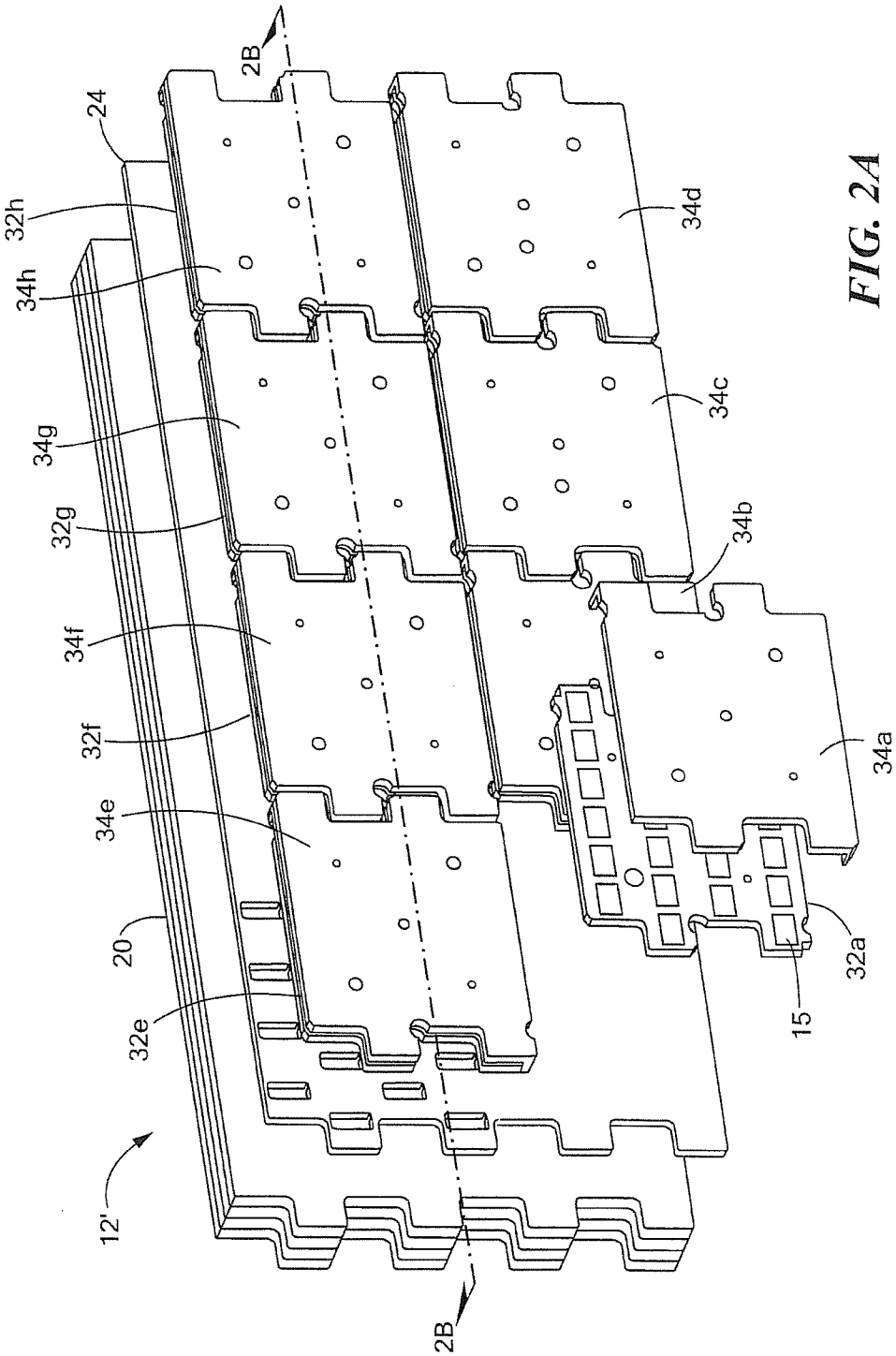
2B
24
32h
34h
34g
32g
34f
32f
34e
20
32e
12'
2B
34d
34c
34b
34a
32a
15

FIG. 2A

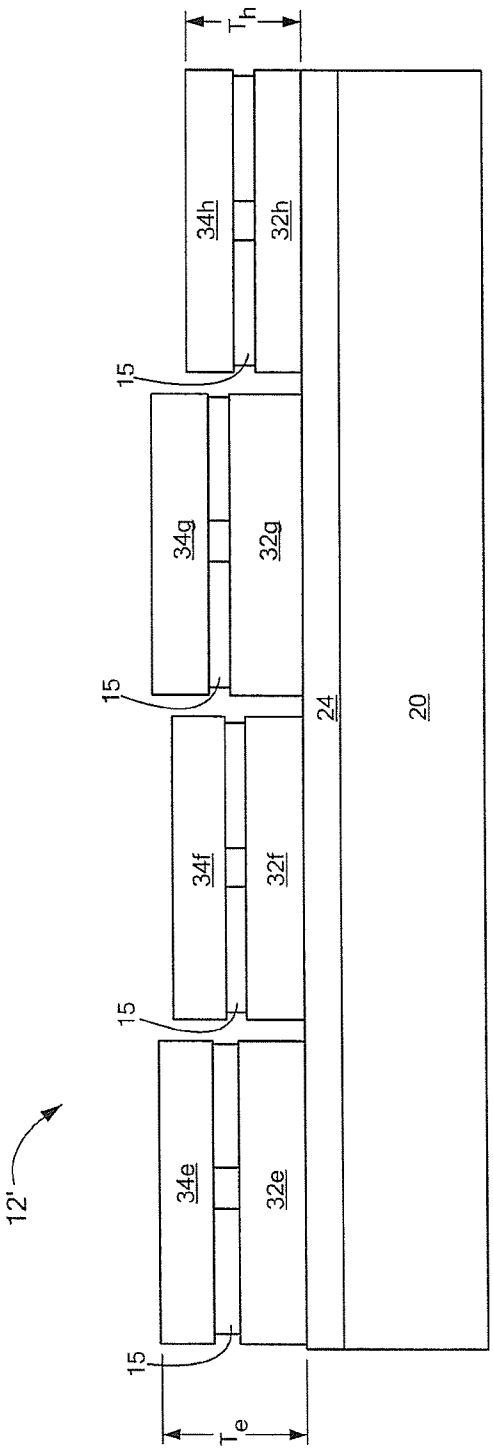

FIG. 2B

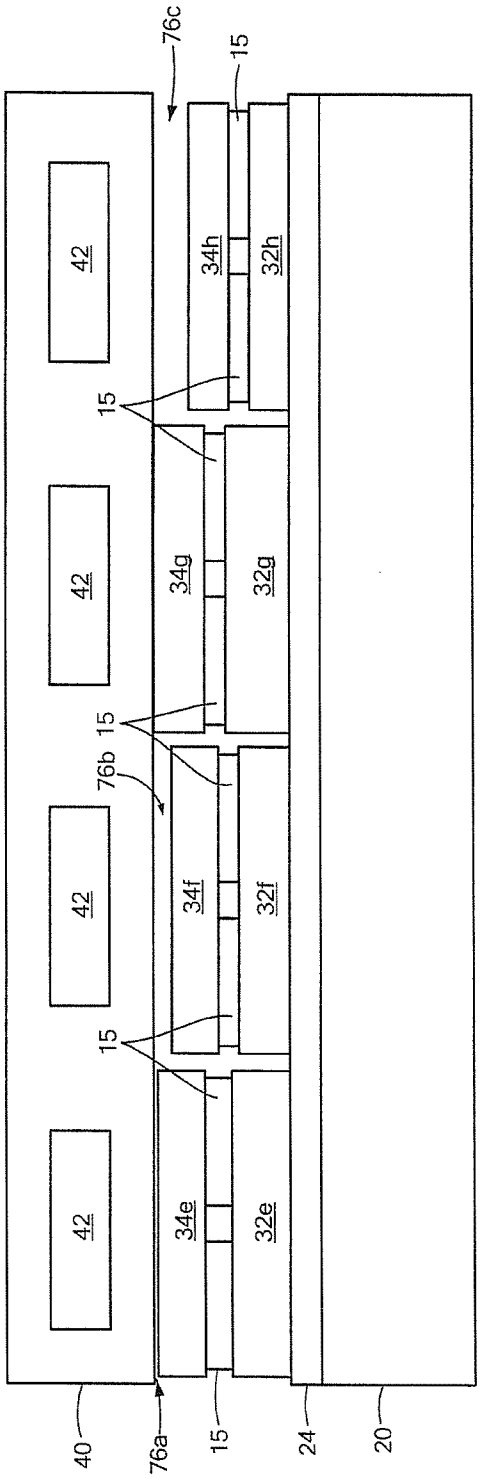
76c
15
42
34h
32h
15
42
34g
32g
15
76b
42
34f
32f
15
42
34e
32e
40
76a
15
24
20

FIG. 2C

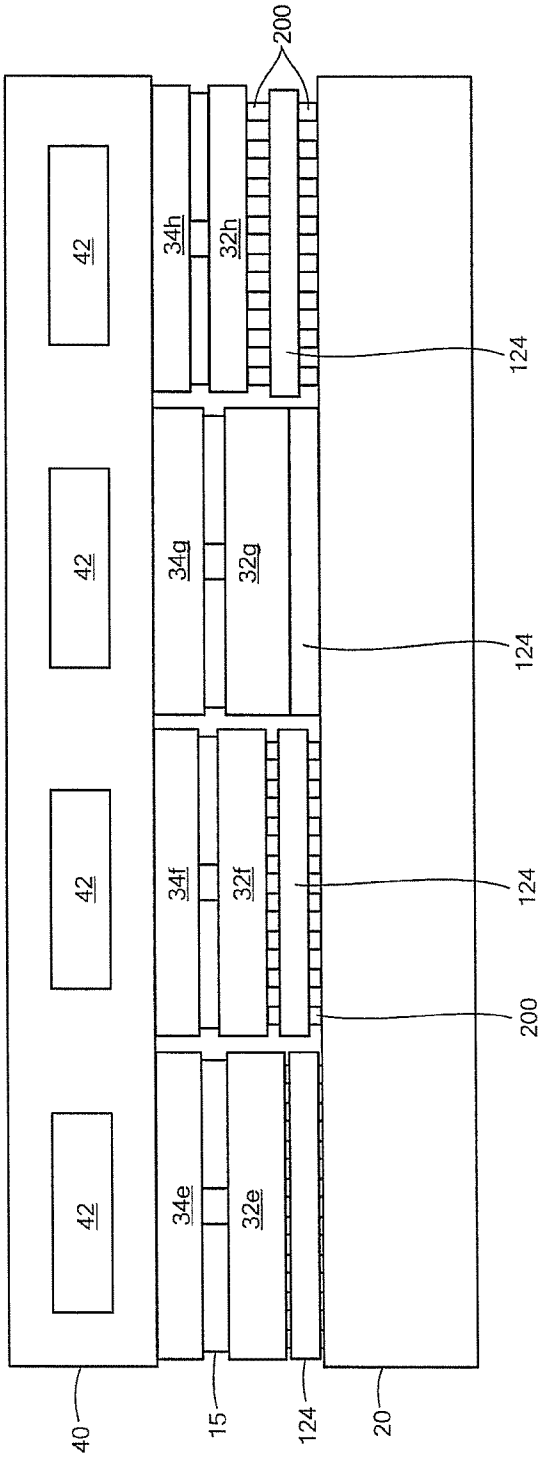
200
42
34h
32h
124
42
34g
32g
124
42
34f
32f
124
200
42
34e
32e
40
15
124
20

FIG. 3

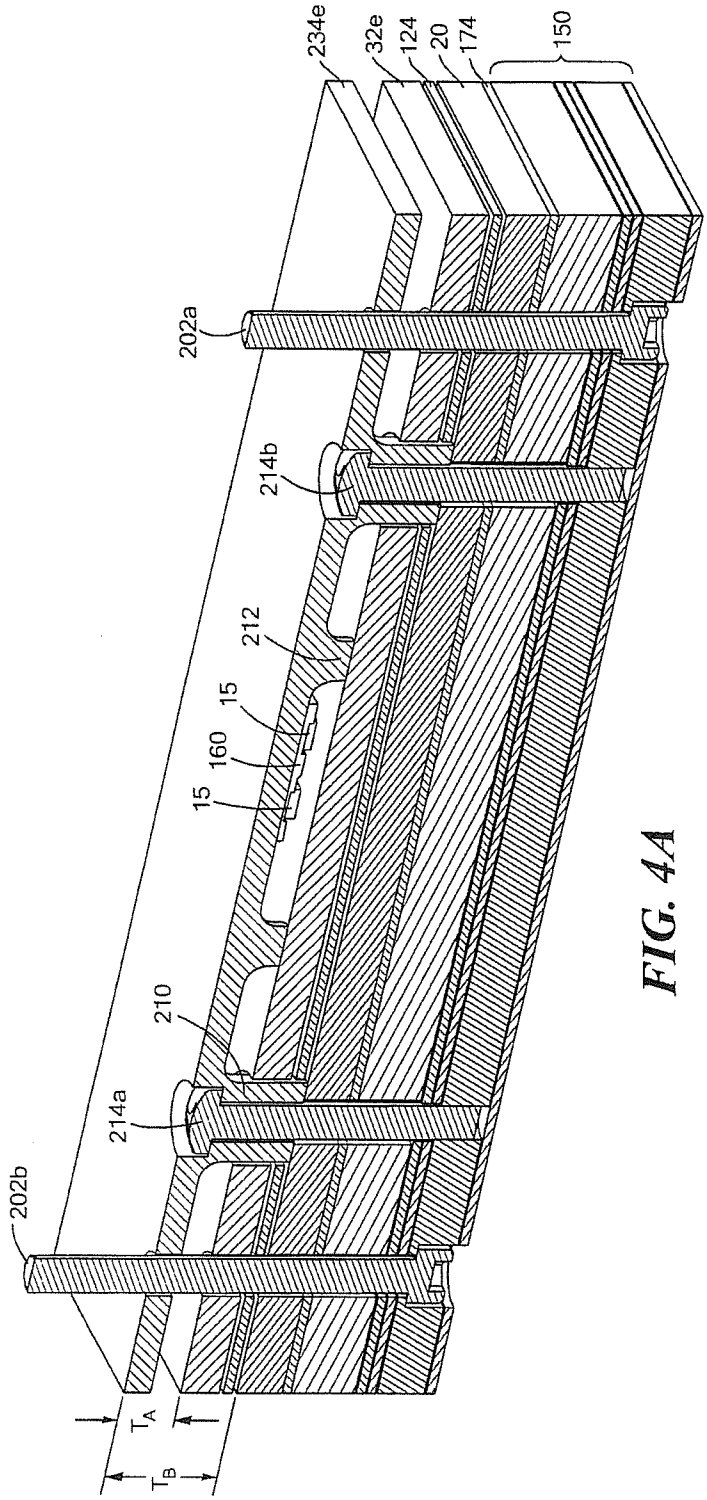
234e
32e
124
20
174
150
202a
214b
212
15
160
15
210
214a
202b
T_A
T_B

FIG. 4A

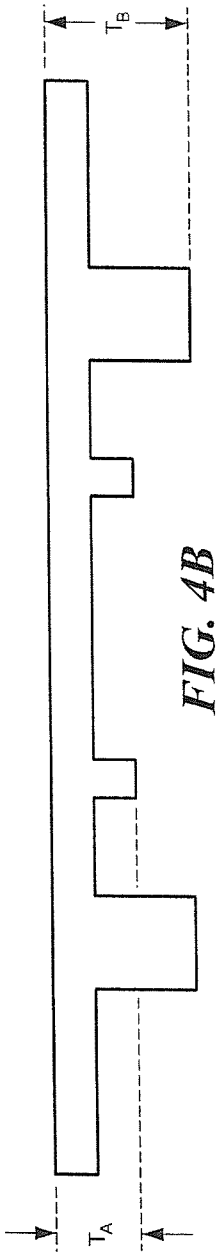
T_B
T_A

FIG. 4B

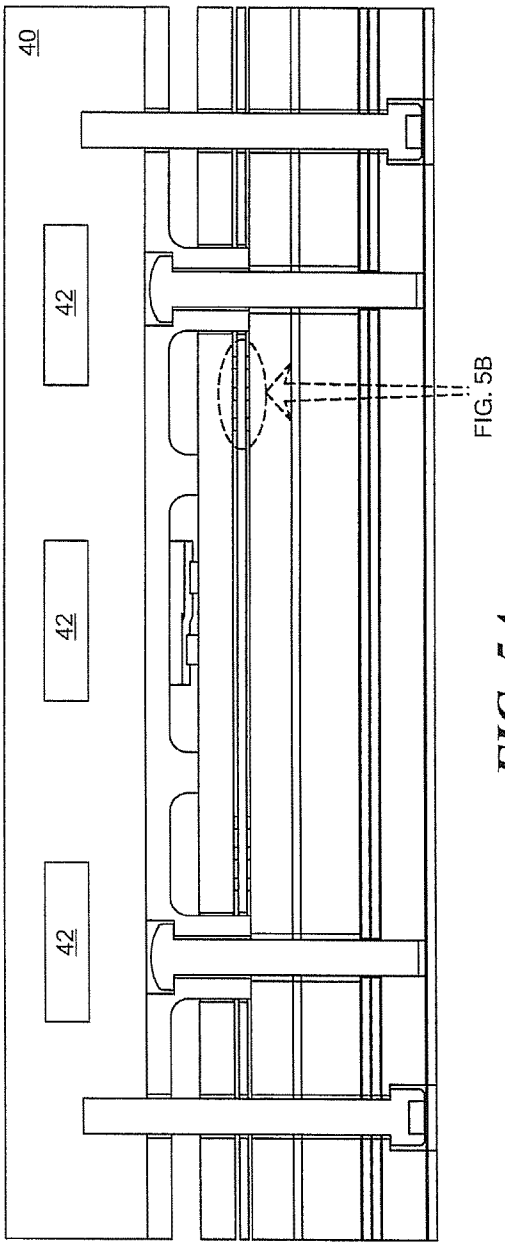

FIG. 5A

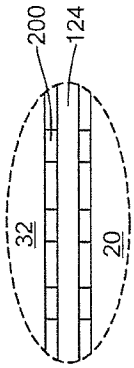

FIG. 5B

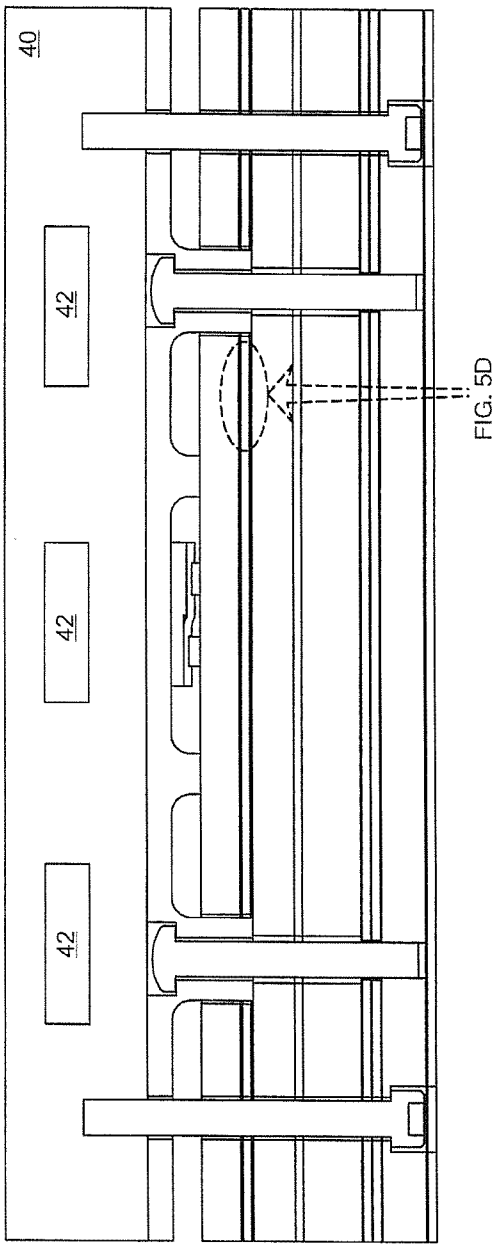

FIG. 5C

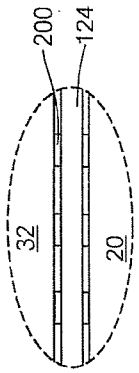

FIG. 5D

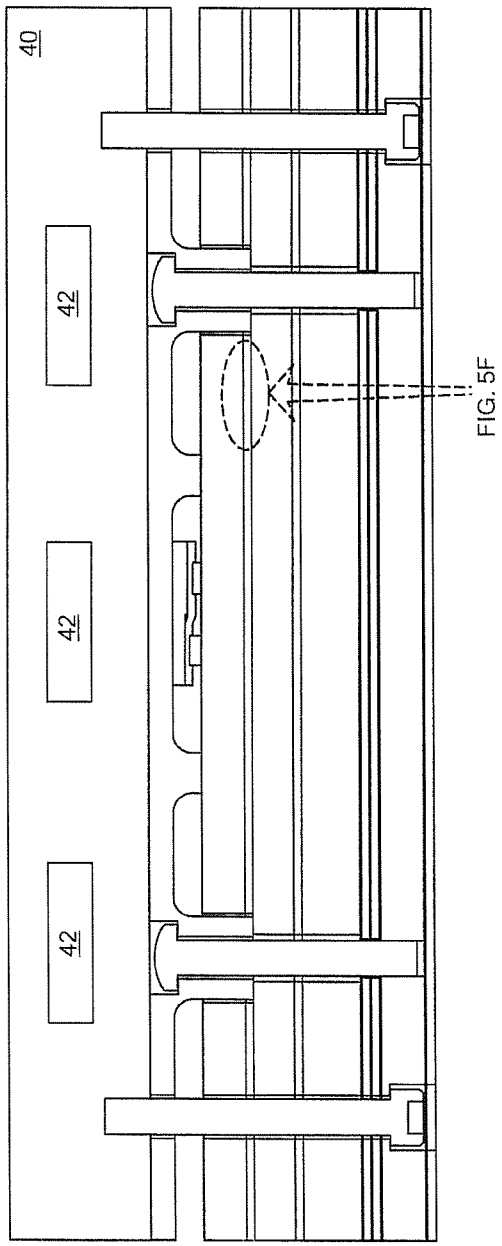

FIG. 5E

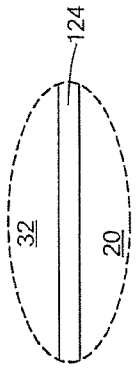

FIG. 5F