METHOD AND APPARATUS FOR ADJUSTING ELECTRICAL CHARACTERISTICS OF SIGNAL TRACES IN LAYERED CIRCUIT BOARDS

Abstract: The electrical characteristics of a signal trace in a layered circuit board are adjusted by selectively modifying the dielectric constant and/or the magnetic permeability of an insulating material layer in the vicinity of a signal interconnect. The electrical characteristic is modified by adding a layer of different material into the circuit board layers either above or below the circuit board plane containing the trace. The different material could be any insulating material with a different dielectric and/or permeability constant. In one embodiment, during the circuit board lamination process, only a selected trace is covered with a layer of the different material, thus the electrical properties of other traces will not be affected. The layer of different material on the trace may cover the entire length of the trace, or it covers one or more parts of the trace, as the adjustment of the electrical properties requires. In another embodiment, the insulating material separating the trace from a reference plane is replaced with a different material in the vicinity of the selected trace. In still another embodiment, the insulating material separating the trace from the reference plane is modified to change its dielectric constant and/or magnetic permeability in the vicinity of the selected trace.
METHOD AND APPARATUS FOR ADJUSTING ELECTRICAL CHARACTERISTICS OF SIGNAL TRACES IN LAYERED CIRCUIT BOARDS
FIELD OF THE INVENTION

This invention relates to electronic systems, and more particularly to electrical interconnection apparatus employing a layered circuit board or printed circuit board.

BACKGROUND OF THE INVENTION

Present day electronic and semiconductor integrated circuits are typically built on a multi-layer substrate or board which is used to interconnect the electronic components or devices which comprise the circuit. The multi-layer boards or substrates, in turn, consist of planar conductive layers separated by planar insulating layers. Portions of some of the conductive layers may be removed leaving electrically conductive signal lines or “traces” which connect the components on a particular layer.

Conductive traces in different layers are typically electrically connected by forming holes in the intervening layers and plating the inside surfaces of the holes to form structures called “plated-through vias.”

Signals in digital electronic systems typically carry information by alternating between two voltage levels (i.e., a low voltage level and a high voltage level) so that a digital signal, over time, has an alternating voltage characteristic with an average frequency. Digital electronic systems are continually being produced which operate at higher and higher signal frequencies. However, in order for electronic circuits to operate at high frequencies, the traces which carry digital signals from one component to another, called signal interconnects, must have predetermined electrical characteristics, such as signal propagation delays and impedances.

In particular, in a complex digital system, there are many signal interconnects which all may have to be designed to meet a certain impedance and delay characteristics. Both the impedance and the per-unit-length delay of traces are determined by the mechanical dimensions and material properties. The per-unit-length signal propagation delay in a trace is primarily influenced by two factors: the trace length and the dielectric constant of the insulating material in the insulating layer between the trace and the power and ground plane (the power and ground planes are collectively called “reference planes.”) The characteristic impedance of a trace is
primarily determined by the cross sectional dimensions of the trace and the reference plane layers and the dielectric constant of the insulating material.

The electrical characteristics of the traces are generally determined during the circuit board construction or "layout" process. During the usual layout procedure, first the circuit board construction materials are selected and then the stackup (layer height of the dielectric insulating materials) is determined. The materials and stackup determine the required trace width to obtain a desired impedance.

Next, in the layout procedure, the major electronic components are arranged on the circuit board and connected by signal interconnects using a trace width which is sufficient to obtain the desired impedance. Since the dielectric constant of the insulating layer has already been determined, a desired signal propagation delay is obtained by adjusting the length of the traces.

It is typical in system requirements that signals are grouped, and, within each group, all traces are designed to have nominally the same signal propagation delay. These traces are said to be "equalized." The equalization procedure involves determining the maximum propagation delay of the traces in the group, which maximum propagation delay is usually the delay of the trace which connects points with the largest physical separation. For example, Figure 1 illustrates a circuit board 100 with two signal interconnect traces 102 and 104 with different lengths. If the traces were both straight, the maximum propagation delay would occur in trace 102 because its terminations 108 and 110 are physically farther apart than the terminations 112 and 114 of trace 104. The equalization of the remaining traces then requires the lengthening of traces whose length would otherwise would yield a smaller delay, for example trace 104. The extra length is produced by including a serpentine or meander shape 106 in the trace 104 to be lengthened. However, in densely populated circuit boards, the space required by such equalization meanders may be hard to allocate.

In addition, the characteristic impedance and the signal propagation delay of a trace are affected by the proximity of other parts of the circuit board, such as by traces in another board layer which carry signals, or by plated through holes, or by cutouts on the power and ground planes close to the trace in question. To compensate for these effects, it may be necessary to readjust the trace dimensions and length in order to
achieve a desired signal propagation and characteristic impedance. Such a readjustment on a densely populated board may also be hard to implement.

It would thus be desirable to have a method and apparatus which could selectively adjust electrical characteristics of a signal interconnect without requiring equalization meanders or an adjustment of the trace dimensions and length.

**SUMMARY OF THE INVENTION**

In accordance with one illustrative embodiment of the invention, the foregoing objects are achieved by selectively modifying the dielectric constant and/or the magnetic permeability of the insulating material in the vicinity of a signal interconnect. The dielectric constant and the permeability are modified by adding a layer of different material into the circuit board layers either above or below the circuit board plane containing the trace. The different material could be any insulating material, a magnetic material or a combined material with a different dielectric and/or permeability constant.

In one embodiment, during the circuit board lamination process, only a selected trace is covered with a layer of the different material, thus the electrical properties of other traces will not be affected. The layer of different material on the trace may cover the entire length of the trace, or it cover one or more parts of the trace, as the adjustment of the electrical properties requires.

In another embodiment, the insulating material separating the trace from the power or ground plane is replaced with a different material in the vicinity of the selected trace.

In still another embodiment, the insulating material separating the trace from the power or ground plane is modified to change its dielectric constant and/or permeability constant in the vicinity of the selected trace.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The above and further advantages of the invention may be better understood by referring to the following description in conjunction with the accompanying drawings in which:
Figure 1 is a top view of a prior art electronic circuit board illustrating two signal traces of different length and utilizing a meander pattern to equalize signal propagation delays.

Figures 2A and 2B are schematic illustrations of two electronic circuit board illustrating two common layered constructions.

Figures 3A and 3B illustrate an embodiment of the invention in which materials are applied over a signal trace to vary the trace electrical characteristics.

Figures 4A and 4B illustrate an embodiment of the invention in which the composition of the insulating material in the vicinity of the trace is modified to vary the trace electrical characteristics.

**Detailed Description**

Figure 2A is a perspective view of a layered circuit board construction in which the invention can be used. This structure may represent a conventional printed circuit board or an integrated electronic circuit substrate with a structure typically called "microstrip." The structure is comprised of a plurality of conductive planes of which two, 200 and 202, are illustrated. The conductive planes are separated by a dielectric layer 204 comprised of an insulating material. In the case of printed circuit boards, the insulating layer 204 is commonly composed of a fiberglass-epoxy composite material called FR4 although other materials, such as ceramics, are also used. In the case of integrated circuits, the insulating layer may be silicon. Some of the conductive planes are etched away to form traces. In Figure 2, plane 200 has been etched to form a trace of which a portion 206 is shown. Plane 202 is generally a reference plane at ground potential. The trace has a width w and a thickness t. In a printed circuit board construction, each conductive plane is typically made of copper. In other layered board constructions, the conductive planes may be comprised of other materials such as aluminum or gold.

In a structure such as that illustrated in Figure 2A, the characteristic impedance "Z₀" of the signal trace is given approximately by the following equation:

\[
Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right) \text{ ohms}
\]
where $\varepsilon_r$ is the relative dielectric constant of the dielectric layer. The propagation delay $t_{pd}$ of the trace per unit length is approximated by the following equation:

$$t_{pd} = \frac{1.017\sqrt{0.475\varepsilon_r + 0.67}}{c} \text{ sec/m}$$

where $c$ is the speed of light in a vacuum (approximately 3 x $10^8$ m/sec.)

Figure 2B is a perspective view of a second common type of layered circuit board construction in which the invention can be used. This structure may represent a conventional printed circuit board or an integrated electronic circuit substrate with a structure typically called “stripline.” The structure is comprised of a plurality of conductive planes of which three, 208, 210 and 216, are illustrated. In a printed circuit board construction, each conductive plane is typically made of copper and planes 208 and 210 are reference planes that are generally grounded. The conductive planes are separated by dielectric layers 212 and 214 which may also be comprised of an insulating material. In the case of printed circuit boards, the insulating layers 212 and 214 are commonly composed of FR4 composite material. Some of the conductive planes are etched away to form traces. In Figure 2B, plane 216 has been etched to form a trace of which a portion 216 is shown (the upper conductive plane 208 and a portion of insulating layer 212 has been removed to reveal trace 216.) The trace has a width $w$ and a thickness $t$.

In a structure such as that illustrated in Figure 2B, the characteristic impedance $Z_o$ of the signal trace is approximated by the following equation:

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{4h}{0.67\pi w \left(0.8 + \frac{t}{w}\right)} \right) \text{ ohms}$$
The propagation delay \( t_{pd} \) of the trace per unit length is approximately given by the following equation:

\[
t_{pd} = \frac{\sqrt{\varepsilon_r}}{c} \text{ sec/m}
\]

Although only two circuit board constructions are shown, in actual printed-circuit-board constructions, other structures are also commonly used. These additional structures include embedded microstrip, offset stripline, co-planar traces and other configurations. Embedded microstrip is basically a microstrip structure as illustrated in Figure 2A with another layer of dielectrics above the trace, but without a top reference plane as illustrated in Figure 2B. Offset stripline is a structure having two or more signal trace layers between two reference planes, where the signal layers are not halfway between the reference planes, hence the name 'offset' stripline. If more than one signal layer is used between two reference planes, to minimize coupling between the signal layers, the layers are usually positioned so that the traces run orthogonal to each other in the different layers. Finally, co-planar transmission lines are structures in which both traces are on the same layer above or below a dielectric support. In general, the characteristic impedance and propagation delay values for all kind of printed-circuit-board structures are well known to those skilled in the art. In general to determine the characteristic impedance of layered, conventional field modeling software is used.

Figures 3A and 3B represent a top view and a cross-sectional view of a portion of a multi-layered circuit board 300. In particular, Figure 3B is a cross-section of the board illustrated in Figure 3A taken along the section line B-B illustrated in Figure 3A. In the substrate illustrated in Figure 3, there are four planar electrical conductors: a first signal conductor represented by traces 306 and 308, a ground planar conductor 314, a power planar conductor 318, and a second signal planar conductor 322. The power planar conductor 318 is connected to a power terminal of an electrical power supply, and the ground planar conductor 314 is connected to a ground terminal of the power supply. Electronic devices are connected between power planar conductor 318
and ground planar conductor 314 to receive electrical power. The first signal planar conductor 306, 308 and the ground planar conductor 314 are separated by a first dielectric layer 302. Similarly, the ground planar conductor 314 and the power planar conductor 318 are separated by a second dielectric layer 316. Finally, the power planar conductor 318 and second signal plane 322 are separated by a third dielectric layer 320 from a bottom planar conductor 324. The substrate 300 may have more layers or less layers than what are illustrated in Figure 3 without affecting the operation of the invention. Similarly, additional insulating layers may be placed on top of traces 306 and 308.

In accordance with the principles of the invention, the electrical characteristics of a trace, such as traces 306 and 308, can be modified by selectively adding a thin layer of modification material either above or below the trace in question. The modification material could be anything with a dielectric and/or magnetic permeability constant different from the surrounding insulating layers. Such a material might be a dielectric material, a magnetic material or a combined material. In one embodiment, during the process of laminating the conductive and insulating layers, only the selected trace is covered with a layer of the modification material, thus the electrical properties of other traces will not be affected. The extra layer covering the selected parts of the selected traces may be an additive process during the lamination, after the etching is complete.

The thin layer of modification material on the trace may cover the entire length of the trace. Such coatings can be applied in varying thickness by conventional screen printing techniques such as those used to manufacture thin film capacitors and resistors. For example, in Figure 3A, modification material 304 covers the entire length of trace 306. Alternatively, the modification material can cover one or more parts of the trace, as the adjustment of the electrical properties requires. In Figure 3A, modification material sections 310 and 312 are shown covering parts of trace 308. Although rectangular areas of modification material are shown, other configurations, such as square, circular, or irregular shapes can also be used.

In one illustrative simulation, a printed circuit board with the construction illustrated in Figure 2 was simulated. This microstrip configuration used an insulating layer of FR4 material with a dielectric constant of 4.3. The height (h) of the layer was
5 mil. In such a configuration a 5 mil wide (w) one ounce copper trace produces a 145.71 picosecond per inch propagation delay. If, according to the principles of the present invention, the trace is entirely covered by a 2-mil thick layer of ceramic-filled epoxy with a dielectric constant of 20, the propagation delay increases to 192.1 picoseconds per inch, an increase of 31%. The characteristic impedance of the trace goes down by the same percentage.

In accordance with another embodiment of the invention, the electrical characteristics of a trace, such as traces 306 and 308, can be modified by selectively modifying the dielectric material in an insulating material either above or below the trace in question. Figures 4A and 4B represent a top view and a cross-sectional view of a portion of a multi-layered circuit board 400. In particular, Figure 4B is a cross-section of the board illustrated in Figure 4A taken along the section line B-B illustrated in Figure 4A. In the substrate illustrated in Figure 4, there are four planar electrical conductors: a first signal conductor represented by traces 406 and 408, a ground planar conductor 414, a power planar conductor 418, and a second signal planar conductor 422. The power planar conductor 418 is connected to a power terminal of an electrical power supply, and the ground planar conductor 414 is connected to a ground terminal of the power supply. Electronic devices are connected between power planar conductor 418 and ground planar conductor 414 to receive electrical power. The first signal planar conductor 406, 408 and the ground planar conductor 414 are separated by a first dielectric layer 402. Similarly, the ground planar conductor 414 and the power planar conductor 418 are separated by a second dielectric layer 416. Finally, the power planar conductor 418 and second signal plane 422 are separated by a third dielectric layer 420 from a bottom planar conductor 424. The substrate 400 may have more layers or less layers than what are illustrated in Figure 4 without affecting the operation of the invention. Similarly, additional insulating layers may be placed on top of traces 406 and 408.

In this embodiment, the insulating material in an insulating layer either above or below the selected trace is modified to change the dielectric constant in the vicinity of the selected trace. The modified insulating layer may extend along the entire length of the trace. For example, in Figure 4A, the insulating layer 402 has been modified in area 404 along the entire length of trace 406. Alternatively, the insulating layer can be
modified in the vicinity of one or more parts of the trace, as the adjustment of the
electrical properties requires. In Figure 4A, the insulating material has been modified
in sections 410 and 412 under parts of trace 408. The modification areas can be
rectangular as shown in area 404 or other configurations, such as circular, as shown
in areas 412 and 414. Other irregular shapes can also be used. In addition the
modification can extend entirely through the insulating layer as illustrated in 404 or
only part way through the layer as illustrated in 412.

The dielectric constant of the insulating material may be modified by
suspending particulates of a substance having a relatively high dielectric constant
(e.g., titanium dioxide or barium titanate) within a dielectric binder material (e.g., epoxy
resin polytetrafluoroethylene, or polystyrene). The dielectric constant of the
particulate-binder combination may be varied by changing the number of particulates
per unit volume of the particulate-binder combination. Increasing the number of
suspended particulates per unit volume of the particulate-binder combination
increases the dielectric constant of the particulate-binder combination. Decreasing the
number of suspended particulates per unit volume of the particulate-binder
combination decreases the dielectric constant of the particulate-binder combination.
In one embodiment, modified areas of insulating material are formed by inserting
materials with different dielectric constants into cutouts in the base material 402 in the
form of inlays. In another embodiment, the base material 402 is prepared with the
modified areas formed in place by varying the particulate-binder combination during
manufacture of the insulating material.

Another set of simulations were performed on a stripline circuit board
configuration. Such a configuration is similar to that sown in Figure 2 with the
exception that a second insulating layer is placed over trace 206 and a further planar
conductor is placed over the second insulating layer. In this latter simulation the
insulating layers were formed of FR4 material with a dielectric constant of 4.3. The
upper insulating layer had a height of 5 mil and the lower insulating layer had a height
of 12 mil. In such a structure a 4 mil wide one ounce copper trace has 175.52
picosecond per inch delay. If a 2 mil deep section of the second 12 mil insulating
layer is removed and replaced with an insulating material with a dielectric constant of
20, the same trace will have a 212.7 picosecond per inch delay, an increase of 20%.
Although exemplary embodiments of the invention have been disclosed, it will be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the spirit and scope of the invention. For example, it will be obvious to those reasonably skilled in the art that, although the description was directed to particular substrate configurations, other substrate configurations could be used in the same manner as that described. In addition, although only straight traces are illustrated, if the traces follow a piece-wise linear or curvilinear path, then the modified areas would conform to the path of the traces. Other aspects, such as the shapes of the modified areas other than those disclosed which achieve the same function, as well as other modifications to the inventive concept are intended to be covered by the appended claims.

What is claimed is:
CLAMNS

1. Apparatus for modifying electrical characteristics of a selected signal interconnect trace in a layered circuit board having a layer of insulating material separating the signal interconnect trace from a planar reference conductor, the insulating material having a first electrical characteristic and the apparatus comprising:
   at least one area formed of a second insulating material having a second electrical characteristic different from the first electrical characteristic and located only in the vicinity of the signal interconnect trace.

2. The apparatus as recited in claim 1 wherein the first electrical characteristic is a first dielectric constant.

3. The apparatus as recited in claim 2 wherein the second insulating material has a second dielectric constant different than the first dielectric constant.

4. The apparatus as recited in claim 1 wherein the first electrical characteristic is a first magnetic permeability.

5. The apparatus as recited in claim 4 wherein the second insulating material has a second magnetic permeability different from the first magnetic permeability.

6. The apparatus as recited in claim 1 wherein the second insulating material comprises a coating of modification material applied over the signal trace.

7. The apparatus as recited in claim 6 wherein the modification material has a electrical characteristic different from the first electrical characteristic.

8. The apparatus as recited in claim 1 wherein the second insulating material comprises a modified area of the insulating layer in the vicinity of the signal trace.
9. The apparatus as recited in claim 8 wherein the modified area comprises an inlay of third insulating material having an electrical characteristic different from the first electrical characteristic.

10. The apparatus as recited in claim 9 wherein the insulating material has a height and the inlay extends through the entire insulating layer height.

11. The apparatus as recited in claim 10 wherein the insulating layer has a height and the inlay extends part way through the height.

12. The apparatus as recited in claim 8 wherein the modified area comprises a material with a fourth dielectric constant suspended in an insulating material having a first dielectric constant to form a material with the second electrical characteristic.

13. The apparatus as recited in claim 12 wherein the insulating material has a height and the modified area extends through the entire insulating layer height.

14. The apparatus as recited in claim 12 wherein the insulating layer has a height and the modified area extends part way through the height.

15. A method for modifying electrical characteristics of a selected signal interconnect trace in a layered circuit board having a layer of insulating material separating the signal interconnect trace from a planar reference conductor, the insulating material having a first electrical characteristic and the method comprising:

(a) forming at least one area of a second insulating material having a second electrical characteristic different from the first electrical characteristic and located only in the vicinity of the signal interconnect trace.
16. The method as recited in claim 15 wherein the first electrical characteristic is a first dielectric constant.

17. The method as recited in claim 16 wherein the second insulating material has a second dielectric constant different than the first dielectric constant.

18. The method as recited in claim 15 wherein the first electrical characteristic is a first magnetic permeability.

19. The method as recited in claim 18 wherein the second insulating material has a second magnetic permeability different from the first magnetic permeability.

20. The method as recited in claim 15 wherein step (a) comprises applying a coating of modification material over the signal trace.

21. The method as recited in claim 20 wherein the modification material has a electrical characteristic different from the first electrical characteristic.

22. The method as recited in claim 15 wherein step (a) comprises (a1) modifying an area of the insulating layer in the vicinity of the signal trace.

23. The method as recited in claim 22 wherein step(a1) comprises inlaying an area of third insulating material having an electrical characteristic different from the first electrical characteristic.

24. The method as recited in claim 22 wherein the insulating material has a height and step (a1) comprises inlaying an area extending through the entire insulating layer height of third insulating material having an electrical characteristic different from the first electrical characteristic.

25. The method as recited in claim 22 wherein the insulating layer has a height and step (a1) comprises inlaying an area extending part way through the height of
third insulating material having an electrical characteristic different from the first electrical characteristic.

26. The method as recited in claim 22 wherein step (a) comprises:
   (a2) suspending a material with a fourth dielectric constant in an insulating material having a first dielectric constant to form a modified area with a material with the second electrical characteristic.

27. The method as recited in claim 26 wherein the insulating material has a height and the modified area extends through the entire insulating layer height.

28. The method as recited in claim 26 wherein the insulating layer has a height and the modified area extends part way through the height.
FIG. 1 PRIOR ART

FIG. 2A PRIOR ART

SUBSTITUTE SHEET (RULE 26)
FIG. 2B PRIOR ART
**FIG. 3A**

**FIG. 3B**

SUBSTITUTE SHEET (RULE 26)