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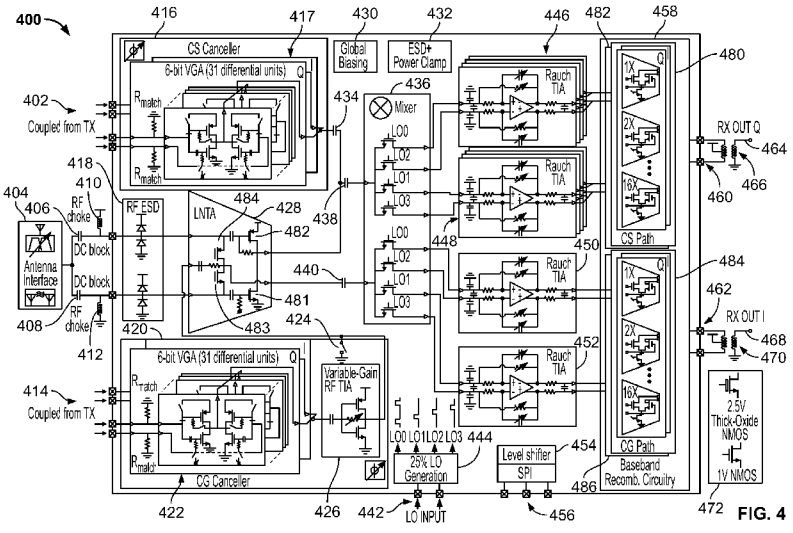


FIG. 4

(57) Abstract: Circuits for reducing out-of-band-modulated transmitter self-interference are provided. In some embodiments, receivers are provided, the receivers comprising: a low noise amplifier (LNA) having an input, a first output, and a second output, wherein the LNA includes: a common source transistor having a gate coupled to an input signal, a drain coupled to the first output of the LNA, and a source coupled to ground; and a common gate transistor having a gate coupled to a transmitter replica signal, a source coupled to the gate of the common source transistor, and a drain coupled to the second output of the LNA.

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CIRCUITS FOR REDUCING OUT-OF-BAND-MODULATED TRANSMITTER SELF-INTERFERENCE

Cross Reference to Related Application

[0001] This application claims the benefit of United States Provisional Patent Application No. 61/938,133, filed February 10, 2014, which is hereby incorporated by reference herein in its entirety.

Statement Regarding Government Funded Research

[0002] This invention was made with government support under contract HR0011-12-1-0006 awarded by Defense Advanced Research Projects Agency. The government has certain rights in the invention.

Background

[0003] A major trend in wireless communication systems is the investigation of radio-frequency (RF) transceivers that can be widely tuned across frequency bands. However, wideband receiver front-ends have to handle interference signals that are much larger than those in conventional narrowband receivers due to the lack of tunable high-front-end RF filters.

[0004] Out-of-band-modulated transmitter self-interference (or TX leakage) due to reduced antenna/duplexer isolation in many circuits imposes challenges, including cross-modulation, second-order inter-modulation and TX noise in the receiver (RX) band.

[0005] Accordingly, circuits for reducing out-of-band-modulated transmitter self-interference are desirable.

Summary

[0006] In accordance with some embodiments, circuits for reducing out-of-band-modulated transmitter self-interference are provided. In some embodiments, receivers are provided, the receivers comprising: a low noise amplifier (LNA) having an input, a first output, and a second output, wherein the LNA includes: a common source transistor having a gate coupled to an input signal, a drain coupled to the first output of the LNA, and a source coupled to ground; and a

common gate transistor having a gate coupled to a transmitter replica signal, a source coupled to the gate of the common source transistor, and a drain coupled to the second output of the LNA.

Brief Description of the Drawings

[0007] FIG. 1 is a block diagram of circuit for cancelling transmitter leakage in accordance with some embodiments of the disclosed subject matter.

[0008] FIG. 2 is a block diagram of circuit for cancelling transmitter leakage, showing a sub-circuit for mixing output signals with a local oscillator and filtering the mixed signals with a trans-impedance amplifier, in accordance with some embodiments of the disclosed subject matter.

[0009] FIG. 3 is a block diagram of a circuit for cancelling transmitter leakage include an injection of a transmitter replica signal in a common source path in accordance with some embodiments of the disclosed subject matter.

[0010] FIG. 4 is a schematic of receiver circuit that cancels transmitter leakage in accordance with some embodiments of the disclosed subject matter.

[0011] FIG. 5 is a schematic of a variable gain amplifier that can be used in a common gate canceller and/or a common source canceller in accordance with some embodiments of the disclosed subject matter.

Detailed Description

[0012] In accordance with some embodiments, circuits for reducing out-of-band-modulated transmitter self-interference are provided.

[0013] Turning to FIG. 1, an example 100 of a circuit for reducing out-of-band-modulated transmitter self-interference in accordance with some embodiments is illustrated. As shown, circuit 100, includes a common gate (CG) transistor 102, a common source (CS) transistor 104, a current source 106, a current source 108, a current source 110, an DC blocking capacitor 112, a resistor (R_S) 114 representing the source impedance looking back into the antenna interface, a variable phase rotator 116, a variable gain amplifier (VGA) 118, a replica input node 120, a signal input node 121, a positive output node 122, and a negative output node 124.

[0014] During operation of circuit 100, an input signal (I_S) coupled to signal input node 121 from signal source 132 drives the gate of CS transistor 104 via DC blocking capacitor 112 and

across source resistor (R_S) 114. The input signal may be provided from any suitable source, such as one or more antennas, in some embodiments. Based on the proximity, strength, and frequency of a signal from a separate transmitter circuit (not shown), a transmitter leakage current ($I_{TX-leakage}$) may also be induced at signal input node 121 as represented by transmitter leakage current source 130.

[0015] To counter this transmitter leakage current, a transmitter replica signal ($V_{TX-replica}$) from signal generator 134 can be applied to replica input node 120. The phase of the replica signal can then be rotated by variable phase rotator 116 and amplified or attenuated by VGA 118. The output of VGA 118 drives the gate of CG transistor 102. A canceller noise signal ($V_{n,canceller}$) is also present at the gate of CG transistor 102 as a result of noise from variable phase rotator 116 and VGA 118.

[0016] Using Kirchhoff's current law, the current at signal input node 121, when considering only the transmitter leakage current, can be represented as:

$$g_{m,CG}(A_{canceller}V_{TX-replica}-V_{in})=I_{TX-leakage}+(V_{in}/R_S)$$

where $g_{m,CG}$ is the trans-conductance of CG transistor 102 and $A_{canceller}$ is the voltage gain of the combination of phase rotator 116 and VGA 118. If the phase rotator and the VGA are adjusted so that $g_{m,CG}A_{canceller}V_{TX-replica}=I_{TX-leakage}$, then $V_{in}=0$, indicating the transmitter leakage voltage swing can be eliminated at the LNA input.

[0017] When transmitter leakage cancellation takes place, the source node of CG transistor 102 can be a virtual ground for the transmitter replica signal, and therefore the CG transistor is not degenerated by source resistor (R_S) 114 and any other resistance present at input node 121.

[0018] The noise from the combination of the phase rotator, the VGA, and the CG transistor, which, as stated above, can be represented by voltage source 136 ($V_{n,canceller}$) and current source 138 ($I_{n,CG}$), can be cancelled as a result of CS transistor 104 sensing this noise and presenting it at negative output terminal 124 (as represented by canceller noise 158 in FIG. 1) so that it matches (and thus cancels out) the corresponding noise presented at positive output terminal 122 (as represented by canceller noise 148 in FIG. 1).

[0019] Current sources 106 and 110 provide a DC biasing current for the CG transistor, and current source 108 provides a DC biasing current for the CS transistor.

[0020] While the transmitter leakage current ($I_{TX-leakage}$) is mostly cancelled at the input, a large leakage current still flows through CG transistor 102 producing a large voltage swing

($I_{TX\text{-}leakage}R_{CG}$) at the positive output node as represented by transmitter replica signal 142. To mitigate this, as shown in FIG. 2, a current-mode down conversion stage 202 with impedance transfer from baseband that includes passive mixers 206 and 218 and baseband trans-impedance amplifiers (TIAs) (formed from amplifier 214, capacitor 210, and resistor 212 and from amplifier 226, capacitor 222, and resistor 224) can be inserted before a combining network (not shown in FIG. 2) to be attached at output nodes 228 and 230 to filter out the large out-of-band leakage current before the achievement of voltage gain. As shown, passive mixers 206 and 218 combine the signals from nodes 122 and 124 with a local oscillator signal (LO) present at LO input nodes 204 and 216, respectively. As also shown, capacitors 208 and 220 may be present at the inputs of amplifiers 224 and 226, respectively, to block out-of-band signals.

[0021] In some embodiments, mixers 206 and 218 can be implemented using MOS transistor switches, as represented by the switch schematic symbol in the schematic mixer symbol in FIG. 2.

[0022] As shown by signals 140 and 150 in FIG. 1, residual transmitter leakage may be present at the gate of transistor 104 and negative output node 124 in some embodiments. This residual transmitter leakage may be the result of mismatches between the $V_{TX\text{-}replica}$ signal (and/or the product of it and the phase shift and/or amplification (or attenuation) provided by devices 116, 118, and/or 102).

[0023] As shown by signals 144 and 152, the desired signal (i.e., the signal resulting from the amplification of I_S from input source 132) may be presented differentially at positive output node 122 and the negative output node 124. Because these differential signals are 180 degrees out of phase, when combined into a single-ended signal, the single-ended signal will have double that of the two differential signals.

[0024] It should be note that reference numbers 130, 132, 134, 136, 138, 140, 142, 144, 146, 148, 150, 152, 156, and 158 do not represent actual components of circuit 100, but rather represent signals (e.g., a noise signal, modulation, leakage, etc.) and/or sources of those signals.

[0025] Turning to FIG. 3, an alternate view of the circuits of FIGS. 1 and 2 in accordance with some embodiments is shown. As illustrated, circuit 300 includes antenna(s) 302, a power amplifier 304, a coupler 306, DC blocking capacitors 308 and 310, a low noise amplifier 312 (comprising a current sources 314, 318, and 322, a common source (CS) transistor 316, and a common gate (CG) transistor 320), variable phase rotators 324 and 330, variable gain amplifiers

326 and 328, mixers 332 and 334, bypass capacitors 336 and 338, amplifiers 344 and 350, capacitors 340 and 346, resistors 342 and 348, variable trans-conductance amplifiers 352 and 354, and a differential amplifier 355.

[0026] Like with the circuits of FIGS. 1 and 2, in circuit 300, a desired receiver signal 360 may be received by antenna(s) 302. One or more continuous wave (CW) jammers 362 may also be received via the antenna(s) 302. As a result of coupling (represented by coupler 306) of a nearby transmitter signal from power amplifier 304, a transmitter leakage 364 and receiver-band transmitter noise 366 may also be present at antenna(s) 302.

[0027] A transmitter replica signal 370 can be provided to the gate of CG transistor 320 via variable phase rotator 330 and variable gain amplifier 328 (which can adjust the phase and the amplitude of the replica signal). As a result of this, the replica signal can then be presented at the gate of CS transistor 316 via DC blocking capacitors 308 and 310 from the source of CG transistor 320. By adjusting the phase and gain of rotator 330 and VGA 328, respectively, the replica signal can cancel out the transmitter leakage at the gate of CS transistor 316. As a result, as shown in 365, the signals at the gate of the CS transistor now include desired receiver signal 360, CW jammer(s) 362, transmitter noise 366, and cross modulation distortion 367 from CG transistor 320, but without transmitter leakage.

[0028] Similarly, as a result of transmitter replica signal 370 being injected at the gate of CG transistor 320, as shown in 376, desired receiver signal 360, CW jammer(s) 362, transmitter noise 366, cross modulation distortion 367, and transmitter replica signal 370 may appear at the input to mixer 334 from the drain of CG transistor 320. The cross-modulation distortion from the CG transistor also appears at the gate of the CS transistor, as mentioned above. To cancel the receiver-band transmitter noise, transmitter replica signal 368 can also be injected in to the CS path between the drain of CS transistor 316 and the input to mixer 332 via variable phase rotator 324 and VGA 326. As a result, desired receiver signal 360, CW jammer(s) 362, transmitter noise 366, cross modulation distortion 367, and transmitter replica signal 368 may appear in the CS path as shown at 374. As a result of filtering of the replica signals in the CS path and the CG path, at the output of variable transconductors 352 and 354, the signals in the paths may be as shown in 378 and 380, respectively. Following a combining of these signals by differential amplifier 355, transmitter noise 366 and cross modulation distortion 367 may be cancelled-out as shown by 382 at node 356.

[0029] Turning to FIG. 4, a detailed schematic of a receiver circuit 400 implemented on a chip in accordance with some embodiments is shown. As illustrated, circuit 400 includes a differential low noise trans-conductance amplifier (LNTA) 428. Like what is shown in FIGS. 1-3, this LNTA includes CS transistors 481 and 482 and CG transistors 483 and 484. A desired receiver signal is provided by antenna(s) 404 to the gates of transistors 481 and 482 connected to the inputs of the LNTA via DC blocking capacitors 406 and 408 and DC blocking capacitors in LNTA 428. RF chokes 410 and 412 may also be provided to minimize out-of-band signals at the inputs to the LNTA. RF ESD diodes 418 may be provided to protect the inputs of the LNTA from electrostatic discharge.

[0030] A transmitter replica signal is provided by CG canceller 420 to the gates of transistors 483 and 484 (via DC blocking capacitors in LNTA 428).

[0031] The drains of transistors 481 and 482 are connected and provide a CS output of the LNTA to mixer 436 via DC blocking capacitor 438. The drains of transistors 483 and 484 are connected and provide a CG output of the LNTA to mixer 436 via DC blocking capacitor 440. As with the CS output of circuit 100 of FIG. 3 (shown at the drain of CS transistor 316), a transmitter replica signal is injected at the CS output of LNTA 428 by CS canceller 416.

[0032] The CS output and the CG output of LNTA 428 are mixed by mixer 444 with local oscillator (LO) signals from local oscillator generator 444. Mixer 444 can be any suitable mixer in some embodiments. For example, mixer can be a four phase, current-driven mixer in some embodiments. In some embodiments, any suitable number of phases can be mixed by mixer 444 For example, eight phases can be mixed, instead of four, to provide a better noise figure, in some embodiments. As shown, when implemented with four phases, the LO generator can generate the LO signals as four 25% non-overlapping LO signals based on a reference LO signal received at LO inputs 442.

[0033] The outputs of mixer 436 can then be provided to second-order Rauch trans-impedance amplifiers (TIAs) 446, 448, 450, and 452. Large input shunt capacitors in the Rauch TIAs can be used to help sink out-of-band transmitter leakage current in the TIAs.

[0034] As illustrated, Rauch TIAs 446 and 448 may each be implemented as four TIAs (or any other suitable number of TIAs) while Rauch TIAs 450 and 452 may each be implemented as only one TIA (or any other suitable number of TIAs) to compensate for weighting of the CS transistors' trans-conductance (e.g., in this case 80 mS) to the CG transistors' trans-conductance

(e.g., in this case 20 mS). Rauch TIAs 446 and 450 can be used for the I channel, while Rauch TIAs 448 and 452 can be used for the Q channel.

[0035] The outputs from the Rauch TIAs can be provided to programmable recombination circuitry 458 to combine the receiver outputs from the CG output and the CS output for noise and cross-modulation distortion cancellation.

[0036] As shown circuity 458 can include four sub-circuits 480, 482, 484, and 486. Sub-circuit 480 is connected to the outputs of Rauch TIA 446, sub-circuit 482 is connected to the outputs of Rauch TIA 448, sub-circuit 484 is connected to the outputs of Rauch TIA 450, and sub-circuit 486 is connected to the outputs of Rauch TIA 452. Within each of these sub-circuits, there is sub-sub-circuit for the I channel and the Q channel. Within each of these sub-sub-circuits, five (or any other suitable number) binary weighted selectable transconductors can be provided to weight the output of the corresponding Rauch TIA in a corresponding one the output 464 and 468. For example, for Rauch TIA 446, one or more of the transconductors labelled 1x, 2x, 4x, 8x, and 16 in the I channel in sub-sub-circuit 480 can be selected and the selected transconductors can determine the contribution of Rauch TIA 446 to output 468. Likewise, as another example, for Rauch TIA 446, one or more of the transconductors labelled 1x, 2x, 4x, 8x, and 16 in the Q channel in sub-sub-circuit 480 can be selected and the selected transconductors can determine the contribution of Rauch TIA 446 to output 464.

[0037] The outputs of the Q sub-sub-circuits of circuitry 458 can be connected to outputs 460, which combine together via transformer 466 to provide Q receiver output 464. Similarly, the outputs of the I sub-circuits of circuitry 458 can be connected to outputs 462, which combine together via transformer 470 to provide I receiver output 468.

[0038] Global biasing circuitry 430 may be provided, as known in the art, to generate biasing circuits in circuit 400 in accordance with some embodiments.

[0039] ESD and power clamp circuitry 432 may be provided, as known in the art, to protect circuit 400 from electrostatic discharge and over-voltage conditions in accordance with some embodiments.

[0040] Level shifter, series-to-parallel-interface SPI circuitry 454 may be provided to program the entire receiver through a single series interface in accordance with some embodiments. Series control signal may be connected to inputs 456 in accordance with some embodiments.

[0041] As shown by legend 472 in FIG. 4, in some embodiments, some devices of circuit 400 can be implemented in 2.5V thick oxide NMOS (e.g., to handle large transmitter leakage) and some devices of circuit 400 can be implemented in 1V NMOS. In some embodiments, the devices can be implemented in any other suitable technologies. In some embodiments, circuit 400 can be implemented in 65 nm CMOS or any other suitable technology.

[0042] In accordance with some embodiments, CG canceller 420 and CS canceller 416 each can include a Cartesian phase rotator 422 and 417, respectively, which each includes two (one for I and one for Q) 6-bit variable-gain trans-conductance amplifiers (VGAs). For the CG canceller, an RF variable-gain TIA (VG-TIA) 426 can be inserted between LNTA CG transistors 483 and 484 and phase rotator 422 for gain variation and current-to-voltage conversion in some embodiments. Note that, in some embodiments, in the Cartesian phase rotators, the magnitude of the output current can also be modified through the VGAs at the expense of phase resolution. The phase-rotator VGAs can be built using inverter-based trans-conductance cells for high linearity in some embodiments.

[0043] Turning to FIG. 5, an example 500 of a VGA circuit that can be used in CG canceller 420 and CS canceller 416 in accordance with some embodiments is illustrated. As shown, circuit 500 receives input signals at nodes 500 and 538. The input signals are provided to the gates of transistors 514 and 518 and transistors 522 and 524, respectively. The drains of transistors 514, 518, 522, and 524 are all connected to output node 520. A bias voltage is provided to nodes 512 and 534.

[0044] Under the control of a switch (SW) signal and a switch-bar (SWb) signal, switches 5084, 510, 516, 524, 532, and 536 control the gain of the amplifier formed by these components.

[0045] Any suitable devices may be used to implement the transistors, the switches, and the resistors (i.e., resistors 506, 508, 528, and 530) of circuit 500 in some embodiments.

[0046] The provision of the examples described herein (as well as clauses phrased as "such as," "e.g.," "including," and the like) should not be interpreted as limiting the claimed subject matter to the specific examples; rather, the examples are intended to illustrate only some of many possible aspects.

[0047] Although the invention has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and the numerous changes in the details of implementation of the invention can be

made without departing from the spirit and scope of the invention, which is only limited by the claims which follow. Features of the disclosed embodiments can be combined and rearranged in various ways.

What is claimed is:

1. A receiver comprising:

a low noise amplifier (LNA) having an input, a first output, and a second output, wherein the LNA includes:

a common source transistor having a gate coupled to an input signal, a drain coupled to the first output of the LNA, and a source coupled to ground; and

a common gate transistor having a gate coupled to a transmitter replica signal, a source coupled to the gate of the common source transistor, and a drain coupled to the second output of the LNA.

2. The receiver of claim 1, further comprising a variable-gain amplifier coupled to the gate of the common gate transistor that amplifies the transmitter replica signal.

3. The receiver of claim 1, further comprising a variable -gain radio frequency trans-impedance amplifier coupled to the gate of the common gate transistor that amplifies the transmitter replica signal.

4. The receiver of claim 1, further comprising a phase rotator coupled to the gate of the common gate transistor that adjusts the phase of the transmitter replica signal.

5. The receiver of claim 1, further comprising a variable-gain amplifier coupled to the drain of the common source transistor that amplifies the transmitter replica signal.

6. The receiver of claim 1, further comprising a multi-phase mixer that has a first input and a second input, that mixes the first output of the LNA and the second output of the LNA each with a different phase of a multi-phase local oscillator signal, and that provides a plurality of outputs.

7. The receiver of claim 6, further comprising a plurality of Rauch trans-impedance amplifiers (TIAs) each having an input and an output, wherein:

the input of each of a first at least one of the plurality of Rauch TIAs is coupled to at least one of the plurality of outputs of the multi-phase mixer; and

the input of each of a second at least one of the plurality of Rauch TIAs is coupled to at least another of the plurality of outputs of the multi-phase mixer.

8. The receiver of claim 7, further comprising:

a first plurality of selectable transconductance amplifiers, each with a different weighting, coupled to the output of each of the first at least one of the plurality of Rauch TIAs; and

a second plurality of selectable transconductance amplifiers, each with a different weighting, coupled to the output of each of the second at least one of the plurality of Rauch TIAs.

9. The receiver of claim 6, wherein each different phase of the multi-phase local oscillator signal is equally shifted in phase.

10. The receiver of claim 1, wherein the transmitter leakage is cancelled at the gate of the common source transistor.

11. The receiver of claim 1, wherein a desired signal is out-of-phase at the first output and the second output of the LNA.

12. The receiver of claim 1, further comprising:

a variable-gain amplifier coupled to the gate of the common gate transistor that amplifies the transmitter replica signal;

a variable -gain radio frequency trans-impedance amplifier coupled to the gate of the common gate transistor that amplifies the transmitter replica signal; and

a phase rotator coupled to the gate of the common gate transistor that adjusts the phase of the transmitter replica signal,

wherein noise produced in the common gate transistor, the variable-gain amplifier, the variable-gain radio frequency trans-impedance amplifier, and the phase rotator is in-phase at the first output and the second output of the LNA.

13. The receiver of claim 1, wherein cross-modulation distortion produced in the common gate transistor is in-phase at the first output and the second output of the LNA.

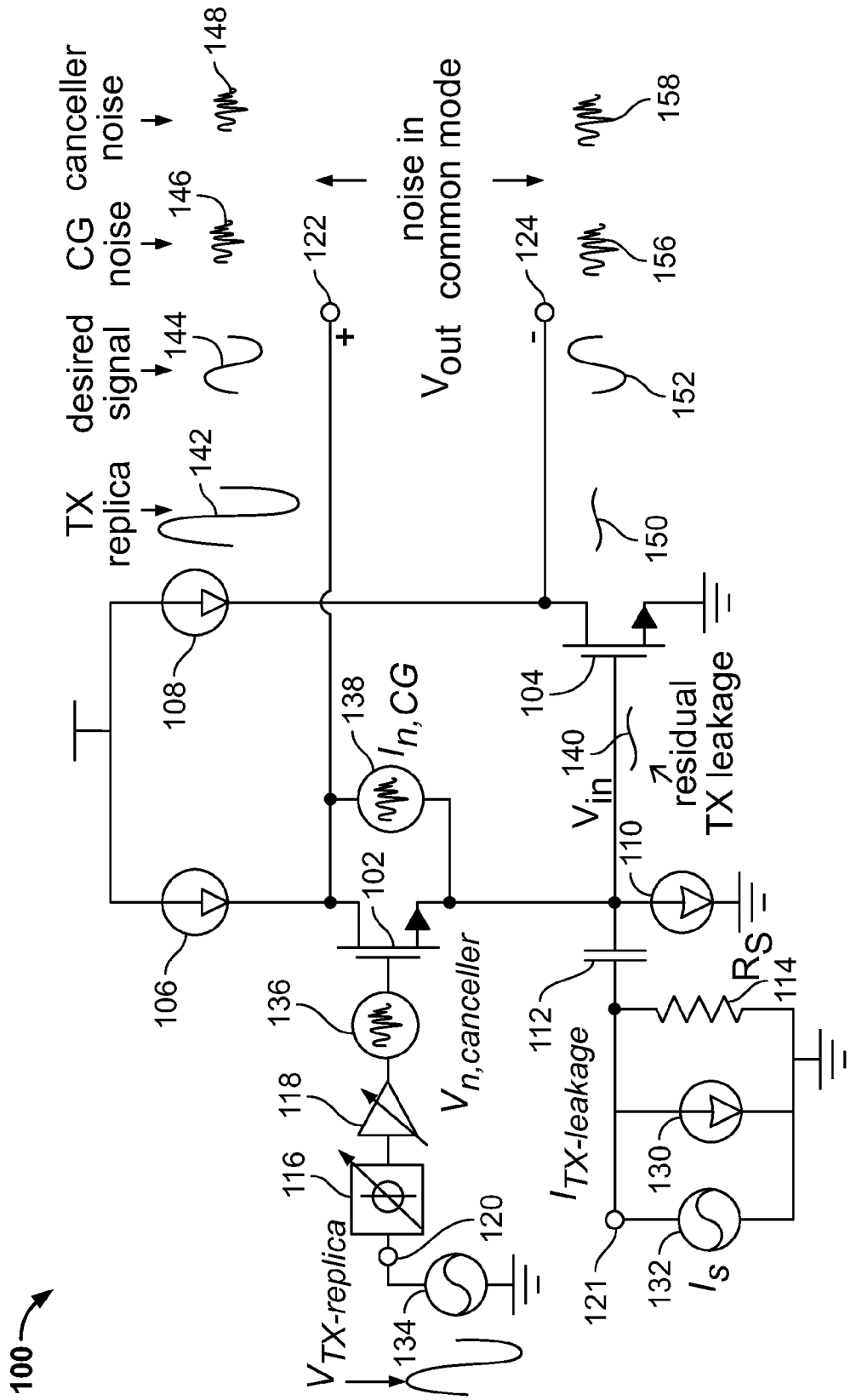

100
TX replica
desired signal
CG canceller noise
noise
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142
122
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noise in
V_{out} common mode
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138
$I_{n,CG}$
$V_{n,canceller}$
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118
116
120
$V_{TX\text{-}replica}$
134
V_{in}
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residual
TX leakage
112
$I_{TX\text{-}leakage}$
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I_S
R_S
114

FIG. 1

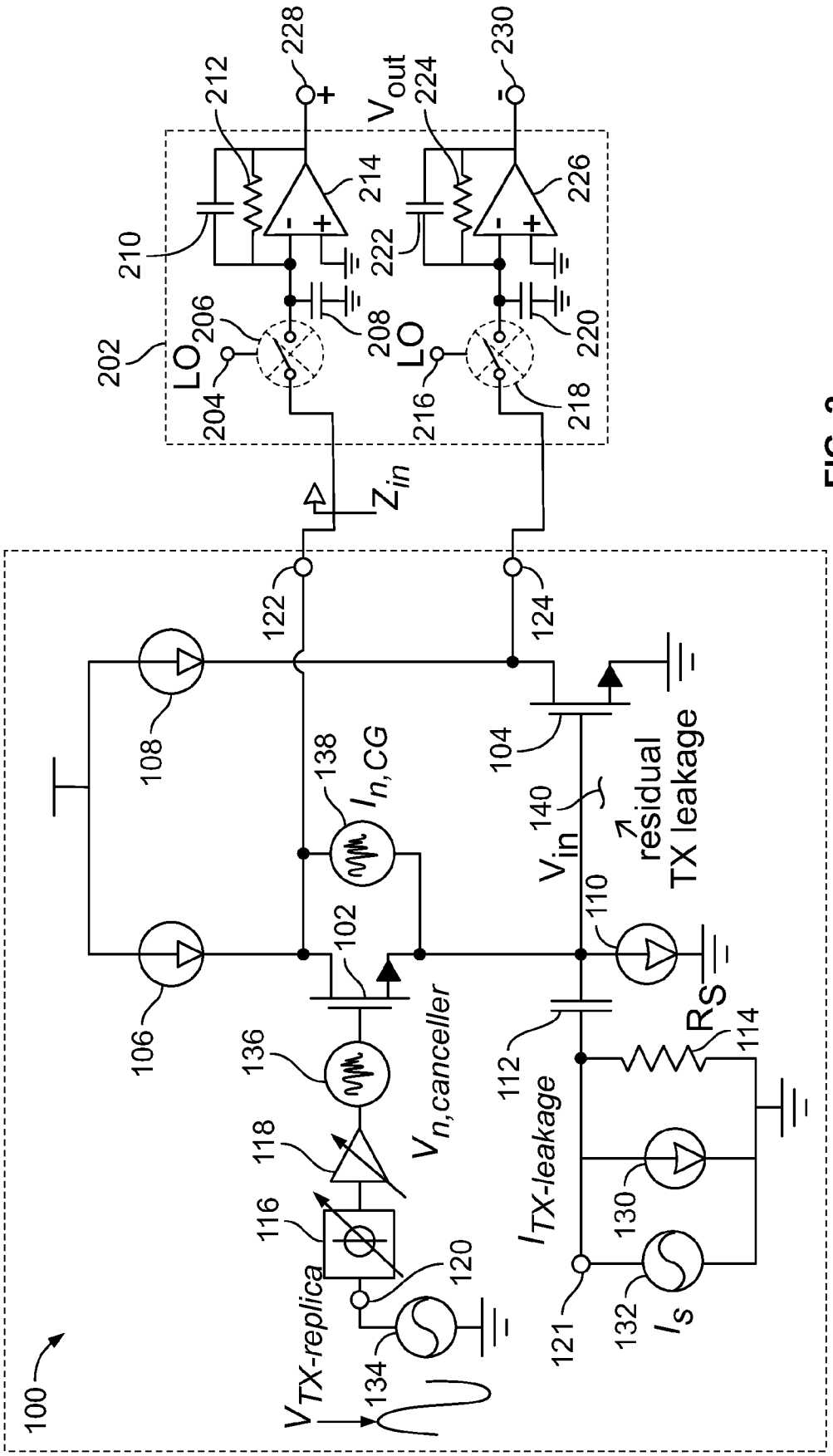

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214
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LO
LO
V_{out}
Z_{in}
$I_{n,CG}$
$V_{n,canceller}$
$V_{TX\text{-}replica}$
$I_{TX\text{-}leakage}$
V_{in}
residual
TX leakage
R_S
I_S

FIG. 2

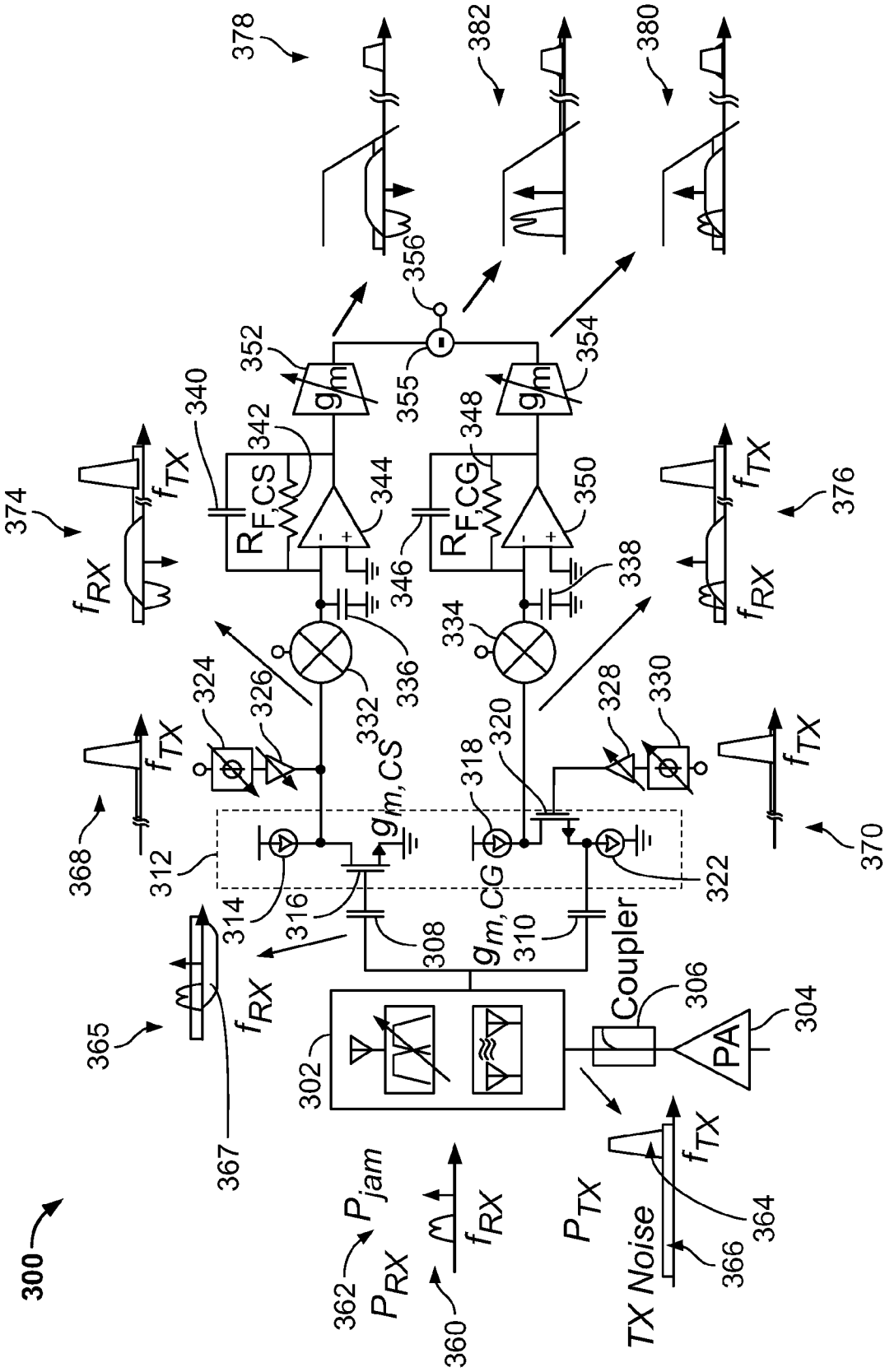

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362
360
364
366
367
368
370
374
376
378
380
382
365
PA
Coupler
P_{jam}
P_{RX}
P_{TX}
TX Noise
f_{RX}
f_{TX}
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$g_{m,CG}$
$R_{F,CS}$
$R_{F,CG}$
gm

FIG. 3

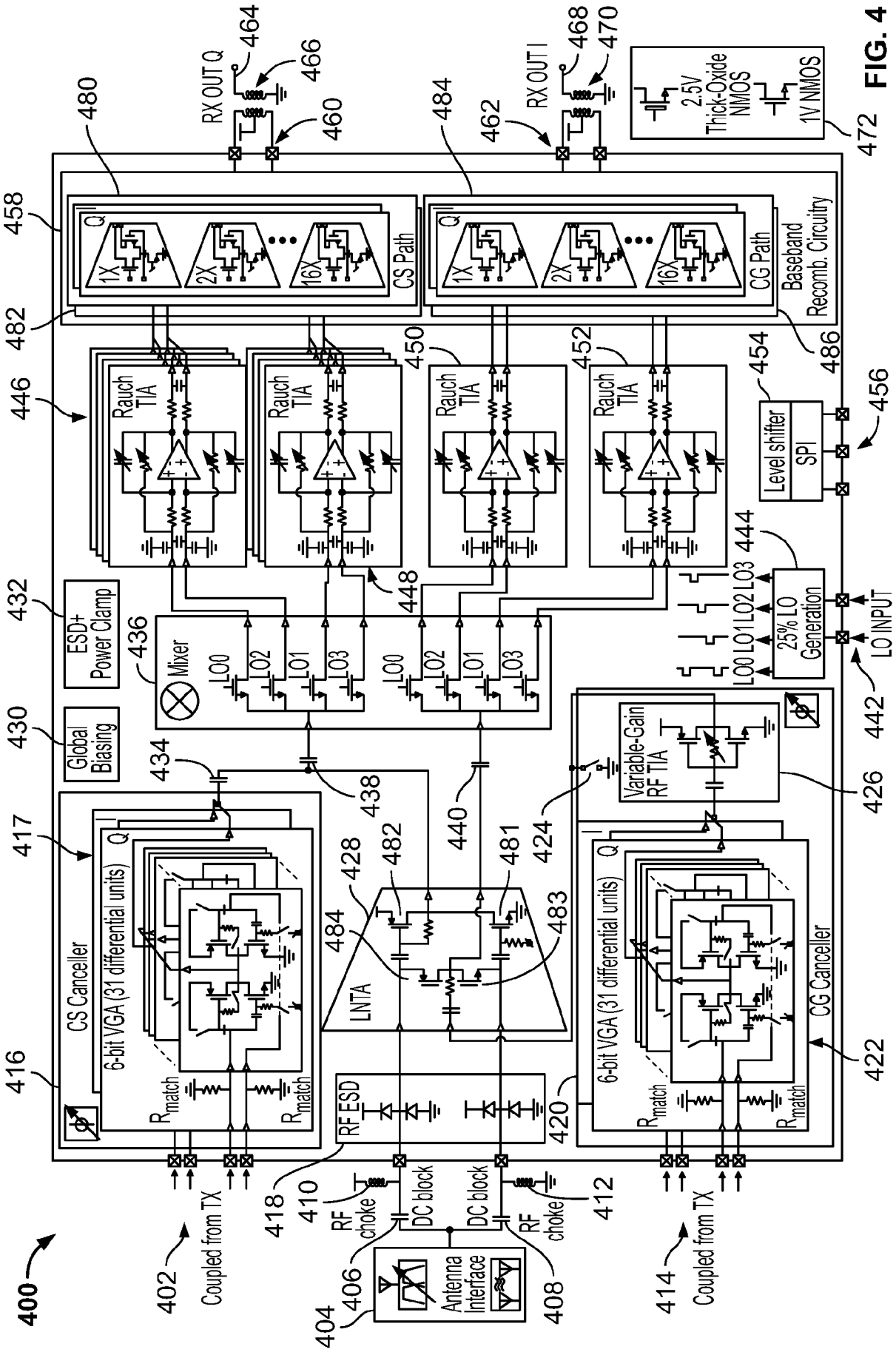

400
402
Coupled from TX
404
406
Antenna Interface
408
RF choke
410
DC block
412
DC block
414
Coupled from TX
416
CS Canceller
6-bit VGA (31 differential units)
I
Q
Rmatch
417
418
RF ESD
420
CG Canceller
422
424
Variable-Gain RF TIA
426
428
LNTA
430
Global Biasing
432
ESD+ Power Clamp
434
436
Mixer
LO0
LO2
LO1
LO3
438
440
442
LO INPUT
444
25% LO Generation
LO0 LO1 LO2 LO3
446
Rauch TIA
448
450
452
454
Level shifter
SPI
456
458
CS Path
1X
2X
16X
CG Path
Baseband Recomb. Circuitry
460
RX OUT Q
462
RX OUT I
464
466
468
470
2.5V Thick-Oxide NMOS
1V NMOS
472
480
481
482
483
484
486

FIG. 4

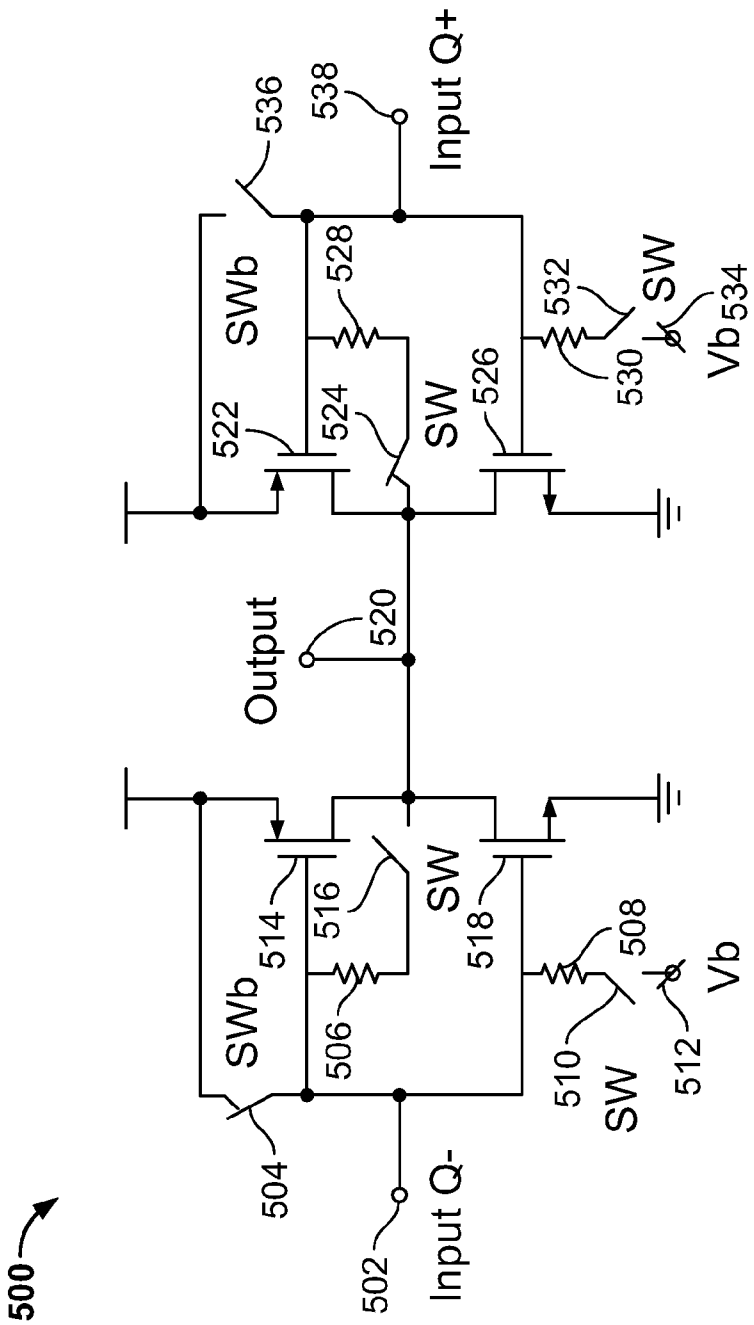

500
502
Input Q-
504
SWb
506
508
510
SW
512
Vb
514
516
SW
518
520
Output
522
524
SW
526
528
530
532
SW
534
Vb
536
538
Input Q+

FIG. 5