United States Patent

[11] 3,617,712

[72] Inventor **Hitoshi Sone**
Chigasaki-shi, Japan

[21] Appl. No. **723,028**
[22] Filed **Apr. 22, 1968**
[45] Patented **Nov. 2, 1971**

[73] Assignee **Kabushiki Kaisha Ricoh**
Tokyo, Japan

[32] Priority **Apr. 24, 1967**
[33] **Japan**
[31] **42/25856**

---

[54] **NUMERICAL DISPLAYING APPARATUS**
2 Claims, 3 Drawing Figs.

[52] **U.S. Cl.** ..... **235/92 EA,** 340/378
[51] **Int. Cl.** **G09f 9/00**
[50] **Field of Search** 235/92; 340/378, 336

[56] **References Cited**

UNITED STATES PATENTS

2,690,303	9/1954	Nolde et al.	235/92
2,649,502	8/1953	Odell	235/92
3,161,867	12/1964	Isborn	235/92
3,204,234	8/1965	Nakauchi	235/92
3,267,262	8/1966	Stuart	235/92
3,400,388	9/1968	Blank	235/92

Primary Examiner—Daryl W. Cook
Assistant Examiner—Joseph M. Thesz, Jr.
Attorney—Burgess, Ryan & Hicks

ABSTRACT: Binary counters FF1, FF2, FF3, and FF4, which are used in a decimal notation displaying device (L), respectively indicate a numeral which corresponds to 1, 2, 4, and 8. A decimal notation number in the aforesaid displaying device is illustrated as a sum of displays which correspond to the aforesaid 1, 2, 4, and 8 respectively.

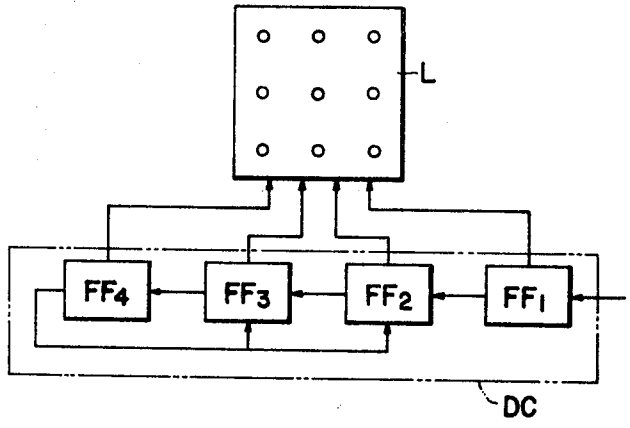


FIG. 1

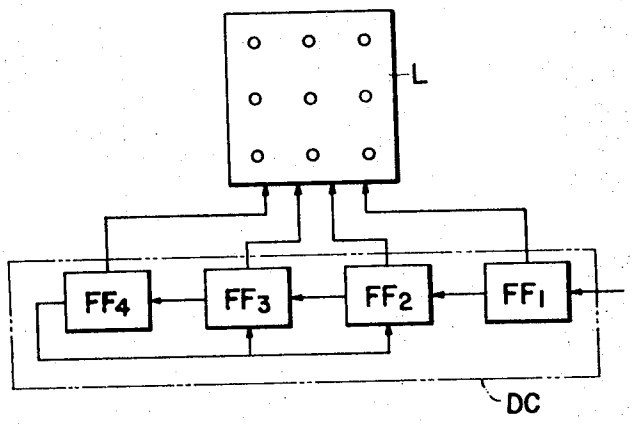
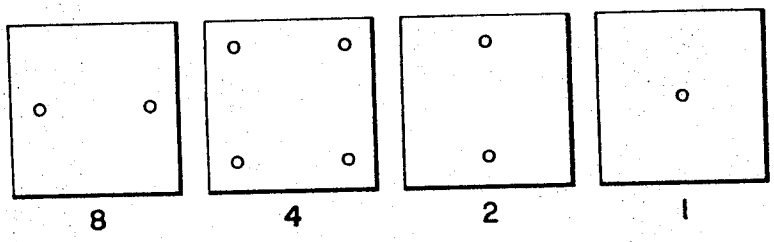


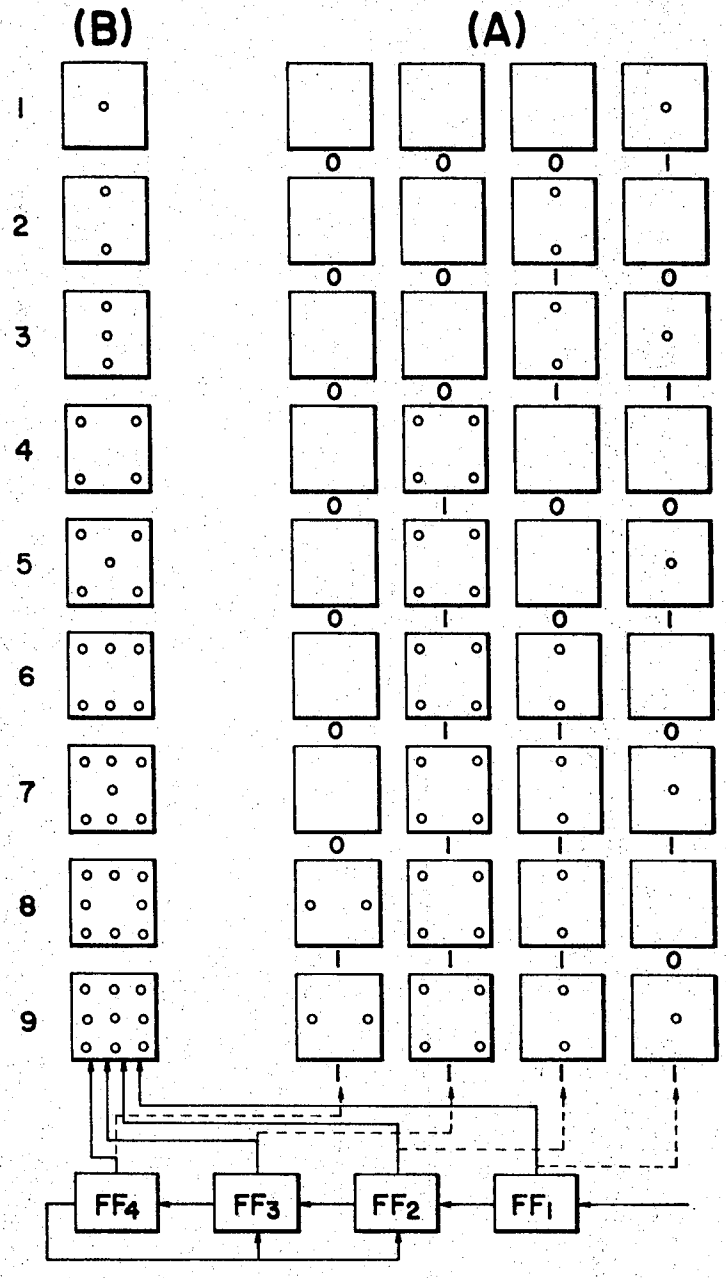
FIG. 2



INVENTOR
HITOSHI SONE

BY Burgess, Ryan & Hicks
ATTORNEYS

FIG. 3



INVENTOR

HITOSHI SONE

BY Burgess, Ryan & Hicks

ATTORNEYS

NUMERICAL DISPLAYING APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to a numerical displaying apparatus. For more details, the invention relates to a numerical displaying apparatus which calculates a decimal notation number using a combination of binary counters.

Conventionally, a decimal notation number is mainly displayed by converting binary notation numbers using binary-decimal converters. According to this conventional method, the Arabic numerals such as 0, 1, 2, ...8, and 9 can be used to illustrate the number, however, the method requires a binary-decimal converter and various component to drive the indicating lamp, and therefore inevitably expensive.

SUMMARY OF THE INVENTION

In accordance with the present invention, in a decimal notation counter consists of binary counters which resolve the input number into numerals 1, 2, 4, and 8, and output of the counter corresponding to these numbers perform the display. The input decimal number is read out as a sum of the indications.

One object of the invention is to considerably simplify structure of the displaying apparatus.

One more object of this invention is to reduce cost of the apparatus.

The invention will be well understood from the following description and the accompanying drawings illustrating an embodiment of the invention.

BRIEF EXPLANATION OF DRAWINGS

FIG. 1 shows configuration of the displaying apparatus.

FIG. 2 shows indication of numerals by each stage of the binary counter in the decimal notation counter.

FIG. 3 shows illustration of the input number upon a combination of the binary counters in FIG. 2.

DESCRIPTION OF A PREFERRED EMBODIMENT

In FIG. 1, DC is a decimal notation counter consisting of a combination of binary counters. Each binary counter consists of a flip-flop FF1, FF2, FF3, and FF4. Output of each counter, or flip-flop, is connected to the decimal notation displaying device L, and display thereof is performed by nine lamps, for example, arranged in columns and rows. The lamps are lit by the binary counter outputs.

When the first stage binary counter is in the condition "1," a lamp in the center is lit, as seen in FIG. 2(1), and when the second stage binary counter is in the condition "1," two lamps in the upper and lower center are lit as in FIG. 2(2). When the third binary counter is in the condition "1," four lamps in corners are lit as in FIG. 2(4), and when the fourth stage binary counter is in the condition "1," two lamps in the right and left side center are lit as in FIG. 2(8). No lamp lights when each binary is in the condition "0."

FIG. 3 shows the indication which corresponds to each input numeral, in figures (A) the lamps which are lit by binary counters in each numeral input are shown, and figures (B) show consequent illustration (display) of input numerals by combination of the lit lamps.

Assuming that the counters are counting a numeral 1 in decimal notation which is referred to as 0001 in binary notation, a lamp in the center lights, and, when the input numeral is 2 (0010), two lamps in upper and lower center light. If the input numeral is 3 (0011), both lamps which indicate 1 and 2, respectively, are lit, thereby indicating the input number with lighting three lamps on the vertical centerline.

Accordingly, input numerals 4 (0100), 5 (0101), 6 (0110), and 7 (0111) are respectively indicated by combination of

lamps lit by each counter, making total number of lamps as 4, 5, 6, and 7.

The decimal notation counter shown in the embodiment comprises a feedback circuit to the second and the third stage in order to convert a hexadecimal notation counting into a decimal notation, and subsequently, numerals 8 and 9 are counted as 1110 and 1111 respectively, thereby indicating them with eight and nine lamps.

However, as no lamp lights when the counted numeral is 0, the indication can not be distinguished from a condition under which the counter is not operating. An adequate method, such as to facilitate a lamp which indicate a condition 0 at a proper portion on the frame of the displaying device, can enable the aforesaid identification.

As previously described, according to this invention, outputs of each binary counter indicate numerals such as 1, 2, 4, and 8, respectively, and a combination thereof directly displays a sum of the indications of these numbers, in other words, a decimal notation number which is counted by binary notation counters is displayed in a decimal notation number.

The invention claimed is:

1. A numerical display apparatus for counting pulses and displaying the result in a decimal format on a visual matrix display, said apparatus comprising;

at least first, second, third and fourth binary counters interconnected to provide at least 10 successive stable states for successively counting said pulses, and

a decimal notation display means operatively connected directly to said interconnected counters for directly displaying the binary states of said counters in a decimal format on a visual matrix display, said display means comprising;

first means for producing a first portion of said visual matrix display corresponding to a stable state of said first counter;

second means for producing a second portion of said visual matrix display corresponding to a stable state of said second counter;

third means for producing a third portion of said visual matrix display corresponding to a stable state of said third counter;

fourth means for producing a fourth portion of said visual matrix display corresponding to a stable state of said fourth counter;

said first, second, third and fourth means being simultaneously operable to produce a composite visual matrix display corresponding to any one of the said successive stable states of said interconnected counters;

an output from said fourth binary counter being fed back to an input of said second and of said third binary counters thereby eliminating 6 of the total possible 16 stable states of said interconnected counters;

said first means comprising a single light source connected to an output of said first counter and corresponding to a decimal 1 notation;

said second means comprising two light sources connected to an output of said second counter and corresponding to a decimal 2 notation;

said third means comprising four light sources connected to an output of said third counter and corresponding to a decimal 4 notation; and

said fourth means comprising two light sources connected to an output of said fourth counter and, in combination with said second and third means, corresponding to a decimal 8 notation.

2. An apparatus as in claim 1 wherein the nine said light sources are arranged in a square matrix to indicate in a composite matrix light display said stable states of said interconnected counters.

* * * * *