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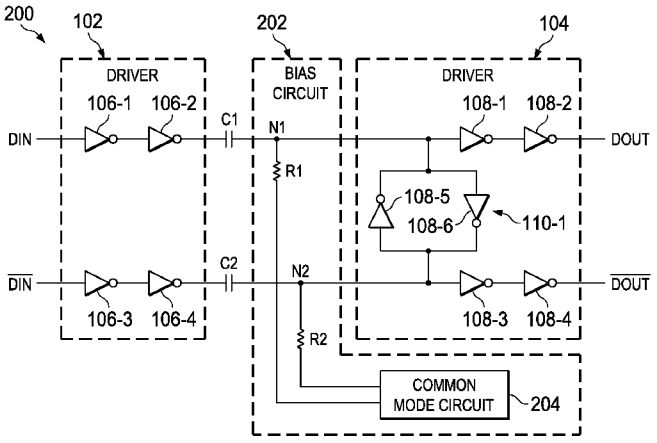


FIG. 4

(57) Abstract: A level shifter (200) is provided. This level sifter includes a first driver (102), a second driver (104), a capacitor (C1, C2), a bias circuit (202) and a common mode circuit (204). The first driver has a first signal path that is coupled between an input terminal and an output terminal, and the first driver operates in a first voltage domain. The second driver operates in a second voltage domain and includes a second signal path and latch (110-1). The second signal path is coupled between an input terminal and an output terminal of the second driver, and the latch is coupled to the input terminal of the second signal path. The capacitor is coupled between the output terminal of the first signal path and the input terminal of the second signal path, and the bias circuit (202) is coupled to the input terminal of the second signal path and operates in the second voltage domain.

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# LEVEL SHIFTER

**[0001]** This relates generally to level shifting and, more particularly, to a level shifter with low jitter.

## BACKGROUND

**[0002]** FIG. 1 shows a conventional level shifter 100. Level shifter 100 is generally comprised of drivers 102 and 104 (which operate in different voltage domains) with capacitors C1 and C2 (which should be sufficiently large so as to have a sufficiently low cut-off frequency) coupled therebetween. For higher voltage applications, capacitors C1 and C2 can be replaced with capacitor strings. Typically, each of drivers 102 and 104 has a pair of signal or data paths (which are generally comprised of inverters 106-1 to 106-4 and 108-1 to 108-4) so as to be able to generate differential signal DOUT/ $\overline{DOUT}$ from differential signal DIN/ $\overline{DIN}$. Latch 110 (which is coupled between the signals paths of driver 104 and which are generally comprised of inverters 108-5 and 108-6) is also included to drive the signal to rail.

**[0003]** A problem with this arrangement, however, is that, as switching occurs, capacitors C1 and C2 are repeatedly charged and discharged. As a result, the voltage on the capacitors C1 and C2 varies, distorting the signal DIN/ $\overline{DIN}$ as it traverses the level shifter 100 (as shown in FIG. 2). Additionally, jitter is introduced, which distorts the eye-opening pattern (as shown in FIG. 3). Thus, there is a need to compensate for distortion in level shifters.

**[0004]** Some other examples of conventional systems are described in U.S. Patent Publ. No. 2006/0091907; Rajapandian et al., "High-voltage power delivery through charge recycling," IEEE J. of Solid-State Circuits, Vol. 41, No. 6, pp. 1400-1410, June 2006; and Breussegem et al., "Monolithic capactivie DC-DC Converter with Single Boundary-Multiphase Control and Voltage Domain Stacking in 90 nm CMOS," IEEE J. of Solid-State Circuits, Vol. 46, No. 7, pp. 1715-1727, July 2011.

SUMMARY

**[0005]** An embodiment provides an apparatus. The apparatus comprises a first driver having a first signal path with an input terminal and an output terminal, wherein the first driver operates in a first voltage domain, and wherein the input terminal of the first signal path receives an input signal; a second driver that operates in a second voltage domain, wherein the second driver has: a second signal path with an input terminal and an output terminal; and a latch that is coupled to the input terminal of the second signal path; a capacitor that is coupled between the output terminal of the first signal path and the input terminal of the second signal path; and a bias circuit that is coupled to the input terminal of the second signal path and that operates in the second voltage domain.

**[0006]** In an embodiment, the second signal path further comprises a plurality of inverters coupled in series with one another in a sequence between the input and output terminals of the second signal path.

**[0007]** In an embodiment, the capacitor further comprises a first capacitor, and wherein the bias circuit further comprises: a resistor that is coupled to the input terminal of the second signal path; a second capacitor; and a common mode inverter that is coupled between the second capacitor and the resistor.

**[0008]** In an embodiment, the common mode inverter is a replica of the first inverter of the sequence.

**[0009]** In an embodiment, the input signal is differential, and wherein the first driver further comprises a third signal path with an input terminal and an output terminal.

**[0010]** In an embodiment , the resistor further comprises a first resistor, and wherein the second driver further comprises a fourth signal path with an input terminal and an output terminal, and wherein the latch and a second resistor are coupled to the input terminal of the fourth signal path, and wherein the apparatus further comprises a third capacitor that is coupled between the output terminal of the third signal path and the input terminal of the fourth signal path.

**[0011]** In an embodiment, the first and second resistors are coupled together.

**[0012]** In an embodiment, the common mode inverter further comprises a first common mode inverter, and wherein the bias circuit further comprises: a fourth capacitor; and a second common mode inverter that is coupled between the second fourth and the second resistor.

**[0013]** In an embodiment, the first and second resistors are adjustable.

**[0014]** In an embodiment, an apparatus is provided. The apparatus comprises a first driver that operates in a first voltage domain, wherein the first driver has: a first input terminal; a first output terminal; and a first set of inverters coupled in series with one another between the first input terminal and the first output terminal; a second driver that operates in a second voltage domain, wherein the second driver has: a second input terminal; a second output terminal; a second set of inverters coupled in series with one another between the second input terminal and the second output terminal; and a latch that is coupled to the second input terminal; a capacitor that is coupled between the first output terminal and the second input terminal; and a bias circuit that is coupled to the second input terminal and that operates in the second voltage domain.

**[0015]** In an embodiment, the second set of inverters are coupled in series with one another in a sequence, and wherein the capacitor further comprises a first capacitor, and wherein the common mode circuit further comprises: a resistor that is coupled to the second input terminal; a second capacitor; and a common mode inverter that is coupled between the second capacitor and the resistor.

**[0016]** In an embodiment, the common mode inverter is a replica of the first inverter of the sequence.

**[0017]** In an embodiment, the first driver further comprises: a third input terminal; a third output terminal; and a third set of inverters coupled in series with one another between the third input terminal and the third output terminal.

**[0018]** In an embodiment, the resistor further comprises a first resistor, and wherein the bias circuit further comprises second resistor, and wherein the second driver further comprises: a fourth input terminal; a fourth output terminal that is coupled to the latch and the second resistor; and a fourth set of inverters coupled in series with one another between the fourth input terminal and the fourth output terminal.

**[0019]** In an embodiment, the apparatus further comprises a third capacitor that is coupled between the third output terminal and the fourth input terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** FIG. 1 is a diagram of an example of a conventional level shifter;

**[0021]** FIG. 2 is a diagram depicting the transient response for the level shifter of FIG. 1;

**[0022]** FIG. 3 is a diagram depicting an eye-opening for the level shifter of FIG. 1;

**[0023]** FIG. 4 is a diagram of an example of a level shifter in accordance with an embodiment of the present invention;

**[0024]** FIGS. 5 and 8 are diagrams of examples of the bias circuit of FIG. 4;

**[0025]** FIG. 6 is a diagram comparing the transient responses for the level shifters of FIGS. 1 and 4; and

**[0026]** FIG. 7 is a diagram depicting an eye-opening for the level shifter of FIG. 4.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0027]** FIG. 4 illustrates an example of a level shifter 200 in embodying principles of the invention. As shown, the level shifter 200 is similar in construction to level shifter 100, except that level shifter 200 includes a bias circuit 202. This bias circuit 202 (which operates in the same voltage domain as driver 104) generally includes resistors R1 and R2 that are coupled to the signal paths of driver 104, and a common mode circuit 204. The common mode circuit 204 generates common mode voltage(s) that can be used to substantially maintain the voltages on capacitors C1 and C2. Each of inverters 106-1 to 106-4, 108-1 to 108-6, and 204 are also comprised of a PMOS transistor and an NMOS transistor, and resistors R1 and R2 can have generally the same value or resistance. Additionally, as shown, level shifter 200 is differential, but level shifter 200 can also be used with a single-ended signal (where the data paths that include inverters 106-3, 106-4, 108-3 and 108-4 and capacitor C2 are omitted).

**[0028]** In FIG. 5, a more detailed example of the bias circuit 202 (labeled 202-A for FIG. 5) can be seen. As shown, the resistors R1 and R2 are coupled together to form a divider between the signals paths of driver 104, and the common mode circuit 204-A generally includes a common mode inverter 204 and capacitor C3. Typically, the inverters 108-1 to 108-4 are matched (meaning that transistors of the same sizes are employed), and common mode inverter 204 (which generally operates in the same voltage domain as driver 104) is typically a replica of inverter 108-1 (meaning that the transistors of 204 are scaled in comparison to inverter 108-1). Being a replica, the current used by inverter 204 is lower.

**[0029]** As mentioned above, using this bias circuit 202-A, the voltages on the capacitors C1 and C2 can be generally maintained; this is usually accomplished by forming additional current paths with the bias circuit 202-A during switching. As an example, it can be assumed that the voltage on node N1 transitions to logic low and the voltage on node N2 transitions to logic high. When the voltage at node N2 becomes sufficiently large, the voltage on node N1

becomes sufficiently small, and neither has railed, the NMOS transistor for inverter 108-5 and the PMOS transistor for inverter 108-6 enter into a linear region. At this point, the common mode circuit 202 forms a current path that limits the amplitude (A) of the of the voltage swing to:

(1) $$VSS + IR_{ONNMOS} \leq A \leq VDD - IR_{ONPMOS},$$

where VDD and VSS are the rail voltages for the domain of the driver 104 and bias circuit 202-A. A current path would also be formed similarly for a transition in the opposite direction. Additionally, the PMOS and NMOS transistors for inverters 108-5 and 108-6 along with the resistors R1 and R2 should also be sized such that the PMOS and NMOS transistors for inverters 108-5 and 108-6 do not enter a deep linear region (i.e., drain-source voltage $V_{DS}$ is less than about 50mV). As a result of employing the bias circuit 202-A, the amplitude of the voltage swing seen by capacitors C1 and C2 is small, meaning that the voltage on capacitors C1 and C2 is substantially maintained. Thus, signal integrity is improved where signal distortion is reduced (as shown in FIG. 6) and where jitter is reduced (as shown in FIG. 7).

**[0030]** Bias circuit 202-A also includes switches S1 to S5 to allow the bias circuit 202-A and level shifter 200 to be deactivated. Switches S1 to S5 are usually controlled by an enable signal such that switches S1, S2, and S4 are closed when the enable signal is logic high or "1" and switches S3 and S5 are closed when the enable signal is logic low or "0." By having this arrangement, switch S5 drives the common mode voltage to ground, and switch S3 drives node N2 to ground, allowing the latch (inverters 108-5 and 108-6) to drive node N1 to rail VDD. Thus, when deactivated, there is little to no quiescent current in level shifter 200.

**[0031]** Turning to FIG. 8, another example of the bias circuit 202 (labeled 202-B for FIG. 8) can be seen. Similar to bias circuit 202-A, bias circuit 202-B includes resistors R3 and R4 and switches S1 to S3, but common mode circuit 204-B generates bias voltages BIAS1 and BIAS2 for each of resistors R3 and R4, respectively, from bias generators 208-1 and 208-2. These bias generators 208-1 and 208-2 use common mode inverters 210-1 and 210-2 (which are replicas of inverters 108-1 and 108-3, respectively, and which operate in a similar manner to inverter 206) and capacitors C4-1 and C4-2 (which operate in a similar manner to capacitor C3) to generate these bias voltages BIAS1 and BIAS2. Additionally, the resistors R3 and R4 are adjustable (which can, for example, be a switched resistor array) so as to "tune" the common mode voltage to compensate for variances in the data paths of driver 104. Bias generators 208-1 and 208-2

also include switches S6-1, S6-2, S7-1, and S7-2 that operate in a similar manner to switches S4 and S5 to lower the quiescent current in driver 200.

**[0032]** Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first driver having a first signal path with an input terminal and an output terminal, wherein the first driver operates in a first voltage domain, and wherein the input terminal of the first signal path receives an input signal;

a second driver that operates in a second voltage domain, wherein the second driver has:

a second signal path with an input terminal and an output terminal; and

a latch that is coupled to the input terminal of the second signal path;

a capacitor that is coupled between the output terminal of the first signal path and the input terminal of the second signal path; and

a bias circuit that is coupled to the input terminal of the second signal path and that operates in the second voltage domain.

2. The apparatus of Claim 1, wherein the second signal path further comprises a plurality of inverters coupled in series with one another in a sequence between the input and output terminals of the second signal path.

3. The apparatus of Claim 2, wherein the capacitor further comprises a first capacitor, and wherein the bias circuit further comprises:

a resistor that is coupled to the input terminal of the second signal path;

a second capacitor; and

a common mode inverter that is coupled between the second capacitor and the resistor.

4. The apparatus of Claim 3, wherein the common mode inverter is a replica of the first inverter of the sequence.

5. The apparatus of Claim 4, wherein the input signal is differential, and wherein the first driver further comprises a third signal path with an input terminal and an output terminal.

6. The apparatus of Claim 5, wherein the resistor further comprises a first resistor, and wherein the second driver further comprises a fourth signal path with an input terminal and an output terminal, and wherein the latch and a second resistor are coupled to the input terminal of the fourth signal path, and wherein the apparatus further comprises a third capacitor that is coupled between the output terminal of the third signal path and the input terminal of the fourth signal path.

7. The apparatus of Claim 6, wherein the first and second resistors are coupled together.

8. The apparatus of Claim 6, wherein the common mode inverter further comprises a first common mode inverter, and wherein the bias circuit further comprises:

a fourth capacitor; and

a second common mode inverter that is coupled between the second fourth and the second resistor.

9. The apparatus of Claim 8, wherein the first and second resistors are adjustable.

10. An apparatus comprising:

a first driver that operates in a first voltage domain, wherein the first driver has:

a first input terminal;

a first output terminal; and

a first set of inverters coupled in series with one another between the first input terminal and the first output terminal;

a second driver that operates in a second voltage domain, wherein the second driver has:

a second input terminal;

a second output terminal;

a second set of inverters coupled in series with one another between the second input terminal and the second output terminal; and

a latch that is coupled to the second input terminal;

a capacitor that is coupled between the first output terminal and the second input terminal; and

a bias circuit that is coupled to the second input terminal and that operates in the second voltage domain.

11. The apparatus of Claim 10, wherein the second set of inverters are coupled in series with one another in a sequence, and wherein the capacitor further comprises a first capacitor, and wherein the bias circuit further comprises:

a resistor that is coupled to the second input terminal;

a second capacitor; and

a common mode inverter that is coupled between the second capacitor and the resistor.

12. The apparatus of Claim 11, wherein the common mode inverter is a replica of the first inverter of the sequence.

13. The apparatus of Claim 12, wherein the first driver further comprises:

a third input terminal;

a third output terminal; and

a third set of inverters coupled in series with one another between the third input terminal and the third output terminal.

14. The apparatus of Claim 13, wherein the resistor further comprises a first resistor, and wherein the bias circuit further comprises second resistor, and wherein the second driver further comprises:

a fourth input terminal;

a fourth output terminal that is coupled to the latch and the second resistor; and

a fourth set of inverters coupled in series with one another between the fourth input terminal and the fourth output terminal.

15. The apparatus of Claim 14, wherein the apparatus further comprises a third capacitor that is coupled between the third output terminal and the fourth input terminal.

16. The apparatus of Claim 15, wherein the first and second resistors are coupled together.

17. The apparatus of Claim 15, wherein the common mode inverter further comprises a first common mode inverter, and wherein the bias circuit further comprises:

a fourth capacitor; and

a second common mode inverter that is coupled between the fourth capacitor and the second resistor.

18. The apparatus of Claim 17, wherein the first and second resistors are adjustable.

FIG. 1
(PRIOR ART)

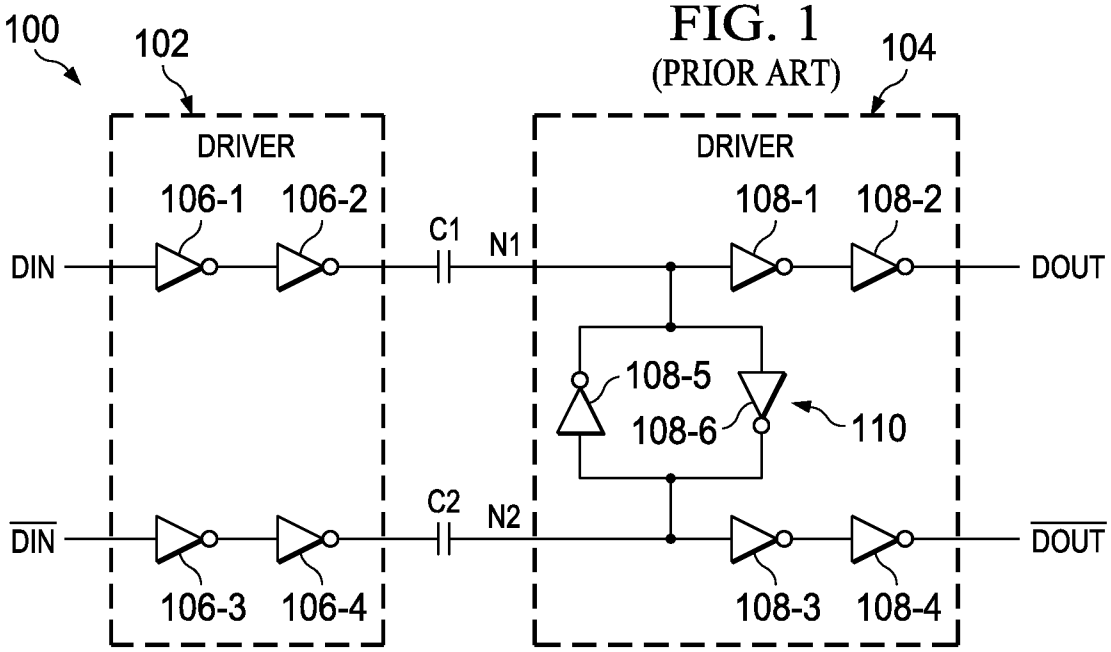



FIG. 3
(PRIOR ART)

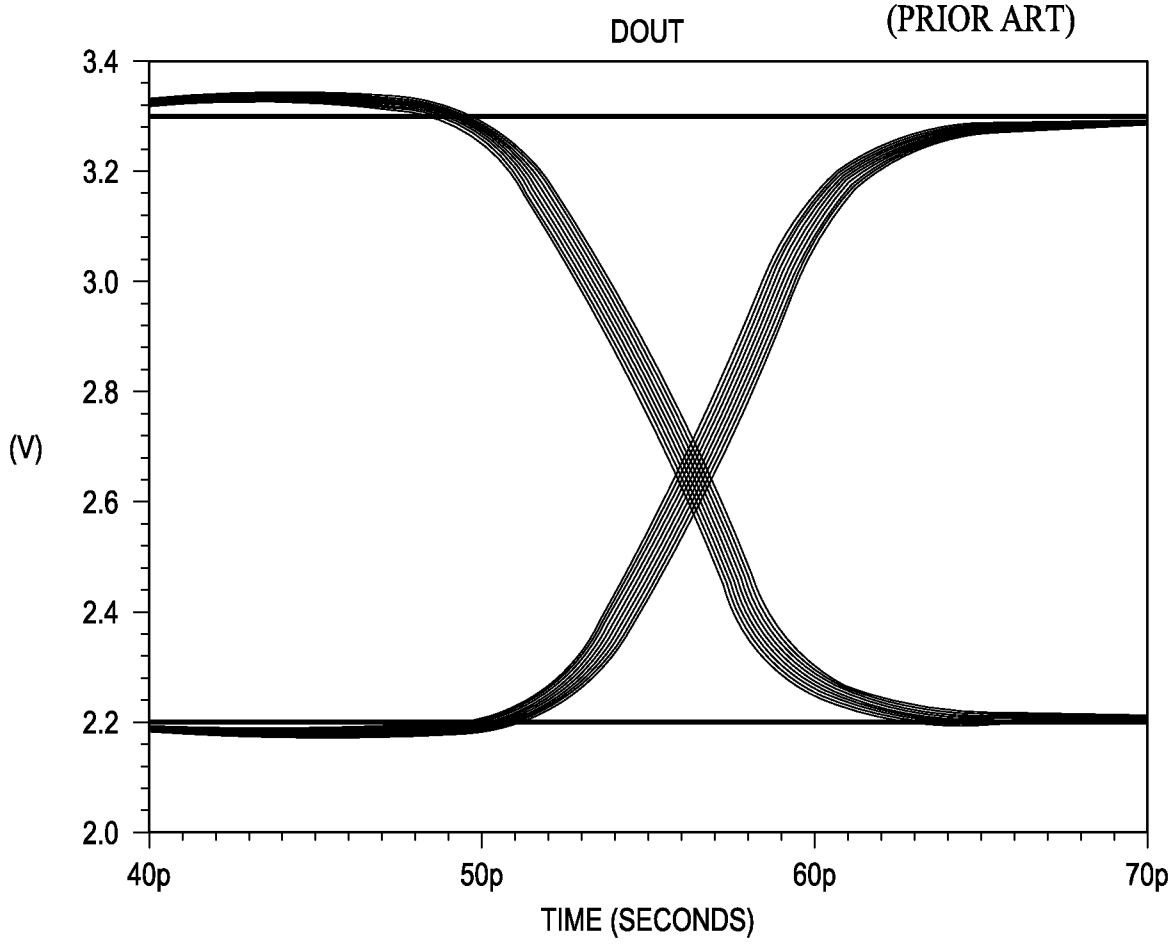
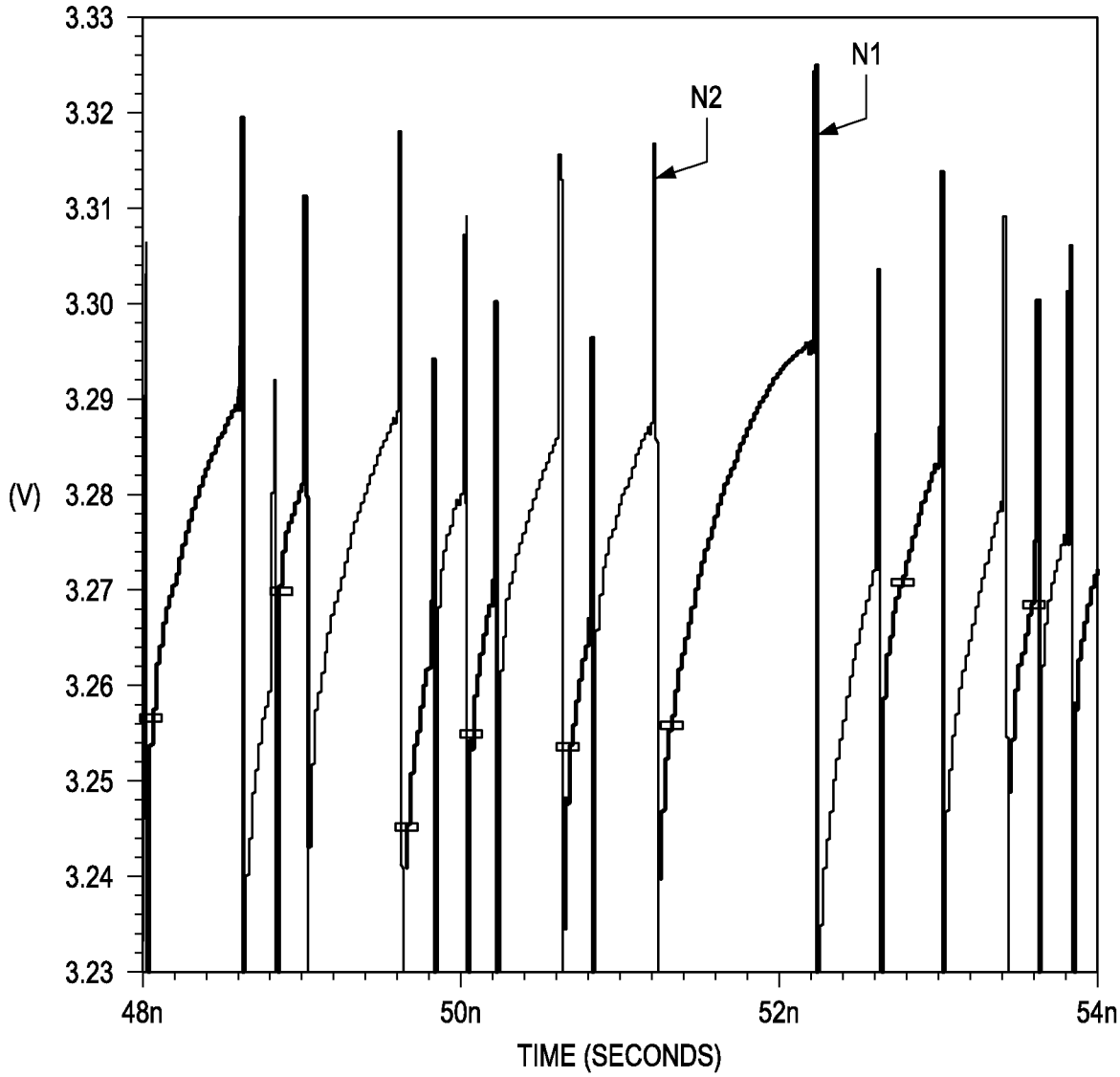


FIG. 2
(PRIOR ART)



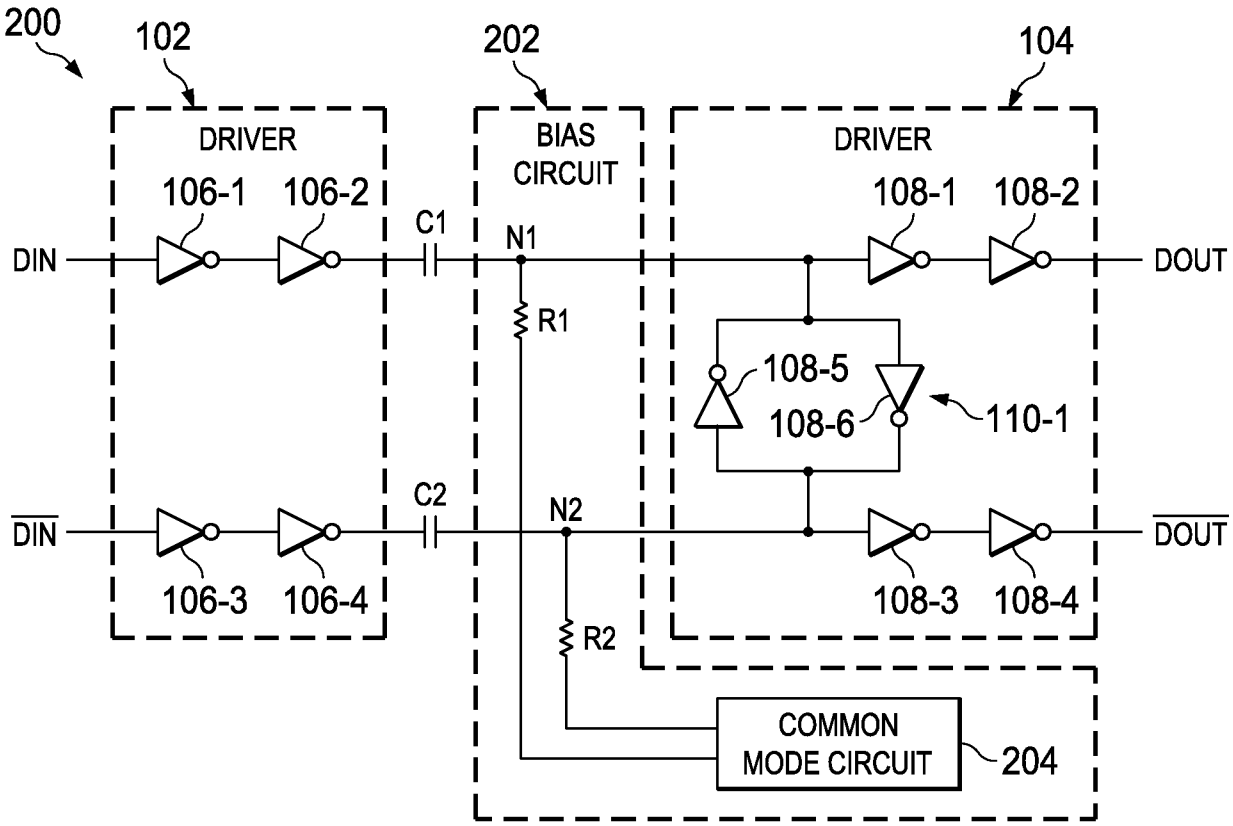

200
102
202
104
DRIVER
BIAS CIRCUIT
DRIVER
106-1
106-2
108-1
108-2
C1
N1
DIN
DOUT
R1
108-5
108-6
110-1
C2
N2
DIN
DOUT
106-3
106-4
108-3
108-4
R2
COMMON MODE CIRCUIT
204

FIG. 4

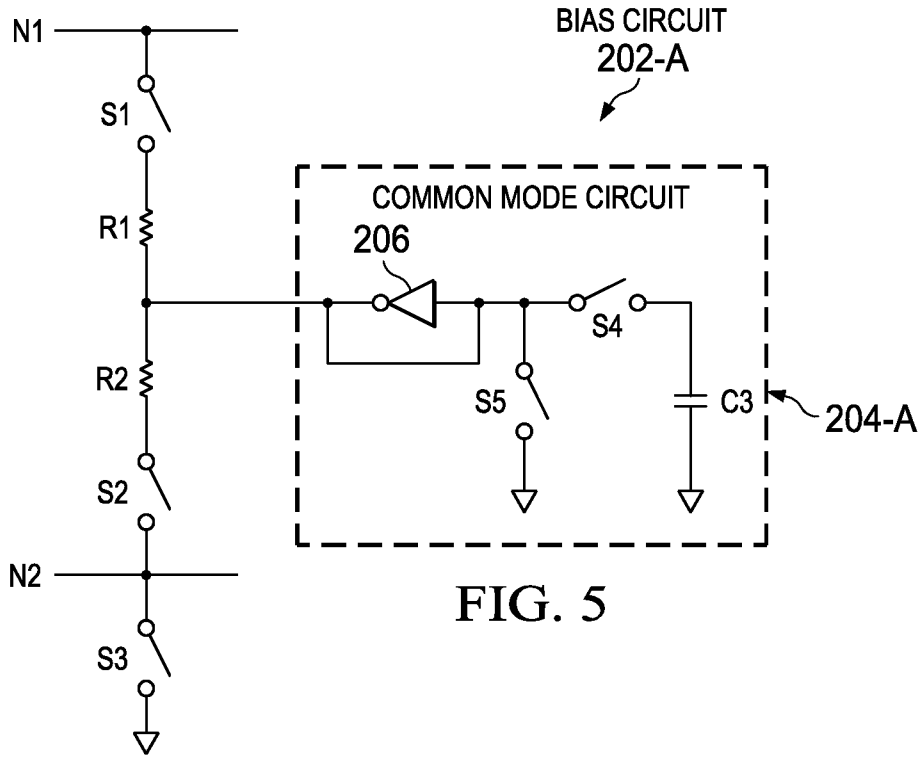

N1
BIAS CIRCUIT
202-A
S1
COMMON MODE CIRCUIT
R1
206
S4
R2
S5
C3
204-A
S2
N2
S3

FIG. 5

FIG. 6

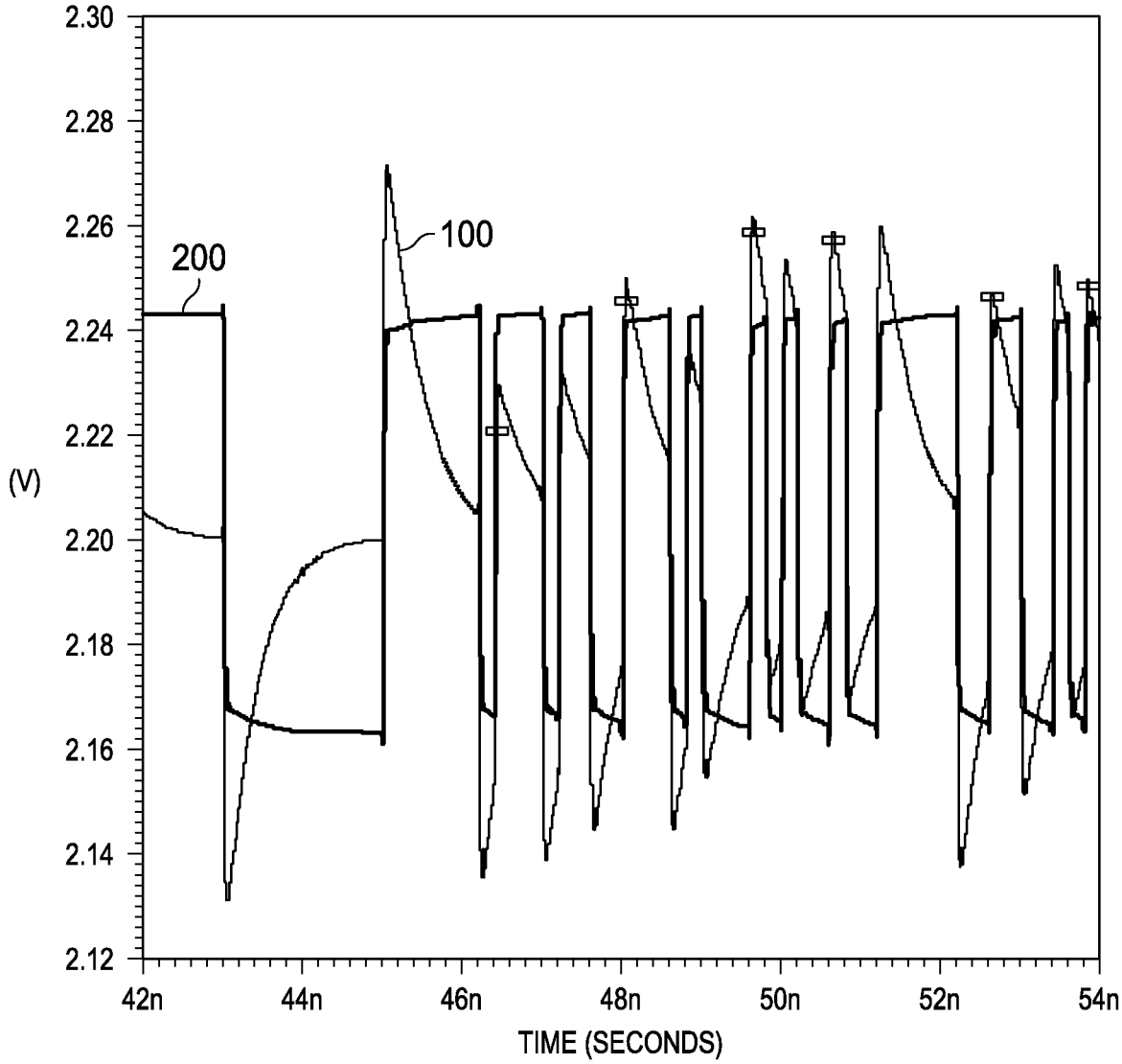

2.30
2.28
2.26
2.24
2.22
2.20
2.18
2.16
2.14
2.12
(V)
200
100
42n
44n
46n
48n
50n
52n
54n
TIME (SECONDS)

FIG. 7

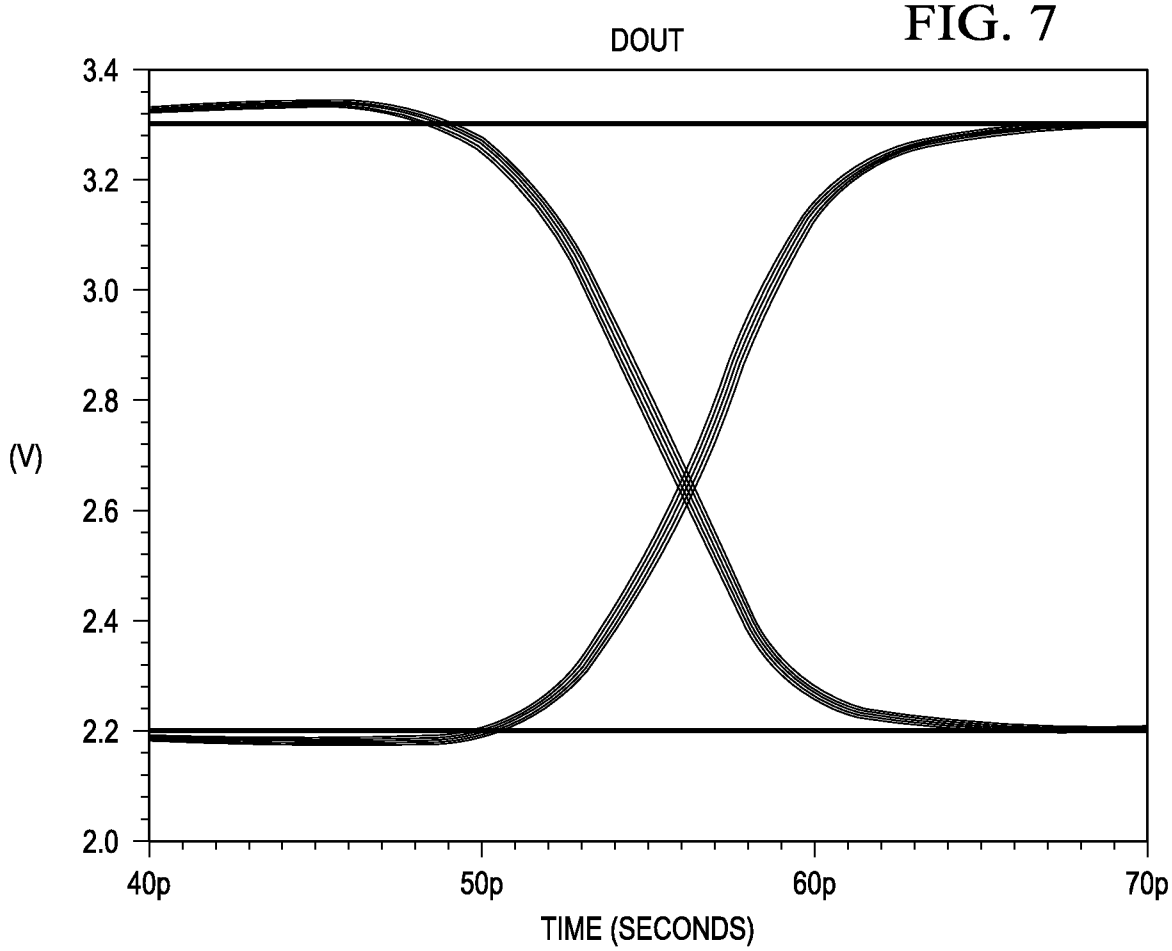
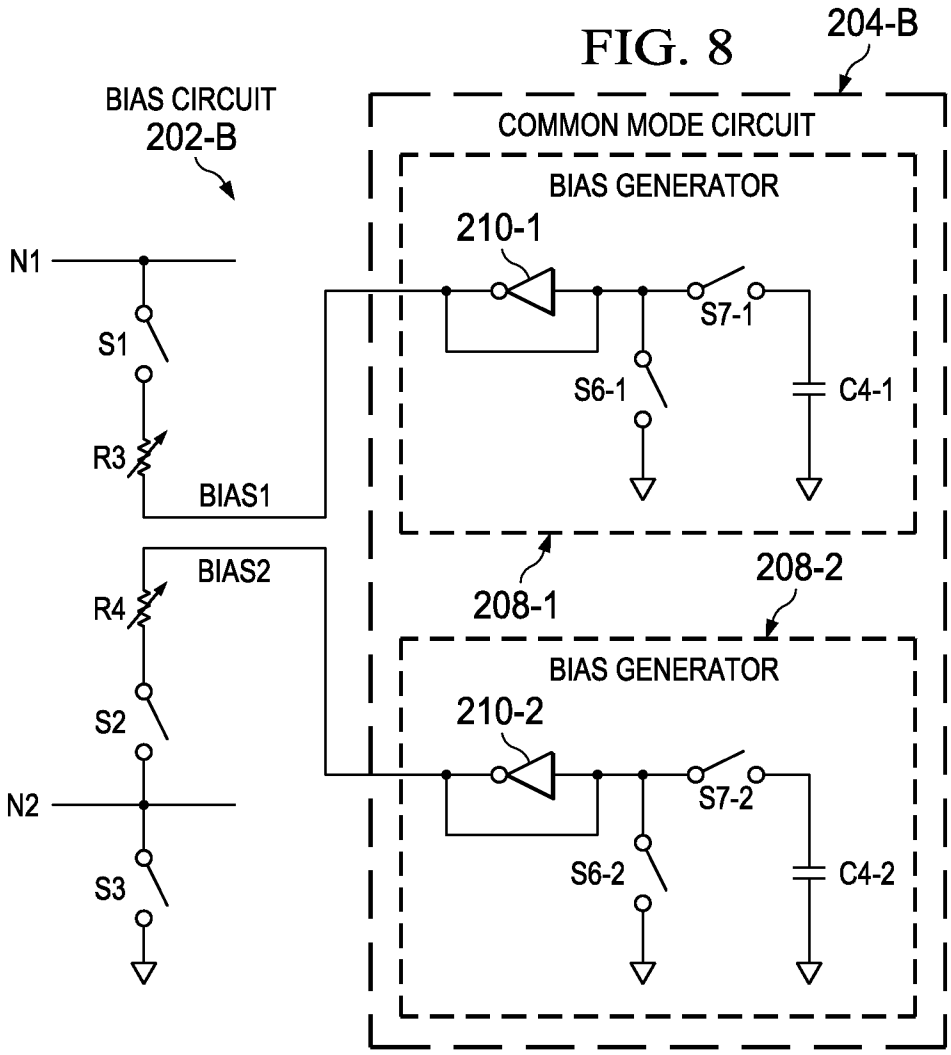


FIG. 8


204-B
BIAS CIRCUIT
202-B
COMMON MODE CIRCUIT
BIAS GENERATOR
210-1
N1
S1
R3
BIAS1
S7-1
S6-1
C4-1
BIAS2
208-1
208-2
R4
S2
N2
S3
BIAS GENERATOR
210-2
S7-2
S6-2
C4-2