(12) UK Patent Application (19) GB (11) 2 102 251 A

(21) Application No **8212656**
(22) Date of filing **30 Apr 1982**
(30) Priority data
(31) **21477**
(32) **30 Apr 1981**
(33) **Italy (IT)**
(43) Application published **26 Jan 1983**
(51) **INT CL³ H04J 3/06**
(52) Domestic classification **H4M** TCX1 TSA1
(56) Documents cited **None**
(58) Field of search **H4M**
(71) Applicants **Italtel Soc Italy Telecomunicazioni SpA (Italy), Piazzale Zavattari 12, 20149 Milano, Italy**
(72) Inventors **Vincenzo Falzone, Marcello Tommasi**
(74) Agents **Marks and Clerk, 57—60 Lincoln's Inn Fields, London, WC2A 3LS**

(54) Improvements in or relating to circuit arrangements for aligning PCM bundles supplied to communications nodes

(57) A circuit arrangement for aligning incoming PCM highways comprises a first functional unit PHADJ which cyclically compares the phase of the signals RRCN of each PCM highway with the phase of a timing signal DCLK of the communication node and introduces a fraction of a bit's delay into the PCM signals whenever the deviation between the falling edge of the timing signal and the transitions of the PCM signals is less than a predetermined quantity. A second functional unit is connected to the output of the first functional unit and complements by a whole number of bits, the delay of the signals of each PCM highway, so as to make the said delay uniform to a predetermined amount.

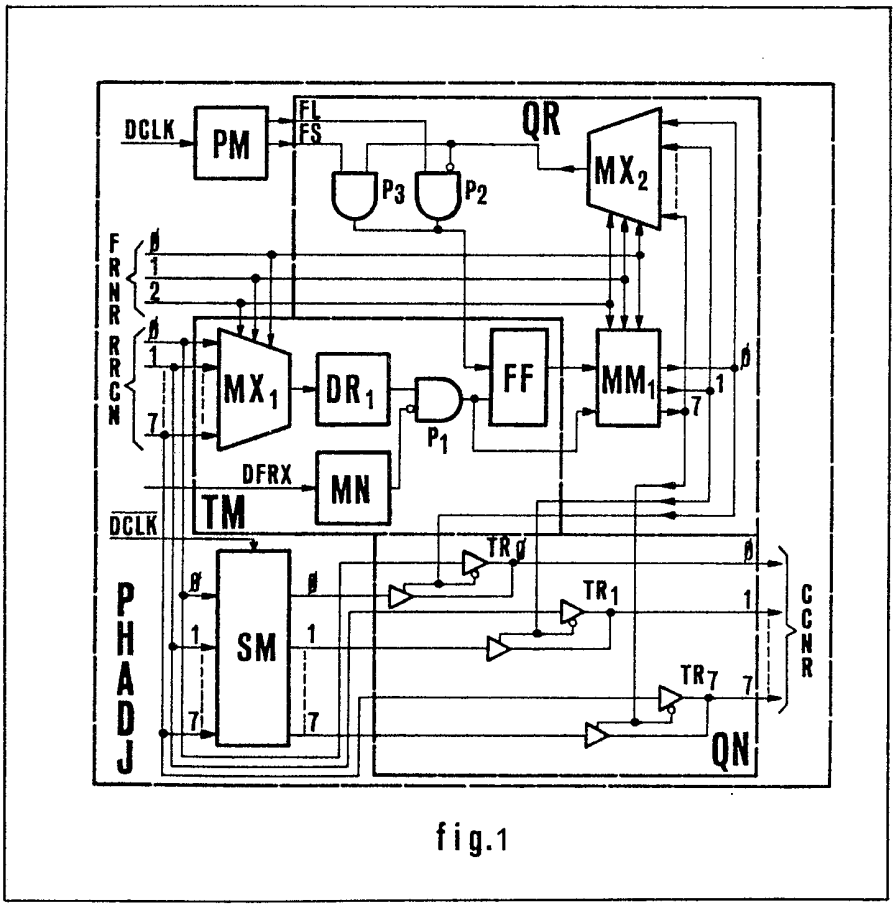

fig.1

GB 2 102 251 A

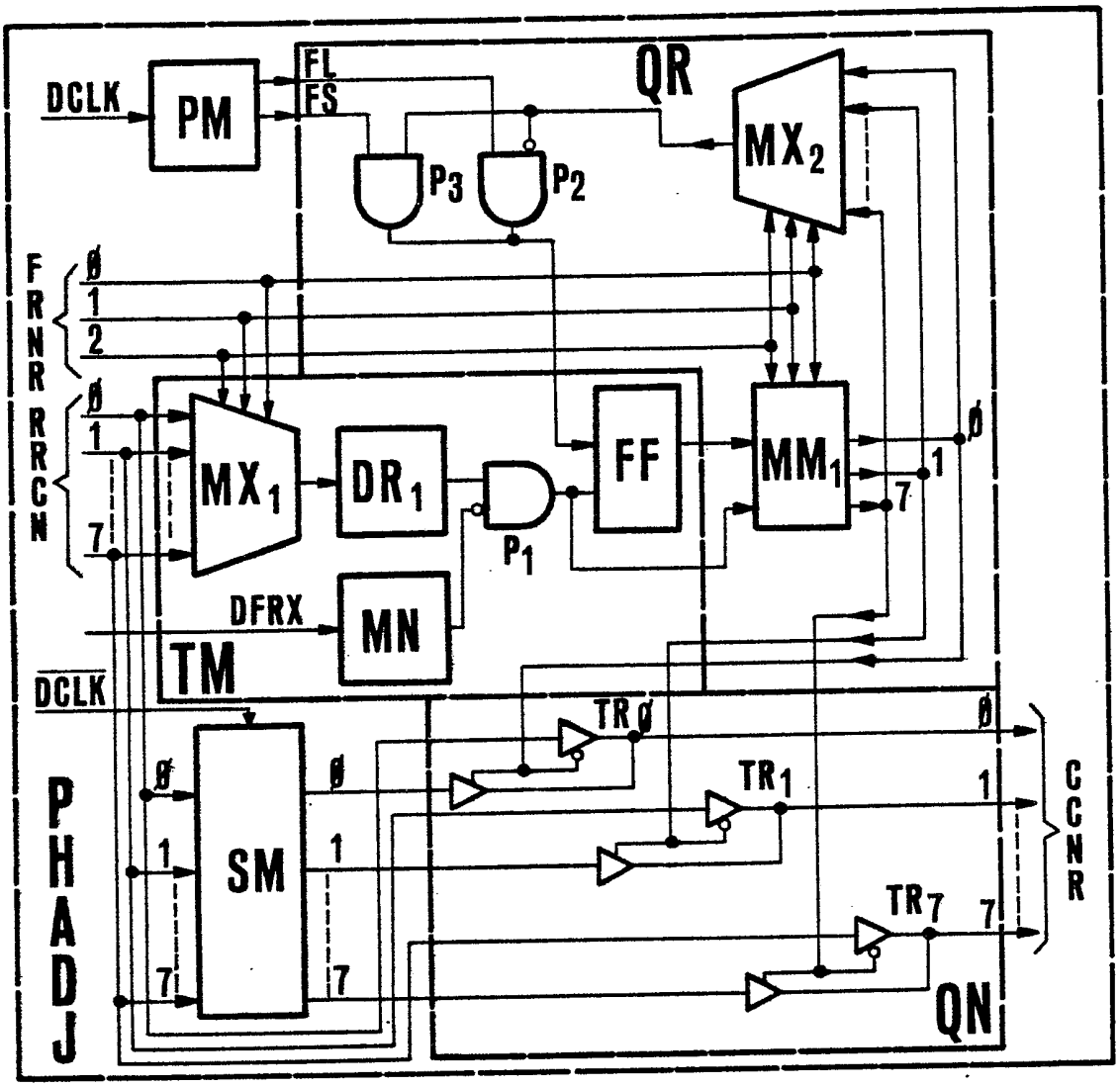
DCLK
PM
FL
FS
QR
MX2
P3
P2
FRNRRRCN
0
1
2
MX1
DR1
FF
MM1
P1
DFRX
MN
TM
DCLK
PHADJ
SM
TR0
TR1
TR7
QN
CCNR

fig.1

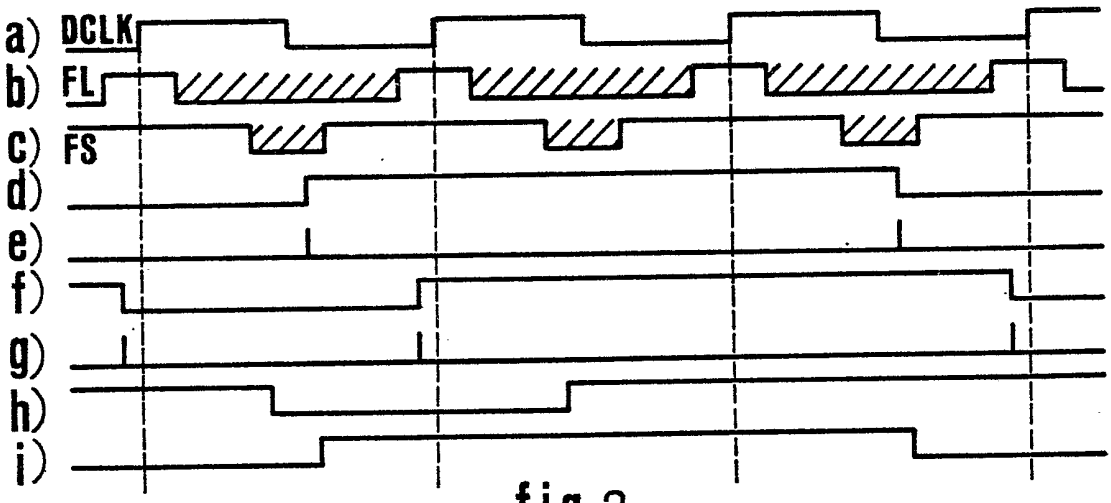
a) DCLK
b) FL
c) FS
d)
e)
f)
g)
h)
i)

fig.2

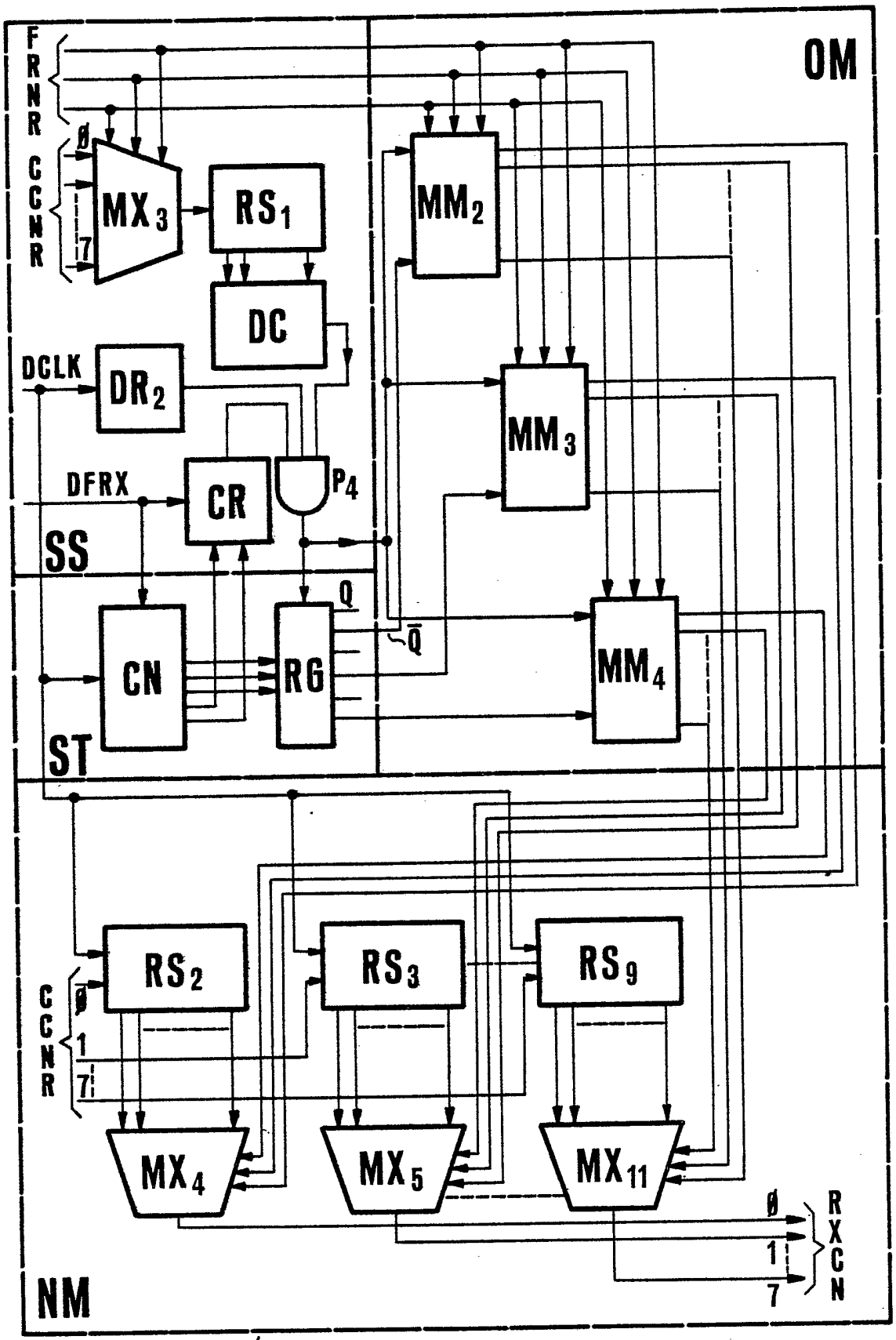
FRNR
CCNR
Ø
7
MX3
RS1
DC
DCLK
DR2
DFRX
CR
P4
SS
Q
Q̄
CN
RG
ST
OM
MM2
MM3
MM4
RS2
RS3
RS9
CCNR
Ø
1
7
MX4
MX5
MX11
Ø
1
7
RXCN
NM
BTADJ

fig.3

SPECIFICATION

Improvements in or relating to circuit arrangements for aligning PCM bundles supplied to communications nodes

The present invention relates to a circuit arrangement for aligning *n* coherent PCM bundles which are supplied to a communication node, such as a switching matrix, but which may be affected by delays that may vary from bundle to bundle.

In Italian patent application no. 19414 A/81 of 30th January 1981, a telephone switching exchange is described which is made up of a plurality of modules, each of which comprises a switching matrix, to the input of which a predetermined number of PCM bundles are connected. The PCM bundles originate from modules disposed at different distances from the one under examination, and so are coherent but may be affected by delays which differ from bundle to bundle.

Before carrying out switching of the digital words allocated in the time channels of the PCM bundles, they must be aligned in such a manner that, at any one instant, there are present at the input of the matrix, the digital words allocated in the i-th time channel of all the bundles. The aligning operations described above are usually carried out by making use of the same number of elastic memories as the number of PCM bundles to be aligned. Generally, a phase locking circuit is associated with each elastic memory, and this supplies a sequence of timing pulses with the same frequency as the PCM bundles to be used to write the PCM signals in their respective memories. Thus the latter are read together, i.e.: at the same time, using the timing pulses of the communication node. Such an arrangement is, however, expensive as it requires the use of as many elastic memories and phase locking circuits as the number of PCM bundles to be aligned.

According to the invention, there is provided a circuit arrangement for aligning signals of *n* PCM bundles supplied to a communication node, comprising a first functional unit arranged to compare cyclically the phase of the signals of each of the *n* PCM bundles with the phase of a timing signal of the communication node having a period T, and to introduce a delay of a fraction of a bit time in the PCM signals when the deviation between the falling edges of the timing signals and the transitions of the PCM signals is more than a predetermined quantity, and a functional unit connected to the output of the first functional unit and arranged to complement, by a whole number of bit times, the delay introduced in the signals of each of the PCM bundles supplied to the second functional unit so as to provide a uniform delay having a predetermined value.

It is thus possible to align the PCM bundles by making use of particularly simple and economical circuits.

In order to avoid continuous changes of decision by such a circuit arrangement, there may be used a time hysteresis which consists in maintaining a previous decision until the slip of the PCM signals exceeds a predetermined amount compared with the timing signal. Thus, the first functional unit can send to the second functional unit PCM signals which are insensitive to the jitters or phase changes of the received signals until such time as the jitters exceed a band of predetermined values.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a first functional unit PHADJ constituting a first part of a preferred embodiment of the invention for performing phase adjustment;

Figure 2 shows wave-forms relating to Figure 1; and

Figure 3 is a block diagram of a second functional unit BTADJ constituting a second part of a preferred embodiment of the invention for performing bit adjustment.

In Figure 1, $RRCN_{\emptyset}, \ldots, RRCN_7$ indicate a corresponding number of PCM bundles, for example 2 M bit/s bundles, supplied to a first functional unit PHADJ arranged to introduce a delay of a fraction of a bit onto each of the signals RRCN in order to supply signals $CCNR_{\emptyset}, \ldots, CCNR_7$, the transitions of which must be spaced from the rising edges of the communication node timing signal DCLK. This is because, downstream from the circuits at present being described, the bits of the signals RRCN are sampled at the rising edges of the signal DCLK in order to discriminate their logic value.

When the edges or transistions of the signals RRCN are "near" to the falling edges of the signal DCLK, operating conditions are favourable for recognizing the received bits as these are sampled at the centre of the bit, whereas when the transitions of the PCM signals are "near" to the rising edges of the signal DCLK, operating conditions are anomalous as the sampling is carried out in proximity to the fronts of the bits. In this latter condition, in the event of jitter being introduced from the transmission lines, it is possible for the sampling of some bits to be missed out altogether, whilst other bits may be sampled twice.

In order to supply signals RRCN whose transitions are spaced from the rising edges of the signal DCLK, the signals RRCN are supplied unaltered or delayed by 1/2 a period when the transitions of the PCM signals are near to the falling or rising edges, respectively, of the signal DCLK.

In order to avoid continuous changes of decision by the circuits which carry out the examination that has just been described, a temporal hysteresis is introduced for maintaining the previous decision taken until such time as the slip of the PCM pulses compared to the pulses DCLK exceeds a predetermined quantity. This temporal hysteresis is obtained by carrying out a comparison between the PCM signal transitions

and two different time windows.

In particular, if the PCM signal was previously supplied unaltered, the following examination is carried out with reference to a "wide" time window around the falling edge of the signal DCLK. In other words, the previous decision is maintained until such time as the PCM signal transitions lie within the wide time window.

On the other hand, if the PCM signal was previously supplied delayed by 1/2 a period, the following examination is carried out with reference to a "narrow" time window around the falling edge of the signal DCLK. In other words the previous decision is modified (iE: changed) when the PCM signal transitions lie within the narrow time window.

In this manner, hysteresis is introduced onto the phase jitter of the received signals so that the signals CCNR output from the functional unit PHADJ are insensitive to the jitter as long as it has a value that is less than a predetermined quantity.

Generation of the time windows described above is performed by first means PM which receives the pulses DCLK illustrated in a diagram (a) of Figure 2, and which is arranged to generate a first signal providing a "wide" time window extending on either side of each falling edge of the signal DCLK, as shown hatched in diagram (b), and a second signal providing a "narrow" time window extending on either side of each falling edge of the signal DCLK, as shown hatched in diagram (c).

Using a signal DCLK with a period $T = 400$ n.secs., the wide time window can be chosen with a duration $T_1 = 300$ n.secs. while the narrow time window can be chosen with a duration $T_3 = 100$ n.secs.

The PCM signals $RRCN_{\emptyset}, \ldots, RRCN_7$ are supplied to second means SM arranged to delay the RRCN signals by T/2, and to third means TM arranged to detect coincidence between the above mentioned time windows and the transitions of the signals RRCN.

In a preferred embodiment, the second means SM comprise a complex of 8 bistable circuits of D type whose data inputs receive respective signals RRCN and whose timing inputs receive the signal $\overline{DCLK}$.

The third means TM comprises a first multiplexer MX_1, whose data inputs receive the signals RRCN and whose address inputs receive the signals $FRNR_{\emptyset}$, $FRNR_1$, $FRNR_2$, which enable the sequential transmission of the signals RRCN. The number expressed by the signals FRNR is increased after an interval of time equal to the frame time (for example 125u secs) of the PCM signals.

The PCM signals relating to the bundle RRCN at the output of the multiplexer MX_1 at each instant, (see diagram d) are supplied to a differentiating circuit DR_1, whose output produces a pulse corresponding to each transition of the intput signals as illustrated in diagram (e).

The pulses from the output of the circuit DR_1 are supplied to a gate circuit P_1 which is disabled by the signal at the output of a monostable circuit MN which excites its output for a predetermined interval of time in response to the reception of a pulse DFRX which is active at the beginning of each frame.

In this way the passage through the circuit P_1 of the pulses generated by the circuit DR_1 is inhibited for such an interval of time that the passage determined by the increase in the number FRNR can be considered cancelled.

The pulses corresponding to the output of the circuit P_1 are supplied to the timing input of a bistable circuit FF of D type which receives at its data input one of the signals generated by the first means PM.

The output from the third means TR is stored in fourth means QR which supplies the time windows to the third means TM enabling signals to fifth means QN.

The fifth means QN includes 8 pairs of transmitting circuits $TR_{\emptyset}, \ldots, TR_7$. One transmitter of each pair receives the signals $RRCN_i$ supplied to the input of the means SM, whereas the other transmitter of each pair receives the corresponding signals that have been delayed by the means SM. The fourth means QR includes a random access memory MM_1 having 8 memory cells which are addressed by the number FRNR mentioned above. The memory MM_1 is arranged to store, for each PCM bundle, the logic level that corresponds to the output of the circuit FF when a pulse is produced by the circuit P_1. The outputs from the memory MM_1 are supplied to a second multiplexer MX_2 which at its address inputs receives the signals FRNR. The output of the multiplexer MX_2 enables a second or third gate circuit P_2 or P_3, which respectively receive at their other input the input the signal FL or the signal FS.

When the apparatus is turned on, bits of logic level Ø are written in the memory MM, so that the pulse that corresponds to the output of the multiplexer MX_2 enables the gate circuit P_2, through which the wide time window signed FL passes. When the number FRNR addresses the system $RRCN_{\emptyset}$ and the relative signals have the phase illustrated in diagram (d), the pulses represented in diagram (e) will correspond to the output of the circuit DR, and these pulses coincide with the wide time window FL, so that a pulse of logic level nought corresponds to the output of the circuit FF and this is stored in the cell of the memory MM relating to that bundle. This pulse is also supplied to the enabling input of the transmitter $TR_{\emptyset}$, thus activating the transmitter which receives the signals $RRCN_{\emptyset}$ at the input of means SM. In fact, because the transitions of the signals $RRCN_{\emptyset}$ coincide with the time window FL, the rising edge of the signals DCLK lies in the central position of the received bits so that this condition is favourable for their sampling.

When the number FRNR increases, it addresses the following cell of the memory MM in which a pulse of logic level nought is stored which enables the circuit P_2 and consequently the signal FL is present on the input of the circuit FF.

If the signals $RRCN_1$ have the phase illustrated in diagram (f), the pulses illustrated in diagram (g) correspond to the output of the circuit DR_1, and these do not coincide to the signal FL so that a pulse of logic level 1 corresponds to the output of the circuit FF. This pulse is stored in the memory MM_1 and enables the transmitter TR_1 which receives the signals $RRCN_1$ delayed by the means SM.

The rising edges of the signal DCLK lie in priximity to the rising edges of the signal illustrated in diagram (f), whereas they lie in the central part of the bits of the same signal when delayed, as is illustrated in diagram (h).

After the remaining PCM systems have been scanned, when the number FRNR once again assumes value Ø, a pulse of logic level nought is provided at the output of the memory MM and this activates the circuit P_2 determining a comparison with the FL signal. If the pulses at the output of the circuit DR_1 coincide with the wide time window FL, then a pulse of logic level nought is once again stored.

When on the other hand, the number FRNR assumes value one, a pulse of logic level one is provided at the output of the memory MM, and this pulse activates the circuit P_3 so that, in this case, the circuit FF carries out a comparison with the narrow time window FS. If the pulses at the output of the circuit DR_1 do not coincide with the time window FS, a pulse of logic level one is stored in the memory MM and consequently the transmitter TR_1 supplies the signals $RRCN_1$ after they have been delayed by the means SM.

The supply of the signals $RRCN_1$ affected by a delay will continue until their slip in comparison to the signals DCLK assumes such a value as to make their transitions coincide with time windows FS, as illustrated in diagram (i). When such a case as that just described happens, a pulse of logic level nought is provided at the output of the memory MM, and this activates the transmitter TR_1 to output the signals $RRCN_1$ at the input to the means SM. By utilizing the signals FL and FS which present time windows of the durations described above, the signals CCNR are immune to the jitter of the input signals RRCN as long as this is less than 100 n secs. This is in fact the highest slip that the signals RRCN can accommodate compared to the signal DCLK without determining changes of decision by the third means TM.

In Figure 3 the second functional unit BTADJ is illustrated in detail and is arranged to introduce a delay (or lag) of a whole bit number in each of the signals CCNR so as to align them in a frame.

The signals $CCNR_0, \ldots, CCNR_7$ are supplied to a multiplexer MX_3 which forms part of sixth means SS arranged to output a pulse in response to detection of the instant of the beginning of the frame of each of the signals CCNR.

The multiplexer MX_3 receives at its address input the abovementioned number FRNR, the increase of which determines the sequential output of the signals CCNR. A shift register RS_1 is connected to the output of the multiplexer MX_3 and has eight memory cells which are connected to a decoding unit DC arranged to supply a pulse when the characteristic binary configuration of the synchronizing word is present in the register RS_1. The output of the unit DC is input to an AND gate P_4 which receives, on a second input, the signal corresponding to the output of a differentiating circuit DR_2 arranged to supply a pulse corresponding to each negative transition of the signal DCLK, and on a third input, the signal corresponding to the output of a recognition circuit CR arranged to activate its output for an interval of time equal to the duration of the first time channel of the frame.

If, during the first time channel of the frame relating to the PCM system selected by the multiplexer MX_3, the presence of the synchronizing word is detected, a pulse is produced by the gate P_4 to enable seventh means ST for calculating the delay of the signal $CCNR_i$, selected by the multiplexer MX_3, compared to the instant of the beginning of the frame defined by DFRX. In particular, the seventh means St supplies a binary configuration which expresses the number of bits by which the signal $CCNR_i$ must be delayed in order to complement its delay with the maximum predetermined delay.

If it has been decided beforehand to realize aligning by delaying the signals CCNR by 8 bits and that the PCM system selected by the multiplexer MX_3 is affected by a delay of 5 bits, then the means ST supplies a binary configuration expressing the number of bits 3 by which it must be delayed in order to provide a delay of 8 bits.

The means St includes a counter CN which receives the signals DCLK and whose three most significant outputs are supplied to a register RG arranged to store the bits present on its input when the output of the gate P_4 is active. In this manner, the number of the pulses of the sequence DCLK counted between the instant defined by DFRX and the instant at which the synchronizing word is received is stored. The complement in 8 of the number stored is supplied by the inverted outputs of the register RG. The three bits expressing the complemented delay are sent to eight means OM arranged to store them in a respective cell of as many memories MM_2, MM_3, MM_4, which are enabled to write, by the pulse at the output of the gate P_4, at the address specified by FRNR.

The i-th outputs of the memories MM_2, MM_3, MM_4 are grouped together and sent to the address inputs of respective multiplexers $MX_4, \ldots, MX_{11}$, data inputs of which are connected to the parallel outputs of shift registers $RS_2, \ldots, RS_9$. The registers $RS_2, \ldots, RS_9$ receive respective signals CCNR at their inputs and store them with timing defined by the sequence of timing pulses DCLK.

The shift registers $RS_2, \ldots, RS_9$ each have 8 memory cells and each cell delays by one bit the signal provided by the previous cell, so that the respective multiplexer is addressed by the signals present on the address inputs in such a manner as to pick up the output of the cell of the register that

delays its respective signal RRCN by the amount calculated by the sixth means SS.

In other words, if the signal $CCNR_7$ has to be delayed by 3 bits in order to complement its delay to 8 bits, the multiplexer MX_{11} supplies the signal present on the third output of the register RS_9.

Therefore, the signals RXCN all having the same delay are provided at the outputs of the multiplexers $MX_4, \ldots, MX_{11}$ so that they appear aligned with each other as desired.

CLAIMS

1. A circuit arrangement for aligning signals of *n* PCM bundles supplied to a communication node, comprising a first functional unit arranged to compare cyclically the phase of the signals of each of the *n* PCM bundles with the phase of a timing signal of the communication node having a period T, and to introduce a delay of a fraction of a bit time in the PCM signals when the deviation between the falling edges of the timing signal and the transitions of the PCM signals is more than a predetermined quantity, and a second functional unit connected to the output of the first functional unit and arranged to complement, by a whole number of bit times, the delay introduced in the signals of each of the PCM bundles supplied to the second functional unit so as to provide a uniform delay having a predetermined value.

2. A circuit arrangement as claimed in claim 1, in which the first functional unit comprises: first means for generating first and second signals representing time windows of duration $T_1<T$ and $T_2<T_1$, respectively, surrounding each falling edge of the timing signal; second means for delaying by the predetermined quantity $T_3<T$ the PCM signals of the *n* bundles; third means for sequentially checking whether the transitions of the PCM signals of each of the *n* bundles lie within the first and second time windows and for supplying a pulse each time that the check gives a negative result; fourth means for storing for each of the *n* bundles the presence or absence of an output pulse from the third means and for enabling the supply of the first signal or the second signals to the third means in response to the absence or presence, respectively, of the said pulse in the memory cell associated with the PCM bundle under examination; and fifth means for sending the PCM signals at the input or output of the second means to the second functional unit in response to the absence or presence, respectively, of the pulse in the respective memory cell of the fourth means.

3. A circuit disposition as claimed in claim 1 or 2, in which the second functional unit comprises: sixth means for sequentially scanning the PCM signals from the first functional unit and for supplying a pulse when the presence of the synchronizing word in the time channel reserved for it is detected; seventh means for counting the number of timing pulses which occur between reception of a pulse indicating the beginning of a frame and the appearance of the pulse at the output of the sixth means, and for supplying a number expressing the complement of the said number of timing pulses in the number of bit times representing the delay of predetermined value; eighth means for storing the number provided by the seventh means for each of the *n* PCM bundles; and nineth means for delaying each PCM bundle from the first functional unit by the corresponding number of bit times stored in the eighth means.

4. A circuit arrangement as claimed in claim 2 or in claim 3 when dependent on claim 2, in which the third means comprises: a first multiplexer whose data input is arranged to receive the *n* PCM bundles, and whose address input of which is arranged to receive a first number which is incremented after an interval of time equal to the frametime; a first differentiating circuit connected to the output of the first multiplexer; a monostable circuit arranged to activate its output for a predetermined time in response to reception of a pulse indicating the beginning of a frame; a first gate circuit arranged to enable the passage of pulses from the output of the first differentiating circuit when the monostable circuit deactivates its output; and a bistable circuit of D type arranged to receive at its timing input the pulses from the output of the first gate circuit and at its data input the first or second signal provided by the fourth means.

5. A circuit arrangement as claimed in claim 4, in which the fourth means comprises: a first memory having *n* cells and arranged to be addressed by the first number; a second multiplexer arranged to receive at its address input the first number and at its data input the outputs of the first memory; and second and third gate circuits arranged to receive the first and second signals, respectively generated by the first means and an enabling signal from the output of the second multiplexer.

6. A circuit arrangement as claimed in claim 3, or in claim 4 and 5 when dependent on claim 3, in which the sixth means comprises: a third multiplexer the data input of which is arranged to receive the PCM signals from the first functional unit and the address input of which is arranged to receive the first number; a first shift register connected to the output of the third multiplexer; a decoding unit connected to the outputs of the first shift register; a second differentiating circuit arranged to receive the timing pulses; a recognition circuit arranged to activate its output for an interval of time equal to the duration of a time channel starting from the beginning of frame pulse; and an AND gate whose inputs are connected to the output of the decoding unit, the output of the second differentiating circuit, and the output of the recognition circuit.

7. A circuit arrangement as claimed in claim 6, in which the seventh means comprises: a counter, the counting input of which is arranged to receive the timing pulses and the zero setting input of which is arranged to receive the beginning of frame pulse; and a register arranged to store the number present in the counter when the output of

the AND gate is active, and to invert the logic level of the bits expressing the stored number.

8. A circuit arrangement as claimed in claim 3 or in any one of claims 4 to 7 when dependent on claim 3, in which the nineth means comprises a complex of *n* shift registers arranged to receive the *n* PCM bundles, respectively, and a complex of *n* multiplexers each of which is arranged to receive at its address input the respective number stored by the eighth means and at its data input the outputs of the respective shift register of the complex.

9. A circuit arrangement for aligning signals of *n* PCM bundles supplied to a communication node, substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1983. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.