

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
31 January 2002 (31.01.2002)

PCT

(10) International Publication Number
WO 02/009178 A3

(51) International Patent Classification⁷: **H01L 29/49**,
21/28, 29/94

(21) International Application Number: PCT/US01/22660

(22) International Filing Date: 18 July 2001 (18.07.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/621,804 21 July 2000 (21.07.2000) US

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(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

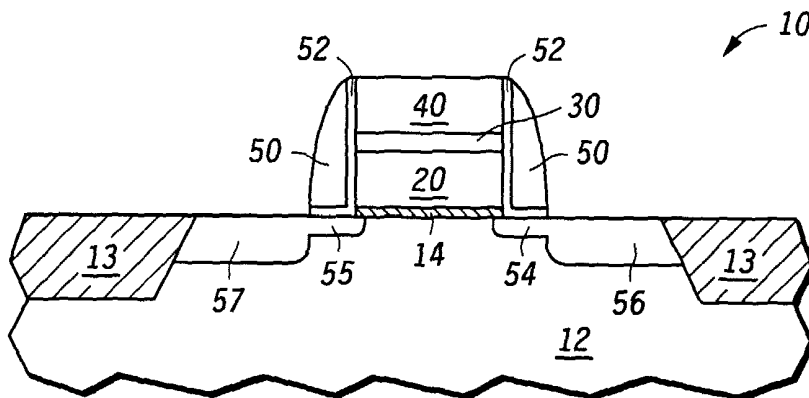
Published:

— with international search report

(88) Date of publication of the international search report:
10 October 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE SAME



(57) Abstract: A semiconductor device (10) has a conductor that overlies an insulating layer (14) and has a first conductive portion (20), a second conductive portion (30), and a third conductive portion (40). The second conductive portion (30) lies between the first (20) and third conductive (40) portions. The first conductive portion (20) has a first element, and the third conductive portion (40) includes a metal and silicon without a significant amount of the first element. The conductor may be a gate electrode or a capacitor electrode.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 01/22660

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L29/49 H01L21/28 H01L29/94

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 719 410 A (AKASAKA YASUSHI ET AL) 17 February 1998 (1998-02-17) column 13, line 16 - line 32 column 15, line 59 - line 63; figures 10A-10D ---	1-31
A	WO 99 43024 A (COMMISSARIAT ENERGIE ATOMIQUE ; BENSACHEL DANIEL (FR); CAMPIDELLI YV) 26 August 1999 (1999-08-26) figures 1A-1G ---	1-31
A	WO 98 13880 A (ADVANCED MICRO DEVICES INC) 2 April 1998 (1998-04-02) page 14, line 5 - line 19; claims 2,3; figure 3 --- -/--	1-31



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

25 June 2002

Date of mailing of the international search report

04/07/2002

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 01/22660

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	UEJIMA K ET AL: "HIGHLY RELIABLE POLY-SIGE/AMORPHOUS-SI GATE CMOS" INTERNATIONAL ELECTRON DEVICES MEETING 2000. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 10 - 13, 2000, NEW YORK, NY: IEEE, US, 10 December 2000 (2000-12-10), pages 445-448, XP000988878 ISBN: 0-7803-6439-2 figure 1A ---	1, 11, 21
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P, X	EP 1 111 686 A (SEIKO EPSON CORP) 27 June 2001 (2001-06-27) figure 2 -----	1, 3, 9, 11, 13, 19, 21, 23, 24

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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