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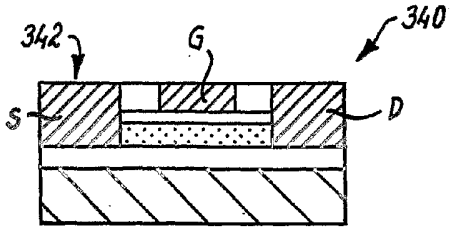
(54) Title: A TRANSISTOR DEVICE WITH METALLIC ELECTRODES AND A METHOD FOR USE IN FORMING SUCH A DEVICE



(57) Abstract: A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising: a first layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode; a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and a third layer comprising a substrate, wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer.

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A Transistor Device With Metallic Electrodes And A Method For Use In Forming Such A Device

FIELD OF THE INVENTION

Embodiments of the invention relate to transistor devices with metallic electrodes and methods for forming such devices. Some embodiments relate to thin film transistor (TFT) devices that are suitable for integration in large area substrates at low cost.

BACKGROUND TO THE INVENTION

JP63299296 (Meiko), JP63299297A (Meiko) and "Manufacturing of Printed Wiring Boards by Ultra-high Speed Electroforming" by Norio Kawachi (Meiko) et al, Printed Circuit World Convention, June 1990 describe the use of the electroforming technique in creating circuit boards (printed wiring boards). Electroforming is an additive process that involves obtaining a replica (negative) of a metal carrier by electrolytic deposition of a metallic film using the carrier as a cathode. A patterned photo-resist is used to limit the electro-deposition of material to the exposed areas of the cathode. The documents additionally teach a transfer lamination process in which the deposited metal and photo-resist are laminated to a substrate and the master is removed leaving a deposited metal photo-resist substrate combination. JP63299296 (Meiko), JP63299297A (Meiko) additionally disclose the electrolytic deposition of a copper plate layer on the master before the deposition of the metal. This copper layer is transferred in the transfer-lamination process and is removed by etching.

US6,284,072 discloses the formation of patterning on a conductive carrier by micro-moulding. An insulating material is embossed to create a pattern that limits the electro-deposition of metal to exposed areas of the conductive carrier.

Electroforming is used in the semiconductor industry in the creation of printed wiring boards and large scale interconnects on bulk semiconductors. Electroforming is not accurate enough for use in bulk semiconductor device processing which is at a scale of nanometres.

The bulk semiconductor industry typically uses metal sputtering with UV photo-lithography to define small scale metal interconnects.

Organic semiconductors are a fairly recent development compared with bulk semiconductors. Devices made from organic semiconductors cannot match the speed or efficiencies of bulk semiconductors, but they have other distinct advantages. They are suitable for large area processing and can be used on flexible substrates. They have therefore attracted a lot of attention for their potential application in display device technologies, particularly their use in thin film transistors for use in active matrix displays.

An organic transistor typically has metallic source, gate and drain electrodes. A thin film of organic semiconductor forms a channel interconnecting the source and drain electrodes, that is separated from the gate electrode by a thin dielectric layer.

As years of research into the creation of bulk semiconductors have been carried out, the organic transistors presently re-use technology developed for bulk semiconductors as these processes are well understood. For example, the metallic electrodes are typically created by metal sputtering.

The inventors have realised that the use of sputtering may be optimal for bulk semiconductors but is sub-optimal for low cost, large area integrated circuits, such as displays incorporating organic thin film transistors.

Sputtering requires a vacuum environment. This is expensive and difficult to implement for large area processes.

Also, to obtain low impedance interconnects using sputtering the interconnects must either be wide or thick. A thick interconnect can create stresses which require controlling, which adds cost. Thick interconnects may limit the resolution of the devices (the number per unit area).

US6344662 describes the creation of a TFT having a hybrid organic-inorganic semiconductor layer. The gate metallization is formed using electron beam evaporation and the metal source and drain are formed separately by vapor deposition. Claim 6 states, without further explanation or clarification, that the gate electrode is produced by a process selected from the group consisting of evaporation, sputtering, chemical vapor deposition, electrodeposition, spin coating, and electroless plating

BRIEF DESCRIPTION OF THE INVENTION

It would therefore be desirable to provide an improved method for creating a semiconductor device suitable for integration in large area substrates at low cost.

Some embodiments of the invention provide a transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising: a first layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode; a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and a third layer comprising a substrate , wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer.

Some embodiments of the invention provide a method for use in forming a transistor device comprising:

(i) forming a transfer layer on a conductive carrier;

(ii) fixing the transfer layer to a substrate; and

(iii) removing the conductive carrier, wherein the transfer layer is formed in step (i) by:

a) selectively masking the conductive carrier, to expose first, second and third portions of the conductive carrier;

b) electro-depositing metal onto the first, second and third portions of the conductive carrier to form first, second and third metal portions;

c) depositing dielectric material over at least the second metal portion;

d) electro depositing metal on the first and third metal portions; and

e) depositing semiconductor material over the dielectric layer.

Some embodiments of the invention provide a method for use in forming a transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising: a first upper planar layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode; a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and a third lower planar layer comprising a substrate, wherein first, second and third planar layers are arranged in order such that the second middle layer is positioned between the first upper layer and the third lower layer, wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal, the gate electrode occupies only the first upper planar layer and the channel occupies only the second middle planar layer, the metallic source electrode consists of the first metal portion of the metallic source electrode overlying the second metal portion of the metallic source

electrode and the metallic drain electrode consists of the first metal portion of the metallic drain electrode overlying the second metal portion of the metallic drain electrode.

The terms electro-deposition and electrolytic deposition are synonymous.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention and to understand how it may be brought into effect reference will now be made to the accompanying drawings of example embodiments of the invention in which:

Figs 1A to 1H illustrate stages in forming a transistor device 340; and
Fig 2 illustrates the transistor device 340.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Figs 1A to 1H schematically illustrate the stages during an additive method for forming a layered thin film transistor (TFT) device 340 using electrolytic deposition and transfer lamination. The figures are not to scale.

Fig 1A illustrates a passivated substantially planar conductive carrier 302. This may be a platen or a sheet of material in a roll to roll process. The passivated substantially planar conductive carrier 302 includes a passivation layer 304 this may for example include a very thin oxide and/or a surfactant.

Figs 1B and 1C illustrate the formation of a first layer 316 of the transistor device on the conductive carrier 302. In Fig 1B insulating material 306 is selectively formed on the passivated conductive carrier 302 by a selective additive process or a selective subtractive process. In a selective subtractive process, insulating material is deposited over the whole of the passivated

conductive carrier 302 as a substantially planar layer and selectively removed from first, second and third portions 308a, 308b and 308c of the passivated conductive carrier 302. In a selective additive process, insulating material is deposited only in the regions of the passivated conductive carrier 302 where required to form patterned structures 306. This may be achieved, for example, by embossing, micro-molding, photolithography or any other suitable alternative process. If photolithography is used, the insulating material 306 is preferably photo-patternable. It is selectively exposed to radiation through a mask or using a spot-laser and developed to expose the portions 308a, 308b and 308c of the conductive carrier 302. One suitable photo-patternable insulator is SU-8 by Micro-Chemical Corporation. This is a hard UV cure polymer, which is used at a thickness of between 1 and 5 μm.

The conductive carrier 302 is connected as a cathode and metal is deposited by electrolytic deposition on the first, second and third exposed portions 308a, 308b and 308c of the passivated conductive carrier 302 to form respective first, second and third metal portions 310a, 310b and 310c. The first metal portion 310a will eventually form part of the drain of the transistor device 340. The second metal portion 310b will eventually form the gate of the transistor device 340. The third metal portion 310c will eventually form part of the source of the transistor device 340.

The metal may be any metal that is capable of electrolytic deposition with good conductivity e.g. Ni, Cu, Ag, Au. It is typically deposited with a thickness of between 2 and 5 μm.

In Fig 1D, dielectric material 322 is selectively formed. It covers the second metal portion 310b and overlaps the portions of the insulating layer 306 that separate the second metal portion 310b from the first metal portion 310a and from the third metal portion 310c. The dielectric material 322 may be formed from photo-patternable material, such as SU8, which is deposited over the whole of the first layer 316 and laser spot cured in the area where it is to

remain. Development of the resist removes it to form the dielectric material 322 covering the second metal portion 310b. The overlap of the dielectric material 322 with the portions of the insulating layer 306, provides tolerance in the alignment of the laser.

The dielectric material 322 therefore covers the second metal portion 310b. This masks the second metal portion 310b from further electrolytic deposition. The dielectric material 322 forms the gate dielectric of the final transistor device 340. The dielectric layer typically has a thickness of the order 100-600nm. The width of the dielectric layer exceeds the width of the second metal portion 310b of the transistor device 340, which is typically 1-5 μm.

Anisotropic electrolytic deposition of metal is then carried out. As illustrated in Fig. 1E, a first further metal portion 324a is deposited on the first metal portion 310a and a second further metal portion 324c is deposited on the second metal portion 310c. The combination of the metal portions 310a and 324a forms the drain of the final transistor device 340 and the combination of the metal portions 310c and 324c forms the source of the final transistor device 340. A well or channel 326 is formed above the dielectric 322 and between the first and second further metal portions 324a and 324c. Brightening agents can be added to the electrolytic solution to control the isotropy/anisotropy of metal growth. This can be used to control the cross-sectional profile of the well or channel 326.

In Fig. 1F, semiconductor material 330 is deposited into the well or trench 326 to fill it. The semiconductor may, for example, be an organic semiconductor, a solution processable semiconductor, nano-particulate dispersion of semiconductor; conjugated polymers or oligomers in solution. The semiconductor may be deposited by spinning it on in liquid solvent form and evaporating the solvent. Alternatively micro-dispensing techniques such as piezo inkjet or thermal inkjet may be used to selectively fill the well or trench

326 . Further laser, heat or radiation processes may be used to improve the semiconductor properties.

The semiconductor material 330 completes the second layer 318 of the transistor device 340. The second layer 318 includes the further first metal portion 324a, the further third metal portion 324c, the semiconductor material 330 and the dielectric 322. No etch-back or patterning is required to place the semiconductor material in the well or channel 326.

The first and second layers 316 and 318 form a transfer layer which is transferred to a passive substrate 314. The passive substrate 314 is adhered to the substantially planar upper surface of the second layer 318 using a layer of adhesive 312 as illustrated in Fig. 1G. This substrate will form the substrate of the final TFT 340. The substrate 314 may be made of glass. Alternatively, it may be a flexible plastic substrate, for example, made from PET. The adhesive used may be NOA81 by Norland Products Inc. The thickness of the substrate 314 is typically between 50 and 200μm. The thickness of the adhesive layer 312 is typically between 5 and 20μm.

The adhesive layer 312 is cured using ultra-violet (UV) radiation or applied heat. The structure may then be shock-cooled and the passivated conductive carrier 302 is removed (peeled-off) to form the TFT device 340, as illustrated in Fig 1H. In Fig 1H, the structure has been inverted.

The final TFT device is illustrated in Fig 2. It has a metallic source electrode S, a metallic drain electrode D and a metallic gate electrode G comprising: a first notional layer 316 including the metallic gate electrode G, a first portion 310c of the metallic source electrode S and a first portion 310a of the metallic drain electrode D; a second notional layer 318 including a second portion 324c of the metallic source electrode, a second portion 324a of the metallic drain electrode and deposited semiconductor material 330 overlying dielectric

material 322; and a third layer 320 including a passive substrate 314 and adhesive 312. The join between the first layer 316 and the second layer 318

through the source S and drain D may be discernable. The metal portions 310a, 310b, 310c, 324a and 324c will generally contain artefacts of the electrolytic process by which they were formed. The TFT device 340 has an upper substantially planar surface 342 including the upper substantially planar surfaces of the first, second and third metal portions 210a, 210b and 210c.

The substrate 314 may be a large area flexible substrate (many square centimetres or metres) with thousands or millions of devices 340 integrated thereon.

It should be appreciated that the above-described method has a number of advantages. The method requires a small number of masks and the associated problem of their accurate alignment is limited. The use of electrolytic deposition of metal on the first and second metal portions to form the relief for receiving the semiconductor 330 is a self-aligning process. The above-described processes can be carried out at low temperature (room temp +/- 100 degrees Celsius) and without vacuum processing. There may additionally be no need for further processing on the final substrate 314, which may be flexible plastic for example. The semiconductor material is encapsulated within the surface of the resulting device, rendering it robust and reducing susceptibility to any contamination/chemical attack from subsequent processing. The resulting upper surface of the device may be substantially planar which is also advantageous for further processing, particularly in display applications.

Although embodiments of the present invention have been described in the preceding paragraphs with reference to various examples, it should be appreciated that modifications to the examples given can be made without departing from the spirit and scope of the invention. For example, referring to

Figs 1E and 1F, the electro-deposition of metal to form the further first and third metal portions 324a and 324c may occur before or after the deposition of semiconductor material 330.

Whilst endeavoring in the foregoing specification to draw attention to those features of the invention believed to be of particular importance it should be understood that the Applicant claims protection in respect of any patentable feature or combination of features hereinbefore referred to and/or shown in the drawings whether or not particular emphasis has been placed thereon.

I/we claim:

CLAIMS

1. A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:
a first layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;
a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and
a third layer comprising a substrate, wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer.

2. A transistor device as claimed in claim 1, wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal.

3. A transistor device as claimed in claim 1 or 2, wherein the first, second and third layers are each of respective substantially uniform thickness.

4. A transistor device as claimed in claim 1, 2 or 3, wherein the third layer includes adhesive bonding the passive substrate to the transistor device.

5. A transistor device as claimed in any one of claims 1 to 4, wherein the first layer has a substantially planar surface comprising substantially planar portions of the source, drain and gate electrodes.

6. A transistor device as claimed in any one of claims 1 to 5, wherein the deposited semiconductor material comprises organic semiconductor material.

7. A transistor device as claimed in any one of claims 1 to 6, wherein the deposited semiconductor material comprises indications that it was deposited from liquid.

8. A transistor device as claimed in any one of claims 1 to 7, wherein the semiconductor material is embedded in the device and overlain by the gate electrode.

9. A transistor device as claimed in any preceding claim wherein the first layer comprises insulating material separating the gate electrode from the source electrode and the drain electrode.

10. A transistor device as claimed in claim 9, wherein the insulating material is photo-patternable.

11. A transistor device as claimed in any preceding claim wherein the substrate is flexible.

12. A substrate for a display device comprising a plurality of transistor devices as claimed in any preceding claim.

13. A method for use in forming a transistor device comprising:
(i) forming a transfer layer on a conductive carrier;
(ii) fixing the transfer layer to a substrate; and
(iii) removing the conductive carrier, wherein the transfer layer is formed in step (i) by:

a) selectively masking the conductive carrier, to expose first, second and third portions of the conductive carrier;

b) electro-depositing metal onto the first, second and third portions of the conductive carrier to form first, second and third metal portions;

c) depositing dielectric material over at least the second metal portion;

d) electro depositing metal on the first and third metal portions; and

e) depositing semiconductor material over the dielectric layer.

14. A method as claimed in claim 13, wherein the step of selectively masking the conductive carrier includes the selective formation of insulating material on portions of the conductive carrier and the retention of the insulating material within the transistor device.

15. A method as claimed in claim 13 or 14, wherein the transfer layer provides a terminal layer of the device.

16. A method as claimed in claim 13, 14 or 15, wherein the step of fixing the transfer layer to a substrate portion embeds semiconductor material within the device.

17. A method as claimed in any one of claims 13 to 16, wherein the semiconductor material deposited in step e) is selectively deposited between the metal deposited in step d).

18. A method as claimed in any one of claims 13 to 16, wherein the step e) precedes step d).

19. A method as claimed in any one of claims 17 to 20, further comprising the step of passivating the conductive carrier before step a).

20. A method as claimed in any one of claims 13 to 19, wherein the conductive carrier is of substantially uniform thickness.

21. A method as claimed in any one of claims 13 to 20, wherein the step of fixing the transfer layer to the substrate involves the application of a curable adhesive to the substrate, the contacting of the adhesive layer and the transfer layer and the curing of the adhesive.

22. A semiconductor device formed using the method as claimed in any one of claims 13 to 21.

23. A device or method substantially as hereinbefore described with reference to and/or as shown in the accompanying drawings.

24. Any novel subject matter or combination including novel subject matter disclosed, whether or not within the scope of or relating to the same invention as the preceding claims.

25. A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:

a first upper planar layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;

a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and

a third lower planar layer comprising a substrate, wherein first, second and third planar layers are arranged in order such that the second middle layer is positioned between the first upper layer and the third lower layer,

wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal, the gate electrode occupies only the first upper planar layer and the channel occupies only the second middle planar layer, the metallic source electrode consists of the first metal portion of the metallic source electrode overlying the second metal portion of the metallic source electrode and the metallic drain electrode consists of the first metal portion of the metallic drain electrode overlying the second metal portion of the metallic drain electrode

26. A transistor device as claimed in any one of claims 1 to 12 or claim 25, wherein the metallic source, gate and drain electrodes consist entirely of electro-deposited material and the metallic gate electrode contacts the dielectric material.

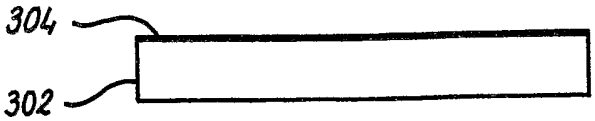

FIG. 1A

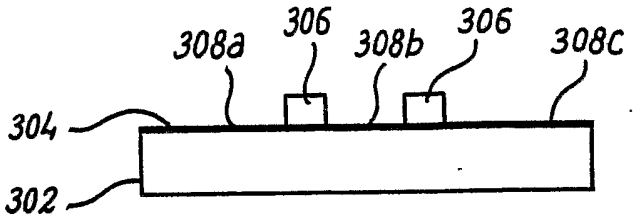

FIG. 1B

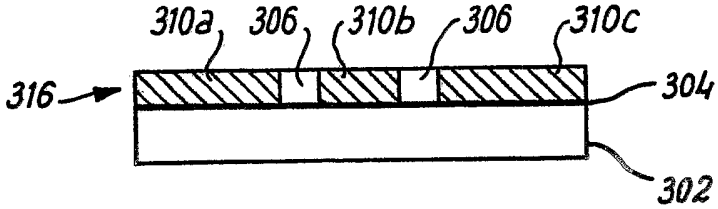

FIG. 1C

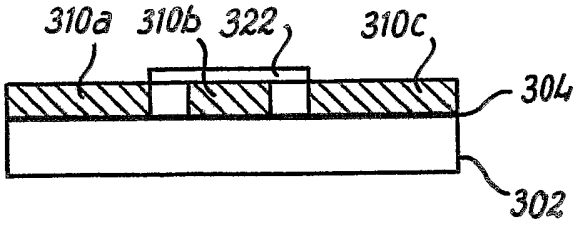

FIG. 1D

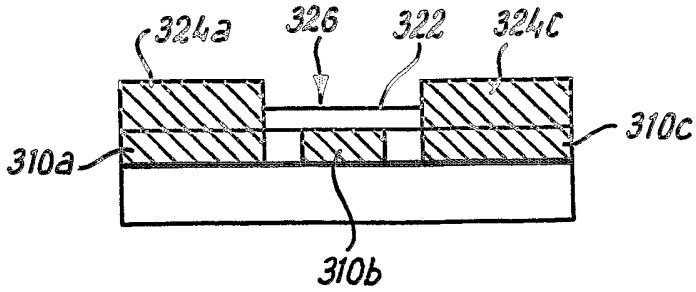

FIG. 1E

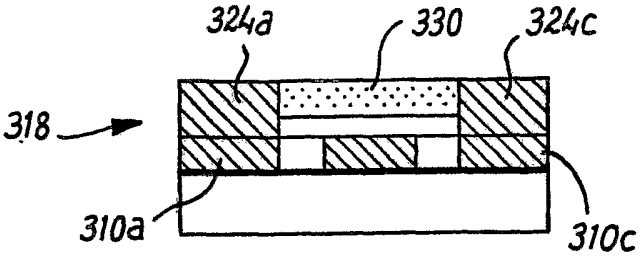

FIG. 1F

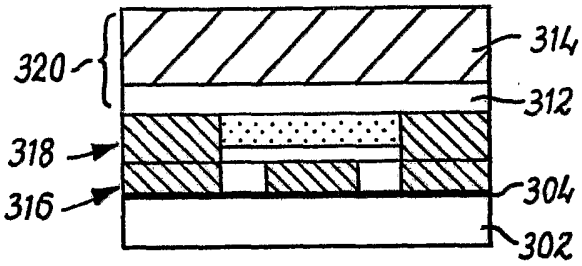

FIG. 1G

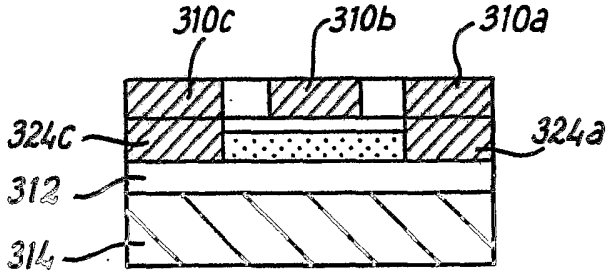

FIG. 1H

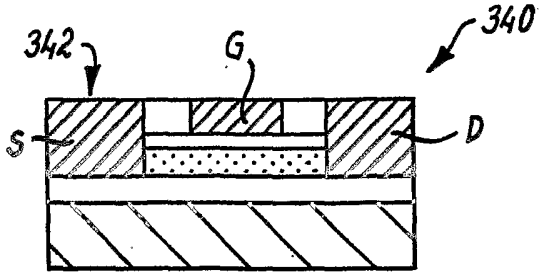

FIG. 2