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(54) **Title**: A READ-OUT INTERFACE CIRCUIT (ROIC)

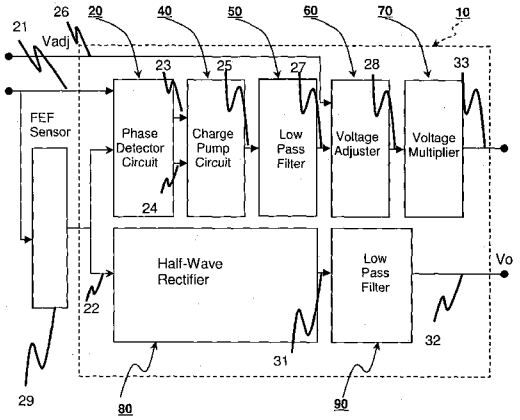


Figure 1

(57) **Abstract**: A read-out interface circuitry (ROIC) (10) connectable to a sensor (29) is provided, the ROIC (10) includes at least one phase detector circuit (20) to compare phase difference between an input reference signal and an output signal from the sensor (29), and at least one charge pump circuit (40) connectable to the at least one phase detector circuit (20) wherein an output of the at least one charge pump circuit (40) is convertible to a direct current (DC) voltage.

A READ-OUT INTERFACE CIRCUIT (ROIC)

FIELD OF INVENTION

The present invention relates to a read-out interface circuitry (ROIC) for humidity sensor, and more specifically for Fringing Electric Field (FEF) sensor in precision agriculture monitoring application.

BACKGROUND OF INVENTION

Commonly used methods for capacitive sensor readout circuitry is by converting capacitance to voltage using a switch capacitor circuit.

U.S. 7,032,448 B2 describes a capacitive humidity sensor with a detection portion and a reference portion that uses electrodes and sensitive film to accomplish its purpose. The described prior art detects humidity by converting a capacitance difference into a voltage signal. However, the drawback of the prior art is that, in applications such as soil moisture sensor systems, a wide range of capacitance with high resolution would be required. Therefore, the circuitry in prior art may become complex and require more space. This will not be ideal in systems that require a small footprint, especially in soil moisture sensor systems.

In other known systems, read out interface circuitry is only able to be integrated with a fixed resolution of analog to digital converters (ADC). This will restrict applications of said circuitry to only those ADC which are compatible at a fixed resolution.

Thus there is a need to provide for a solution that allows readings from a sensor to be captured and processed at any resolution, which does not limit applications where the solution may be applied.

SUMMARY OF INVENTION

Accordingly there is provided a read-out interface circuitry (ROIC) connectable to a sensor, the ROIC includes at least one phase detector circuit to compare phase difference between an input reference signal and an output signal from the sensor and at least one charge pump circuit connectable to the at least one phase detector circuit wherein an output of the at least one charge pump circuit is convertible to a direct current (DC) voltage.

The present invention consists of several novel features and a combination of parts hereinafter fully described and illustrated in the accompanying description and drawings, it being understood that various changes in the details may be made without departing from the scope of the invention or sacrificing any of the advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

Figure 1 illustrates a block diagram showing the architecture of an embodiment of a read-out interface circuitry (ROIC) in the present invention;

Figure 2 illustrates a schematic diagram showing the phase detector circuit in the embodiment of the present invention;

Figure 3 illustrates a schematic diagram showing the charge pump circuit in the embodiment of the present invention;

Figure 4 illustrates a schematic diagram of the first low pass filter in the embodiment of the present invention;

Figure 5 illustrates a schematic diagram of the voltage adjuster circuit in the embodiment of the present invention;

Figure 6 illustrates a schematic diagram of the voltage multiplier circuit in the embodiment of the present invention; and

Figure 7 illustrates a schematic diagram of the half wave rectifier and a second low pass filter in the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention relates to a read-out interface circuitry (ROIC). Hereinafter, this specification will describe the present invention according to the preferred embodiment of the present invention. However, it is to be understood that limiting the description to the preferred embodiment of the invention is merely to facilitate discussion of the present invention and it is envisioned that those skilled in the art may devise various modifications and equivalents without departing from the scope of the appended claims.

The following detailed description of the preferred embodiment will now be described in accordance with the attached drawings, either individually or in combination.

The present invention provides for a read-out interface circuitry (ROIC) (10) for humidity sensor, and more specifically for Fringing Electric Field (FEF) sensor (29) in precision agriculture monitoring application. Figure 1 depicts a block diagram of the ROIC (10) which includes at least one phase detector circuit (20) for comparing phase difference between an input reference signal and an output reference signal from the FEF sensor (29). At least one half-wave rectifier circuit (80) wherein the amplitude detector circuit detects amplitude of the output signal from the FEF sensor (29). At least one charge pump circuit (40) is further connectable to the at least one phase detector circuit (20). Output of the at least one charge pump circuit (40) is further convertible to a direct current (DC) voltage.

The charge pump circuit (40) is further connectable to a first low pass filter (50). The first low pass filter (50) is then connectable to a voltage adjuster circuit (60) which is further connectable to an analog multiplexer to produce a predetermined voltage. The

voltage adjuster circuit (60) and the voltage multiplier circuit (70) function together to tune output voltage range of the ROIC (10). The voltage multiplier circuit (70) is integrable with an analog to digital converter (ADC) of any resolution. The FEF sensor (29) is connectable to a half wave rectifier (80) which is further connectable to a second low pass filter (90).

The phase detector circuit (20) is a phase frequency detector which leads to an accuracy level of 0.1° or 5 nanoseconds (ns) in detectable phase difference. Use of the charge pump circuit (40) allows the output of the FEF sensor (29) to be linearized. Power consumption of the ROIC (10) is reduced in idle mode due to the use of the charge pump circuit (40) in idle mode. The functions of the voltage adjuster circuit (60) and the voltage multiplier circuit (70) are to widen phase detection range in the ROIC (10) and to amplify the output voltage.

The half wave rectifier (80) is used to extract a magnitude of the output signal from the FEF sensor (29). The half wave rectifier (80) is used in combination with a second low pass filter (90) for DC-level extraction.

Figure 2 shows a schematic design of the phase detector circuit (20) which is a frequency mixer or analog multiplier circuit. The ROIC (10) utilizes the phase detector circuit (20) to produce an output voltage proportional to frequency differences or phase differences of two input signals. Accordingly, the phase detector circuit (20) in this embodiment detects any phase difference found between the output signal from the FEF sensor (29) and the input reference signal. An advantage of the phase detector circuit (20) over existing XOR circuit used in prior art is that the present embodiment of the invention produces less noise. Spur noise produced by an XOR based phase

detector is double than that of a phase detector circuit (20) employed in the ROIC (10). A reduction of up to 50% is observed in the present embodiment of the invention.

In this embodiment, the ROIC (10) is used to calculate a percentage of volumetric water content (%VW) from output of the FEF sensor (29). A formula as seen below is used to calculate the percentage of volumetric water content (%VW):

$$\%VWC = 30.215C_x^3 + 847.81C_x^2 + 7975.2\,C_x + 25156$$

Wherein,

$$C_x = c_1 \left[\frac{V_o}{\omega R_L (V_o - V_i)} \right] \sin \varnothing + c_o$$

$\varnothing$ = Phase different input and output voltage from the FEF sensor (20).

V_o = Ouput voltage which is detected from the FEF sensor (20) in rms (root-mean square) value.

V_i = Input voltage which is biased into the FEF sensor (20)in rms value.

R_L = Load resistor equals to 100K Ohm.

c_1 and c_0 = Correction factor.

Figure 3 shows a schematic diagram of the charge pump circuit (40). The charge pump circuit (40) controls current flow within the ROIC (10). The charge pump circuit (40) generates positive current levels in response to "HIGH" signal level from the phase detector (23) levels and generates negative current levels in response to "LOW" signal level from the phase detector (23). The charge pump circuit (40) then provides a net current which is then converted to an equivalent DC voltage by the first low pass filter (50). It is to be appreciated that each DC voltage corresponds to a predetermined phase difference. Power down switches (41) control current to charge pump circuit

(40). The power down switches (41) help control circuit power consumption by allowing current to flow into the charge pump circuit (41) when current is needed.

The first low pass filter (50) is used to suppress noise levels within the ROIC (10). An example of the first low pass filter (50) is a first order loop filter as seen in Figure 4. The first order loop filter extracts a DC level from an alternating current (AC) signal. The DC level of a first order loop filter carries phase difference values and output signal amplitude.

As seen in Figure 5, a voltage adjuster circuit (60) is used to adjust DC voltage level from the first order loop filter. A plurality of voltage sources are connectable to an analog multiplexer wherein a predetermined voltage is derived by selecting a combination of inputs S0, S1 and S2 as seen in Figure 5. Resistors (R1, R2, R3, R4) must be of an equal value.

Figure 6 shows a voltage multiplier circuit (70). A variable resistor (R6) is included in the voltage multiplier circuit (70), which is the voltage varying element. Tuning of the variable resistor (R6) enables a multiplying factor to be changed. This feature enables the ROIC (10) to be integrable with an analog-to-digital converter (ADC) of any resolution.

Figure 7 depicts a half wave rectifier (80) schematic wherein the half wave rectifier (80) is used to extract magnitude of an output signal from the FEF sensor (29). The half wave rectifier (80) is used in combination with a second low-pass filter (90) for DC level extraction.

The ROIC (10) uses phase detection to compare phase differences between a FEF sensor (29) and a reference signal (21). Half-wave rectifier circuitry (80) is used to sense output voltage from the FEF sensor (29). A power down mode in charge pump circuit (40) helps to significantly reduce the ROIC (10) power consumption. Tuning and amplifying circuits are used to adjust output voltage levels and amplify a signal to a range that can be detected by a selected ADC. This increase flexibility is an improvement over existing ROIC capabilities as it can be easily integrated with any ADC regardless of the ADC resolution, depending on application it is intended for.

Therefore, the invention is suitable for use in applications such as, but not restricted to, any sensor system that requires capturing electrical signals generated by sensors and integrating with any ADC with a variety of resolutions.

CLAIMS

1. A read-out interface circuitry (ROIC) (10) connectable to a sensor (29), the ROIC (10) includes:
   i. at least one phase detector circuit (20) to compare phase difference between an input reference signal and an output signal from the sensor (29); and
   ii. at least one charge pump circuit (40) connectable to the at least one phase detector circuit (20);
   wherein an output of the at least one charge pump circuit (40) is convertible to a direct current (DC) voltage.

2. The ROIC (10) as claimed in claim 1, wherein the charge pump circuit (40) is further connectable to a first low pass filter (50).

3. The ROIC (10) as claimed in claim 1, wherein the low pass filter (50) is connectable to a voltage adjuster circuit (60) which is further connectable to an analog multiplexer to produce a predetermined voltage.

4. The ROIC (10) as claimed in claim 3, wherein the voltage adjuster circuit (60) is connectable to a voltage multiplier circuit (70) to tune output voltage range.

5. The ROIC (10) as claimed in claim 1, wherein the sensor (29) is connectable to a half wave rectifier (80).

6. The ROIC (10) as claimed in claim 5, wherein the half wave rectifier (80) is connectable to a second low pass filter (90).

7. The ROIC (10) as claimed in claim 4, wherein the voltage multiplier circuit (70) is integrable with an analog to digital converter (ADC) of any resolution.

8. The ROIC (10) as claimed in claim 1, wherein the phase detector circuit (20) is a phase detector circuit (20).

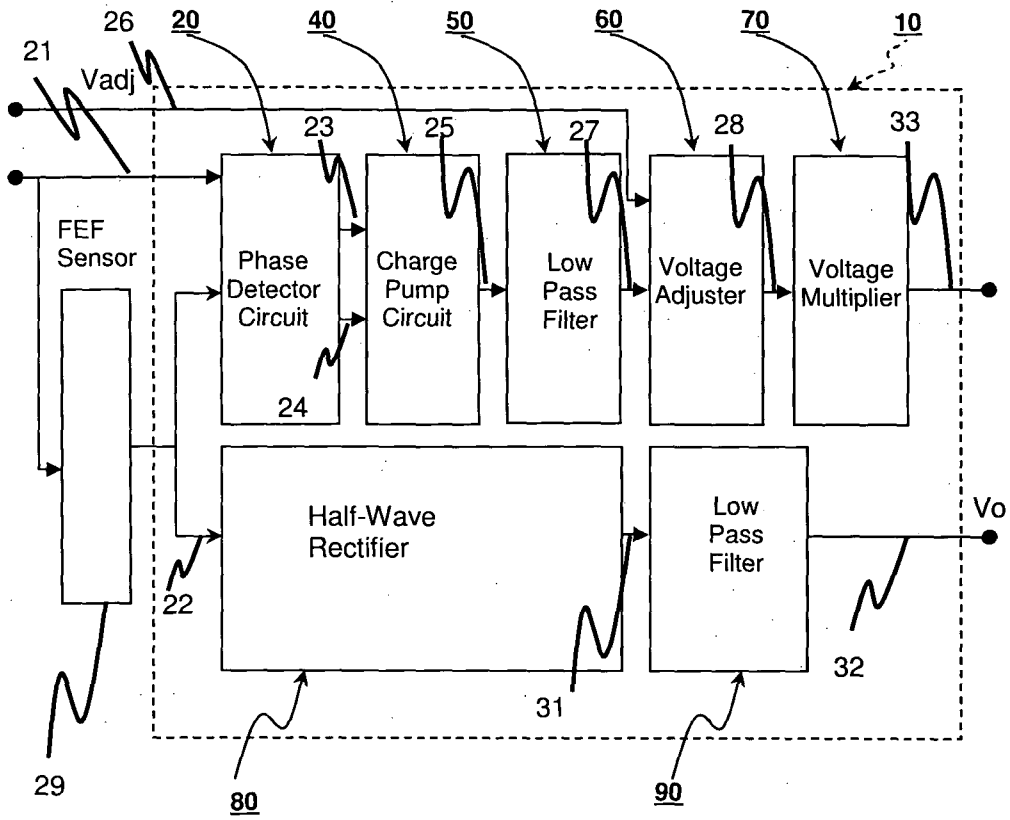
9. The ROIC (10) as claimed in claim 1, wherein the sensor (29) is a Fringing Electric Field (FEF) sensor.

10. The ROIC (10) as claimed in claim 1, wherein the charge pump circuit (40) linearizes the output of the sensor (29).

11. The ROIC (10) as claimed in claim 1, wherein the charge pump circuit (40) reduces power consumption of the ROIC (10) in idle mode.

12. The ROIC (10) as claimed in claim 1, wherein the ROIC (10) is used with humidity sensors.

13. The ROIC (10) as claimed in claim 1, wherein the ROIC (10) is used in precision agriculture monitoring applications.


26
20
40
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23
25
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Figure 1

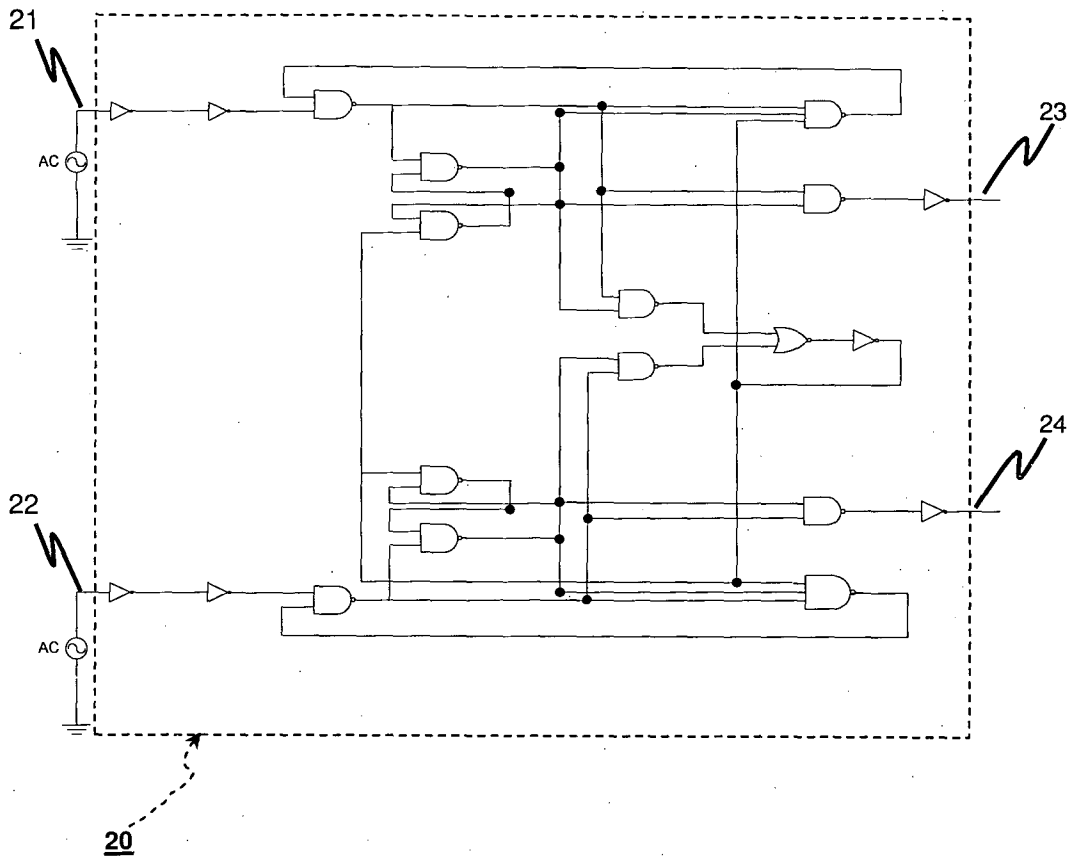

Figure 2

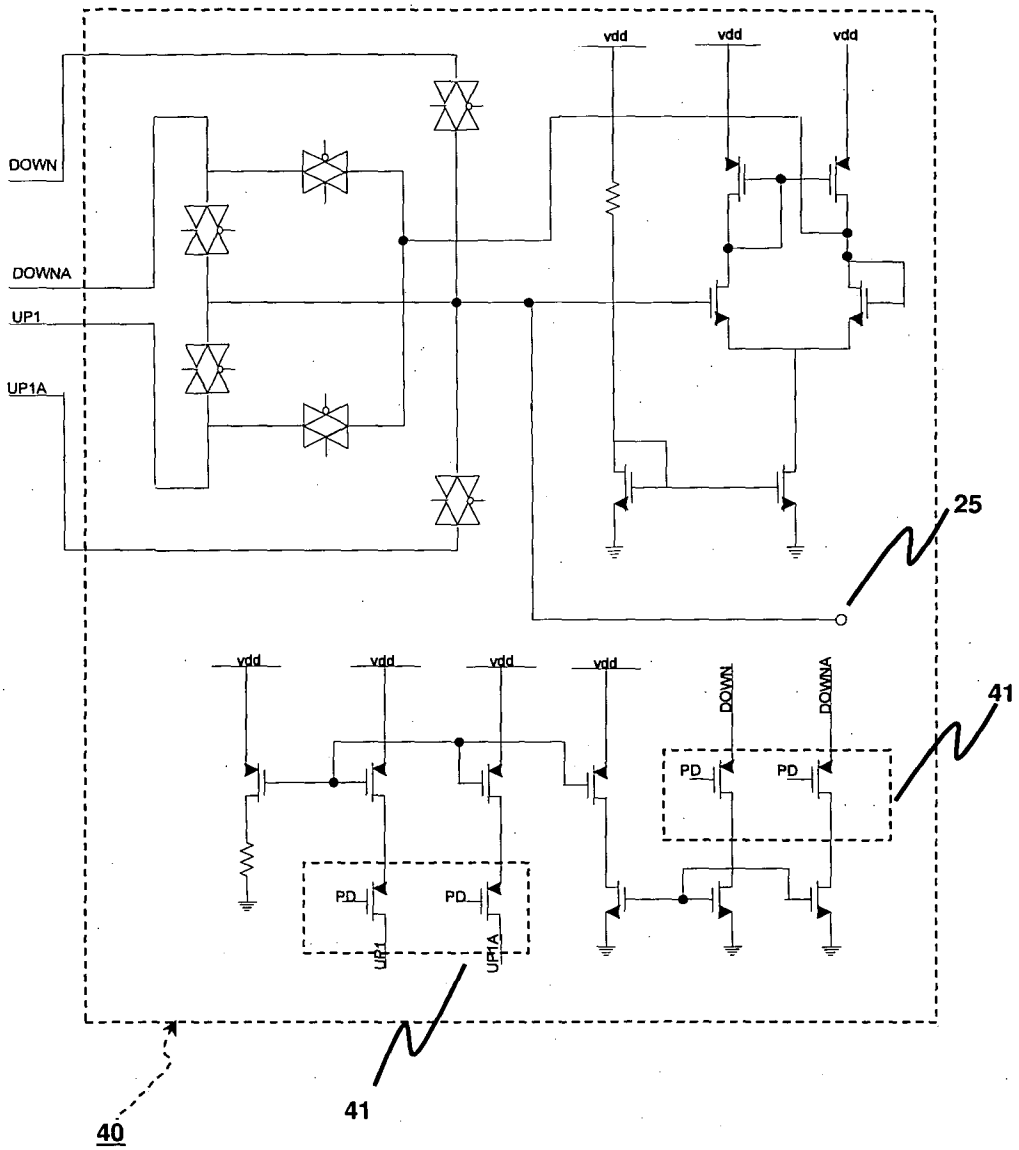
vdd
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Figure 3

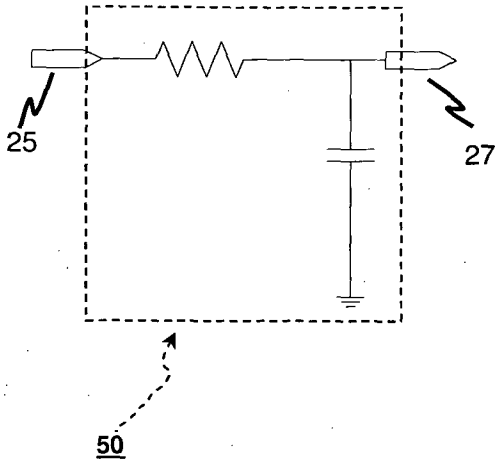

Figure 4

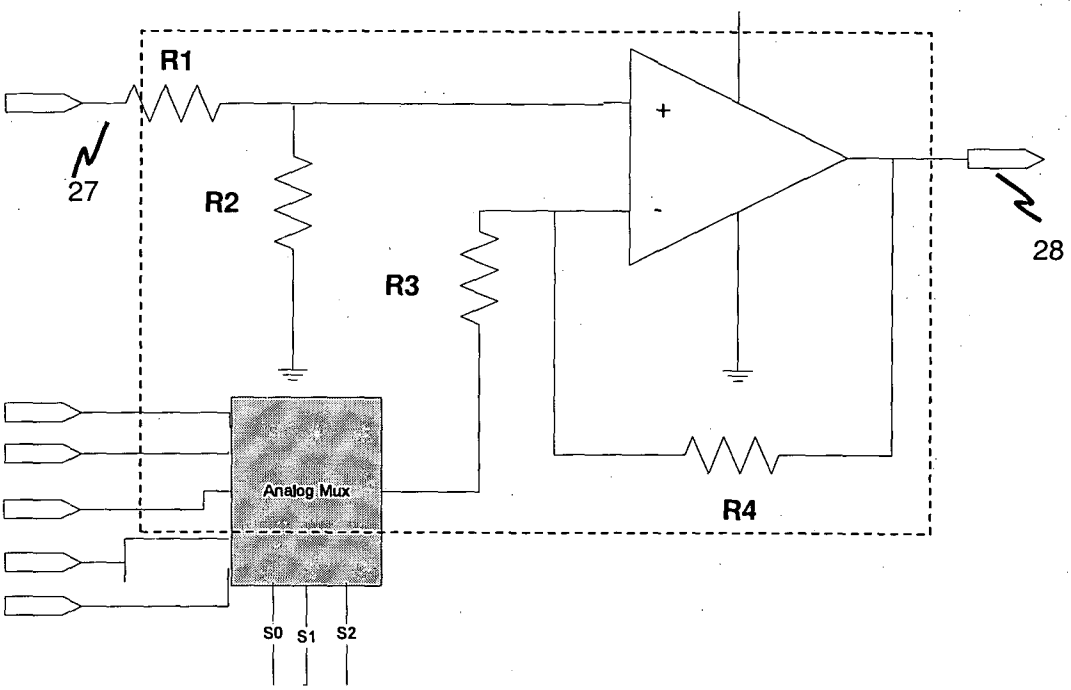

Figure 5

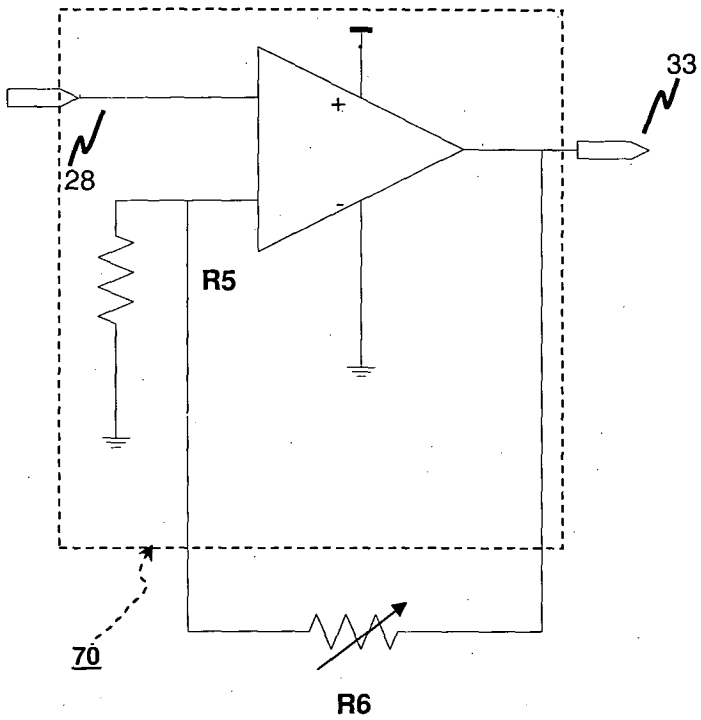

Figure 6

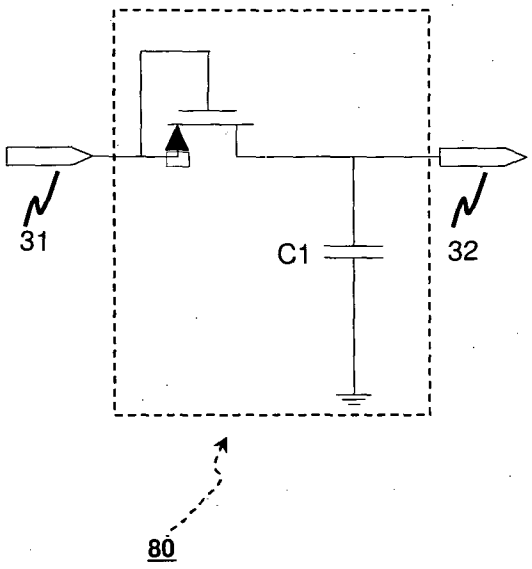

Figure 7