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(54) **METHODS FOR ETCHING HIGH ASPECT RATIO FEATURES**

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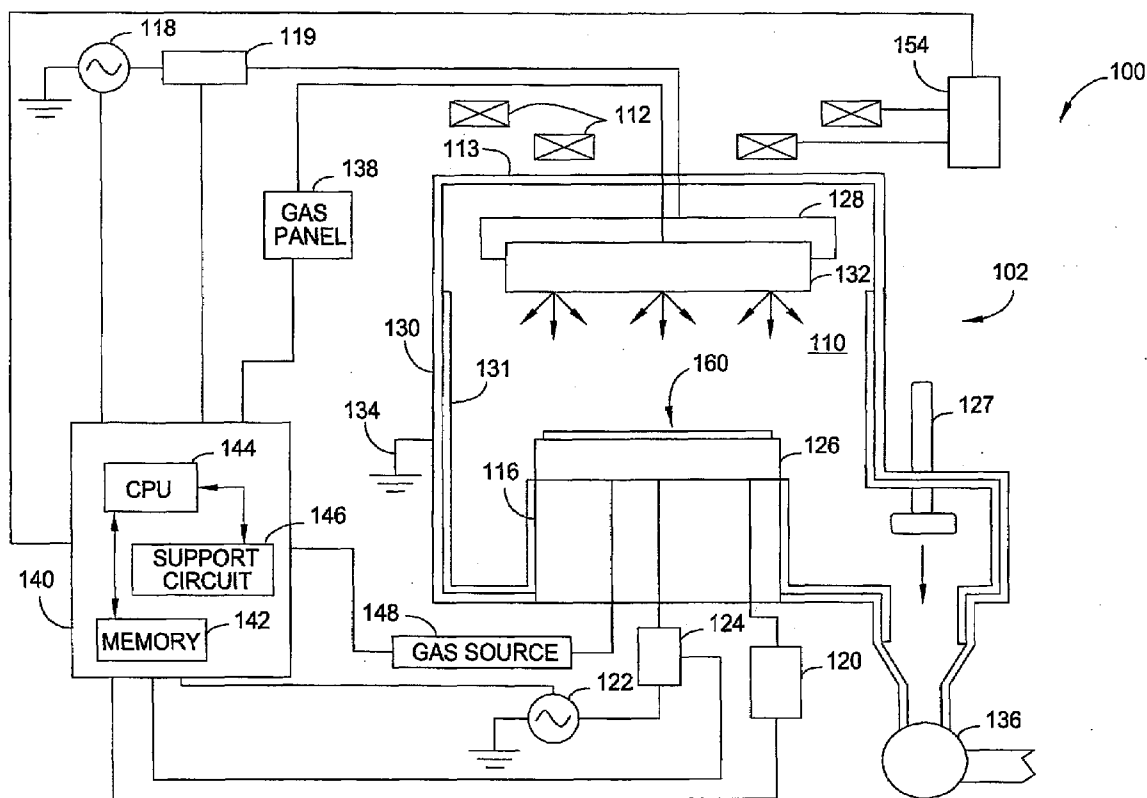
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(57) **ABSTRACT**

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Methods for forming features for high aspect ratio application in etch process are provided in the present invention. In one embodiment, the method for etching a dielectric layer disposed on a substrate includes placing a substrate having a portion of a dielectric layer exposed through a patterned photoresist layer in an etch chamber, supplying a gas mixture containing argon (Ar) gas into the etch chamber, forming a plasma from the gas mixture using dual frequency RF power and etching the exposed dielectric layer using the plasma formed from the gas mixture.

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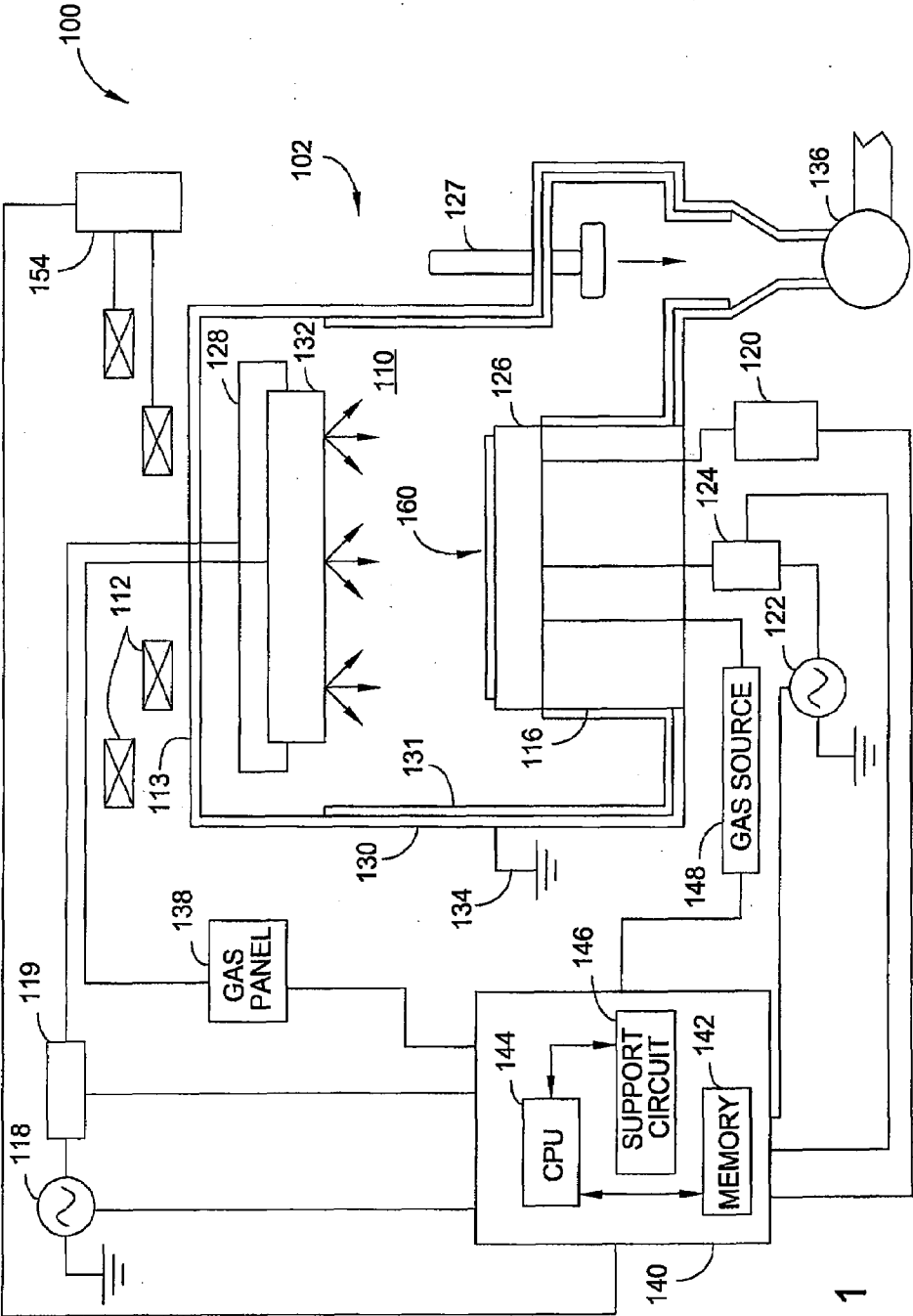


FIG. 1

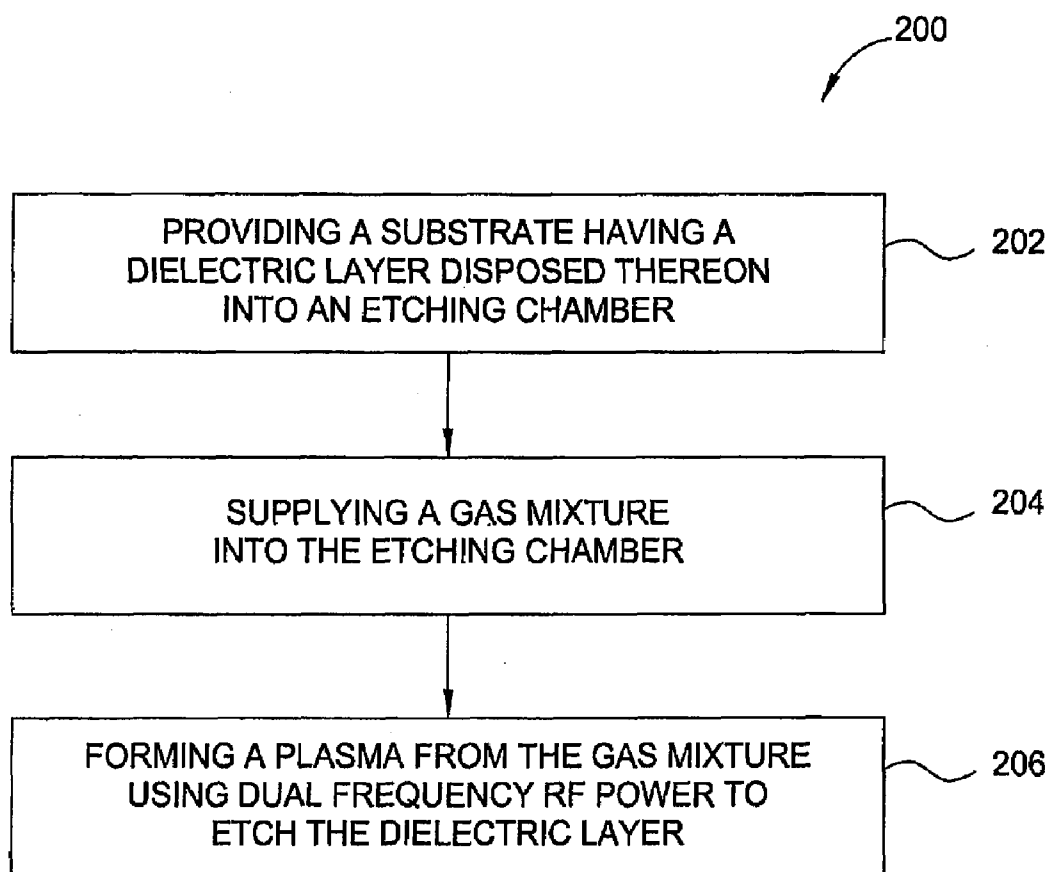
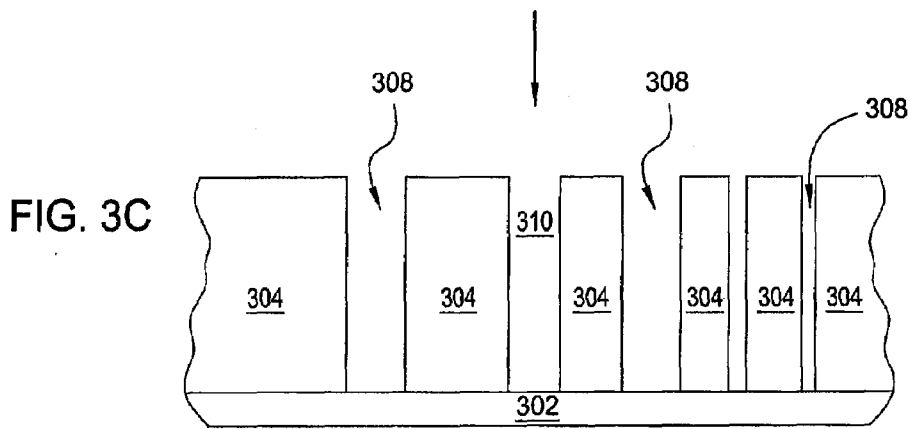
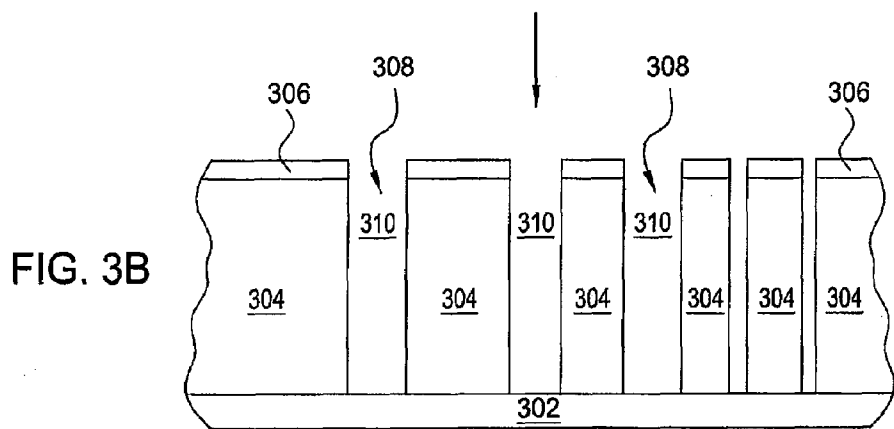
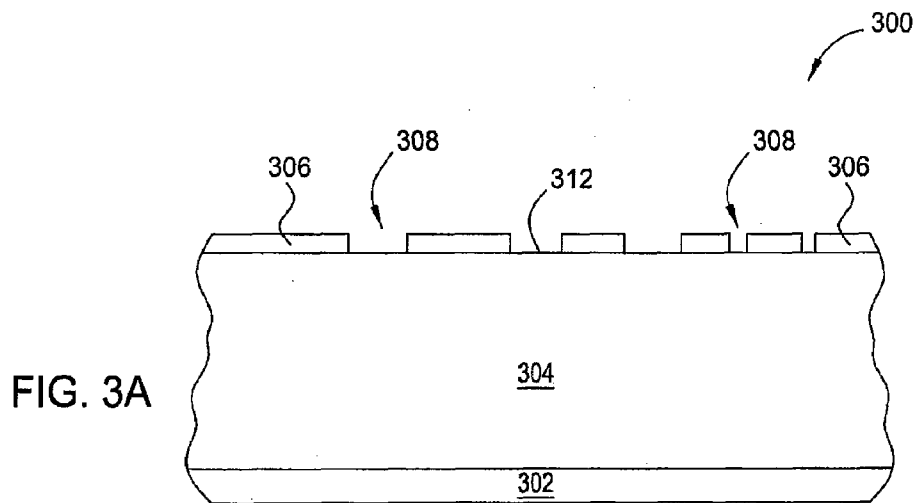


FIG. 2



## METHODS FOR ETCHING HIGH ASPECT RATIO FEATURES

### BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention generally relates to methods for etching high aspect ratio features on a substrate. More specifically, the present invention generally relates to methods of etching high aspect ratio features in a dielectric layer disposed on a substrate.

[0003] 2. Description of the Related Art

[0004] Reliably producing sub-half micron and smaller features is one of the key technologies for the next generation of very large scale integration (VLSI) and ultra large-scale integration (ULSI) of semiconductor devices. However, as the limits of circuit technology are pushed, the shrinking dimensions of interconnects in VLSI and ULSI technology have placed additional demands on processing capabilities. Reliable formation of a gate pattern is important to VLSI and ULSI success and to the continued effort to increase circuit density and quality of individual substrates and die.

[0005] As the feature sizes have become smaller, the aspect ratio, or the ratio between the depth and width of a feature has steadily increased, such that manufacturing processes are now being required to etch features into materials having aspect ratios of up to 10:1 and even greater. As the aspect ratio of features has increased, feature profile and/or spacing uniformity has become increasingly harder to control. Double or multiple sloped profiles become increasingly present at higher aspect ratios, thus causing poor control of the feature critical dimensions.

[0006] Conventionally, features having aspect ratios of about 5:1 and higher are produced by anisotropic plasma etching. Anisotropic plasma etching has been shown to minimize undercutting while retaining critical dimensions of the features by producing straighter sidewalls and flatter bottoms. Geometry of critical dimension (CD) of the top and bottom, profile angle, bowing and necking, of the features, such as contact/via holes are highly associated with the plasma properties present during an etching process. Changes in the plasma properties during an etch process may result from changes in plasma chemistries, dissociated ion plasma flux, ion energy distributions across the substrate and the like. During high aspect ratio etching, the plasma properties may vary resulting in a variance in the profiles formed and/etched on the features. Profile deformation (e.g., bowing, necking, or tapered top) may limit the etching rate, thereby causing a gradually slowing of the etch rate over the course of etching. The gradually slowing etch rate eventually leads to either an etch stop or taper profile of the features formed on the substrate. Thus, process challenges must still be overcome in order to effectively etch high aspect ratio features to enable next generation devices.

[0007] Therefore, there is a need for an improved method for etching features with high aspect ratios.

### SUMMARY OF THE INVENTION

[0008] Methods for etching high aspect ratio features are provided. The methods described herein advantageously facilitate profile and dimension control of high aspect ratio features while maintaining good etching rate. In one embodiment, a method for etching a dielectric layer disposed on a substrate includes placing a substrate having a portion of a

dielectric layer exposed through a patterned photoresist layer in an etch chamber, supplying a gas mixture containing an inert gas into the etch chamber, forming a plasma from the gas mixture using dual frequency RF power, and etching the exposed dielectric layer using the plasma formed from the gas mixture.

[0009] In another embodiment, a method for etching a dielectric layer disposed on a substrate includes placing a substrate having a portion of a dielectric layer exposed through a patterned photoresist layer in an etch chamber, supplying a gas mixture containing argon (Ar) gas at a flow rate between about 5 sccm and about 250 sccm into the etch chamber, forming a plasma from the gas mixture using dual frequency RF power, and etching the exposed dielectric layer using the plasma formed from the gas mixture.

[0010] In yet another embodiment, a method for etching a dielectric layer disposed on a substrate includes placing a substrate having a portion of a dielectric layer exposed through a patterned photoresist layer in an etch chamber, supplying a gas mixture containing a carbon fluorine containing gas, an oxygen containing gas and argon (Ar) gas into the etch chamber, wherein the Ar gas flow is maintained between about 5 sccm and about 250 sccm, forming a plasma from the gas mixture using dual frequency RF power, and etching the exposed dielectric layer using the plasma formed from the gas mixture.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

[0012] FIG. 1 is a schematic diagram of a plasma processing apparatus that may be used to practice an etching process according to one embodiment of the invention;

[0013] FIG. 2 is a process flow diagram illustrating one embodiment of an etch process of the invention; and

[0014] FIGS. 3A-3C are sequential cross-sectional views of a substrate having a dielectric layer disposed thereon etched according to the process of FIG. 2.

[0015] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

[0016] It is to be noted, however, that the appended drawings illustrate only exemplary embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

### DETAILED DESCRIPTION

[0017] The invention generally relates to methods for forming high aspect ratio features in dielectric layers by an etch process. In one embodiment, the method includes using a dual frequency plasma formed from a gas mixture having a low inert gas flow to etch a high aspect ratio feature in a dielectric layer disposed on a substrate.

[0018] The etch process described herein may be performed in any suitably adapted plasma etch chamber, for example, an eMAX® etch reactor, an eMAX® CT plus, a MERIE® etch reactor, a HART® etch reactor, a HARE® TS etch reactor, a Decoupled Plasma Source (DPS®), DPS®-II,

or DPS® Plus, or DPS® DT etch reactor of a CENTURA® etch system, all of which are available from Applied Materials, Inc. of Santa Clara, Calif. Other suitable plasma etch chambers, including those from other manufacturers, may also be utilized.

[0019] FIG. 1 depicts a schematic cross-sectional view of one embodiment of a plasma etch chamber 102 suitable for performing one or more steps of the invention. The plasma etch chamber 102 may include a process chamber 110 having a conductive chamber wall 130 and a lid 113. The temperature of the conductive chamber wall 130 is controlled using liquid-containing conduits (not shown) that are located in and/or around the conductive chamber wall 130. The conductive chamber wall 130 is connected to an electrical ground 134. A liner 131 is disposed in the process chamber 110 to cover the interior surfaces of the conductive chamber wall 130. The liner 131 serves as a surface protection layer that protects the interior surface of the chamber wall 130 of the process chamber 110. In one embodiment, the liner 131 may be fabricated by ceramic materials including Al<sub>2</sub>O<sub>3</sub>, AlN, silicon carbide, Y<sub>2</sub>O<sub>3</sub>, and the like.

[0020] The process chamber 110 is a vacuum vessel that is coupled through a throttle valve 127 to a vacuum pump 136. A support pedestal 116 is disposed in the bottom of the process chamber 110 to support a substrate 160 positioned thereon. The support pedestal 116 may include an electrostatic chuck 126 for retaining the substrate 160. A DC power supply 120 is utilized to control the power supplied to the electrostatic chuck 126. The support pedestal 116 is coupled to a radio frequency (RF) bias power source 122 through a matching network 124. The bias power source 122 is generally capable of producing an RF signal having a tunable frequency of from about 50 kHz to about 60 MHz, and a bias power of about 0 to about 5,000 Watts. The bias power source 122 may provide a signal at multiple frequencies, such as about 13.6 MHz and about 2 MHz. Optionally, the bias power source 122 may be a DC or pulsed DC source.

[0021] The temperature of the substrate 160 is at least partially controlled by regulating the temperature of the support pedestal 116. In one embodiment, the support pedestal 116 includes a cooling plate (not shown) having channels for flowing a coolant. In addition, a backside gas, such as helium (He) gas, provided from a gas source 148, fits provided into channels disposed between the back side of the substrate 160 and grooves (not shown) formed in the surface of the electrostatic chuck 126. The backside gas provides efficient heat transfer between the pedestal 116 and the substrate 160. The electrostatic chuck 126 may also include a resistive heater (not shown) disposed within the chuck 126 to heat the substrate 160 during processing. In one embodiment, the substrate 160 is maintained at a temperature of between about 10 to about 500 degrees Celsius during processing.

[0022] A showerhead 132 is mounted to a lid 113 of the process chamber 110 in a spaced-apart relation to the substrate pedestal 116 facing toward the substrate 160. A gas panel 138 is fluidly coupled to a plenum (not shown) defined between the showerhead 132 and the lid 113. The showerhead 132 includes a plurality of holes to allow gases provided to the plenum from the gas panel 138 to enter the process chamber 110. The holes in the showerhead 132 may be arranged in different zones such that various gases can be released into the chamber 110 with different volumetric flow rates.

[0023] The showerhead 132 and/or an upper electrode 128 positioned proximate thereto is coupled to a RF plasma power

source 118 through an impedance transformer 119 (e.g., a quarter wavelength matching stub). The RF power source 118 is generally capable of producing an RF signal having a tunable frequency of about 50 kHz to about 160 MHz and a source power of about 0 to about 5,000 Watts. The RF plasma power source 118 may provide a signal at multiple frequencies, such as about 13.6 MHz or about 2 MHz.

[0024] The chamber 102 may also include one or more coil segments or magnets 112 positioned exterior to the chamber wall 130, near the chamber lid 113. Power to the coil segment (s) 112 is controlled by a DC power source or a low-frequency AC power source 154.

[0025] During substrate processing, gas pressure within the interior of the chamber 110 is controlled using the gas panel 138 and the throttle valve 127. In one embodiment, the gas pressure within the interior of the chamber 110 is maintained at about 0.1 to about 999 mTorr.

[0026] A controller 140, including a central processing unit (CPU) 144, a memory 142, and support circuits 146, is coupled to the various components of the chamber 102 to facilitate control of the processes of the present invention. The memory 142 can be any computer-readable medium, such as random access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote to the chamber 102 or CPU 144. The support circuits 146 are coupled to the CPU 144 for supporting the CPU 144 in a conventional manner. These circuits include cache, power supplies, clock circuits, input/output circuitry and subsystems, and the like. A software routine or a series of program instructions stored in the memory 142, when executed by the CPU 144, causes the chamber 102 to perform an etch process of the present invention.

[0027] FIG. 1 only shows one exemplary configuration of various types of plasma etching chambers that can be used to practice the invention. For example, different types of source power and bias power can be coupled into the plasma chamber using different coupling mechanisms. Using both the source power and the bias power allows independent control of a plasma density and a bias voltage of the substrate with respect to the plasma. In some applications, the source power may not be needed and the plasma is maintained solely by the bias power. The plasma density can be enhanced by a magnetic field applied to the vacuum chamber using electromagnets, such as the magnets 112, driven with a low frequency (e.g., 0.1-0.5 Hertz) AC current source or a DC source. In other applications, the plasma may be generated in a different chamber from the one in which the substrate is located, e.g., remote plasma source, and the plasma subsequently guided into the chamber using techniques known in the art.

[0028] FIG. 2 illustrates a flow diagram of one embodiment of an etching process 200 utilized to etch an exposed portion of a dielectric layer disposed on a substrate according to one embodiment of the invention. FIGS. 3A-3C are schematic cross-sectional views illustrating the sequence of the dielectric layer etching process 200. The process 200 may be stored in memory 142 as instructions that when executed by the controller 140 cause the process 200 to be performed in the chamber 102.

[0029] The process 200 begins at step 202 by providing a substrate 302 having a dielectric layer 304 disposed thereon into an etching chamber, such as the etching chamber 102 as described in FIG. 1. The dielectric layer 304 disposed on the substrate 302, as shown in FIG. 3A, has a thickness sufficient to be etched and formed high aspect ratio feature therein. In

one embodiment, the thickness may be between about 0.5  $\mu\text{m}$  and 4  $\mu\text{m}$  to form features having aspect ratio between about 1:5 and about 1:100, for example about 1:5 and about 1:50, such as greater than about 1:10.

**[0030]** In one embodiment, the dielectric layer **304** may be silicon dioxide, boron-doped oxide (BSG), organosilicate, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), fluorine doped silicon oxide (FSG), tetraethoxysilane (TEOS), carbon doped silicon oxide (SiOC) or BLACK DIAMOND<sup>®</sup> dielectric material (all available from Applied Materials, Inc). The dielectric layer **304** may be formed using any suitable depositions techniques, such as atomic layer deposition (ALD), cyclical layer deposition (CLD), physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), evaporation, and the like.

**[0031]** The substrate **302** may be a material such as crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped silicon wafers and patterned or non-patterned wafers silicon on insulator (SOI), carbon doped silicon oxides, silicon nitride, doped silicon, germanium, gallium arsenide, glass, sapphire. The substrate **302** may have various dimensions, such as 200 mm or 300 mm diameter wafers, as well as, rectangular or square panes. Unless otherwise noted, embodiments and examples described herein are conducted on substrates having a 200 mm diameter or a 300 mm diameter.

**[0032]** In one embodiment, the substrate **302** and the dielectric layer **304** disposed thereon may be utilized to form high aspect ratio contact holes/vias in the interlayer dielectric connection (ILD). In another embodiment, the substrate **302** and the dielectric layer **304** disposed thereon may be utilized to form high aspect ratio contact holes/vias of greater than about 1:10 in the interlayer dielectric connection (ILD). In the embodiment depicted in FIG. 3A, a surface **312** of the dielectric layer **304** is exposed through an opening **308** defined by a patterned photoresist layer **306**.

**[0033]** At step **204**, a gas mixture is supplied into the etching chamber **102**. The gas mixture includes a relatively low amount of inert gas flow. The inert gas may be selected from a group consisting of argon gas (Ar), helium gas (He), nitric oxide (NO), carbon monoxide (CO), nitrous oxide (N<sub>2</sub>O), oxygen gas (O<sub>2</sub>), nitrogen gas (N<sub>2</sub>) and the like. In one embodiment, the inert gas is argon gas (Ar). In one embodiment, the Ar inert gas may be supplied into the etching chamber at a gas flow rate of less than about 250 sccm, such as less than about 200 sccm. In another embodiment, the Ar inert gas may be supplied into the etching chamber at a rate between about 5 sccm and about 250 sccm, such as between about 15 sccm and about 200 sccm, for example, about 50 sccm.

**[0034]** The gas mixture may include, but is not limited to, a carbon fluorine containing gas and at least an oxygen containing gas. Suitable examples of carbon fluorine containing gas may include, but not limited to, CH<sub>2</sub>F<sub>2</sub>, CHF<sub>3</sub>, CH<sub>3</sub>F, C<sub>2</sub>F<sub>6</sub>, CF<sub>4</sub>, C<sub>3</sub>F<sub>8</sub>, C<sub>4</sub>F<sub>6</sub>, C<sub>4</sub>F<sub>8</sub>, and the like. Suitable examples of oxygen containing gas may include, but not limited to, nitric oxide (NO), carbon monoxide (CO), nitrous oxide (N<sub>2</sub>O), oxygen gas (O<sub>2</sub>), and the like. In the embodiment of present application, the gas mixture supplied into the etching chamber **102** at step **204** are C<sub>4</sub>F<sub>6</sub> and O<sub>2</sub> accompanying with low flow Ar inert gas.

**[0035]** In one embodiment suitable for etching the dielectric layer, the carbon fluorine containing gas may be supplied

into the etching chamber at a flow rate between about 200 sccm and about 2000 sccm, such as between about 300 sccm and about 1200 sccm, for example, about 500 sccm. The oxygen containing gas may be supplied into the etching chamber at a flow rate between about about 10 sccm and about 300 sccm, such as between about 20 sccm and about 200 sccm, for example, about 50 sccm.

**[0036]** Several process parameters of the gas mixture at step **204** are regulated while supplying into the etching chamber. In one embodiment, a pressure of the gas mixture in the etch chamber is regulated between about 10 mTorr to about 350 mTorr, for example, between about 20 mTorr to about 50 mTorr, and the substrate temperature is maintained between about -20 degrees Celsius and about 50 degrees Celsius, for example, between about -10 degrees Celsius and about 20 degrees Celsius.

**[0037]** At step **206**, a dual frequency RF power is utilized to energize the gas mixture into a plasma to etch the dielectric layer **304** through the openings **308** defined by the patterned photoresist layer **306**. The dual frequency RF power may be provided from the sources **118**, **122** singularly or in combination. The source **118** and/or sources **122** may provide one or both of the frequency components of the dual frequency. For example, the bias power source **122** may provide power at two or more frequencies while the power source **118** is off, and vice versa. In another example, the power source **118** may provide power at a first frequency while the bias power source provides power at a second frequency power used to energize the plasma. Some beneficial frequencies pairs include 2 and 13 MHz, 2 and 60 MHz, 13 and 60 MHz, 2 and 13 kHz, 2 and 60 kHz, and 13 and 60 kHz.

**[0038]** The dual frequency power plasma, along with the low inert gas flow, dissociates mainly the active etchants, such as carbon fluorine containing etchants, in the gas mixture and keeps the oxygen containing gas, such as O<sub>2</sub> gas, relatively insensitive to the plasma, thereby efficiently minimizing the polymerization produced by the recombination of ionized carbon and oxygen elements. The reduced polymerization prevents necking, clogging or deformation of the etched features which may eventually lead to etch stop, thereby enabling the etching process to continue until a desired depth and width of the features is reached. Additionally, the low inert gas flow allows the gas mixture to be carried into the chamber with low ion bombardment to the substrate, thereby preventing overetching or profile deformation on the etched features. The low inert gas flow also maintains high and intense active etchant densities without significantly diluting the gas mixture. The high and intense active etchant dissociation in the dual frequency plasma maintains a high etch rate without adversely effecting etching profiles in high aspect ratio applications.

**[0039]** A first RF power **118** may have a RF frequency between about 60 MHz and about 200 MHz to provide a plasma sufficient to dissociate the gas mixture. In one embodiment, the first RF power may have a RF frequency set at about 13.56 MHz. A second RF power **122** may have a RF frequency between about 2 MHz and about 14 MHz to provide a plasma toward the substrate surface, thereby assisting the dissociated gas species flowing deep into the high aspect ratio features formed on the substrate. In one embodiment, the second RF power may have a RF frequency set at about 2 MHz.

**[0040]** In one embodiment, a first RF power having a RF frequency about 13.56 MHz may be applied at a power of

about 50 Watts to about 4000 Watts along with a second RF power having a RF frequency about 2 MHz at a power of about 50 Watts to about 4000 Watts to provide a dual frequency plasma to the gas mixture to promote the high aspect ratio etching process. The etching time may be processed at between about 5 seconds to about 500 seconds.

**[0041]** In one embodiment, the first RF power provides a power at about 2000 Watts at a frequency of 13.56 MHz and the second RF power provides a power at about 2000 Watts at a frequency of 2 MHz to etch the dielectric layer **304**. The dielectric layer **304** may be a TEOS film or SiO<sub>2</sub> film. The gas mixture utilized to etch the TEOS film or SiO<sub>2</sub> film are C<sub>4</sub>F<sub>6</sub> gas, O<sub>2</sub> gas and low flow Ar gas. In one embodiment, the C<sub>4</sub>F<sub>6</sub> gas has a flow rate at about 500 sccm, and the O<sub>2</sub> gas has a flow rate at about 50 sccm. The Ar inert gas has a low gas flow at about 50 sccm. During etching, the gas pressure may be regulated at about 15 mTorr, and the substrate temperature may be maintained at between about 30 degrees Celsius.

**[0042]** The process of etching the dielectric layer **304** is terminated after reaching an endpoint signaling that the underlying substrate **302** has been exposed, as shown in FIG. 3B at that a desired depth has been etched into the dielectric layer **304**. The etching process defines a feature **310**, such as trench, or via, in the dielectric layer **304**. The endpoint may be determined by any suitable method. For example, the endpoint may be determined by monitoring optical emissions, expiration of a predefined time period or by another indicator for determining that the dielectric barrier layer **406** to be etched has been sufficiently removed. Optionally, as or after the feature **310** is formed in the dielectric layer **304** on the substrate **302**, the patterned photoresist layer **306** may be removed, as shown in FIG. 3C. In one embodiment, the photoresist layer **306** is removed by ashing or exposed to an oxygen containing plasma.

**[0043]** Thus, the present invention provides an improved method for etching features in a dielectric layer in high aspect ratio applications. The method described herein advantageously facilitates profile and dimension control of features with high aspect ratios and promotes the etching rate of the process through dual frequency plasma etching with low inert gas flow.

**[0044]** While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

**1.** A method for etching a dielectric layer disposed on a substrate, comprising:

placing a substrate having a portion of a dielectric layer exposed through a patterned photoresist layer in an etch chamber;

supplying a gas mixture containing an inert gas into the etch chamber;

forming a plasma from the gas mixture using dual frequency RF power; and

etching the exposed dielectric layer using the plasma formed from the gas mixture.

**2.** The method of claim **1**, wherein the step of supplying the gas mixture further comprises:

supplying a carbon fluorine containing gas and an oxygen containing gas into the etch chamber.

**3.** The method of claim **2**, wherein the carbon fluorine containing gas includes at least one of CH<sub>2</sub>F<sub>2</sub>, CHF<sub>3</sub>, CH<sub>3</sub>F, C<sub>2</sub>F<sub>6</sub>, CF<sub>4</sub>, C<sub>3</sub>F<sub>8</sub>, C<sub>4</sub>F<sub>6</sub> and C<sub>4</sub>F<sub>8</sub>.

**4.** The method of claim **2**, wherein the carbon fluorine containing gas is C<sub>4</sub>F<sub>6</sub>.

**5.** The method of claim **2**, wherein the oxygen containing gas includes at least one of nitric oxide (NO), carbon monoxide (CO), nitrous oxide (N<sub>2</sub>O), and oxygen gas (O<sub>2</sub>).

**6.** The method of claim **2**, wherein the oxygen containing gas is oxygen gas (O<sub>2</sub>).

**7.** The method of claim **2**, wherein the step of supplying further comprises:

supplying the carbon fluorine containing gas at a flow rate between about 200 sccm and about 2000 sccm; and

supplying the oxygen containing gas at a flow rate between about 20 sccm and about 200 sccm.

**8.** The method of claim **1**, wherein the inert gas is Ar and is supplied at a low flow rate between about 5 sccm and about 250 sccm.

**9.** The method of claim **1**, wherein the inert gas is Ar and is supplied at a flow rate less than 200 sccm.

**10.** The method of claim **1**, wherein the step of forming the plasma from the gas mixture using dual frequency RF power further comprises:

supplying a first RF power into the etching chamber; and

supplying a second RF power into the etching chamber.

**11.** The method of claim **10**, wherein the first RF power has a RF frequency about 13.56 MHz.

**12.** The method of claim **10**, wherein the second RF power has a RF frequency about 2 MHz.

**13.** The method of claim **10**, wherein the step of forming the plasma from the gas mixture using dual frequency RF power further comprises:

supplying the first RF power of about 50 Watts to about 4000 Watts; and

applying the second RF power of about 50 Watts to about 4000 Watts.

**14.** The method of claim **1**, wherein the dielectric layer includes at least one of silicon dioxide, boron-doped oxide (BSG), organosilicate, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), fluorine doped silicon oxide (FSG), tetraethoxysilane (TEOS) and carbon doped silicon oxide (SiOC).

**15.** The method of claim **1**, wherein the dielectric layer is tetraethoxysilane (TEOS).

**16.** The method of claim **1**, wherein the step of etching further comprises:

maintaining the process pressure at between about 10 mTorr and about 350 mTorr.

**17.** The method of claim **1**, wherein the formed features have an aspect ratio greater than 1:5.

**18.** The method of claim **1**, further comprising:

forming a feature in the dielectric layer having substantially straight sidewall and substantially flat bottom.

**19.** The method of claim **1**, further comprising:

forming a feature in the dielectric layer having substantially no profile deformation.

**20.** A method for etching a dielectric layer disposed on a substrate, comprising:

placing a substrate having a portion of a dielectric layer exposed through a patterned photoresist layer in an etch chamber;



supplying a gas mixture containing at least argon (Ar) gas at a flow rate between about 5 sccm and about 250 sccm into the etch chamber;

forming a plasma from the gas mixture using dual frequency RF power; and

etching the exposed dielectric layer using the plasma formed from the gas mixture.

**21.** The method of claim **20**, wherein the step of forming the plasma from the gas mixture using dual frequency RF power further comprises:

supplying a first RF power at a RF frequency at between about 13.56 MHz; and

supplying a second RF power at a RF frequency at between about 2 MHz.

**22.** The method of claim **20**, wherein the step of supplying the gas mixture further comprises:

supplying at least a carbon fluorine containing gas and an oxygen containing gas into the etch chamber.

**23.** A method for etching a dielectric layer disposed on a substrate, comprising:

placing a substrate having a portion of a dielectric layer exposed through a patterned photoresist layer in an etch chamber;

supplying a gas mixture containing at least a carbon fluorine containing gas, an oxygen containing gas and at least argon (Ar) gas into the etch chamber, wherein the Ar gas flow is maintained at between about 5 sccm and about 250 sccm;

forming a plasma from the gas mixture using dual frequency RF power; and

etching the exposed dielectric layer using the plasma formed from the gas mixture.

**24.** The method of claim **23**, wherein the step of forming the plasma from the gas mixture using dual frequency RF power further comprises:

supplying a first RF power at a RF frequency at between about 13.56 MHz; and

supplying a second RF power at a RF frequency at between about 2 MHz.

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