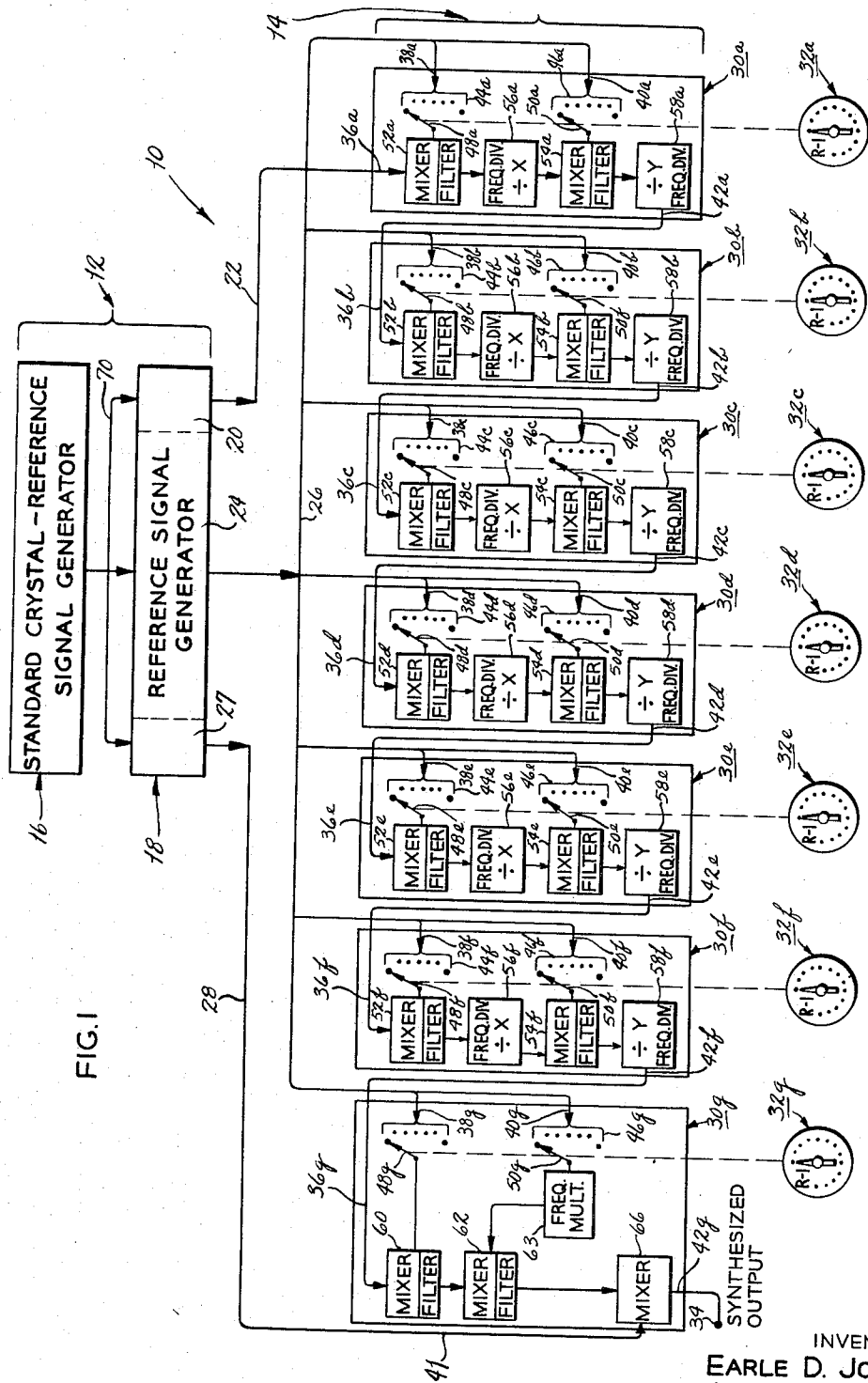


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3 Sheets-Sheet 1



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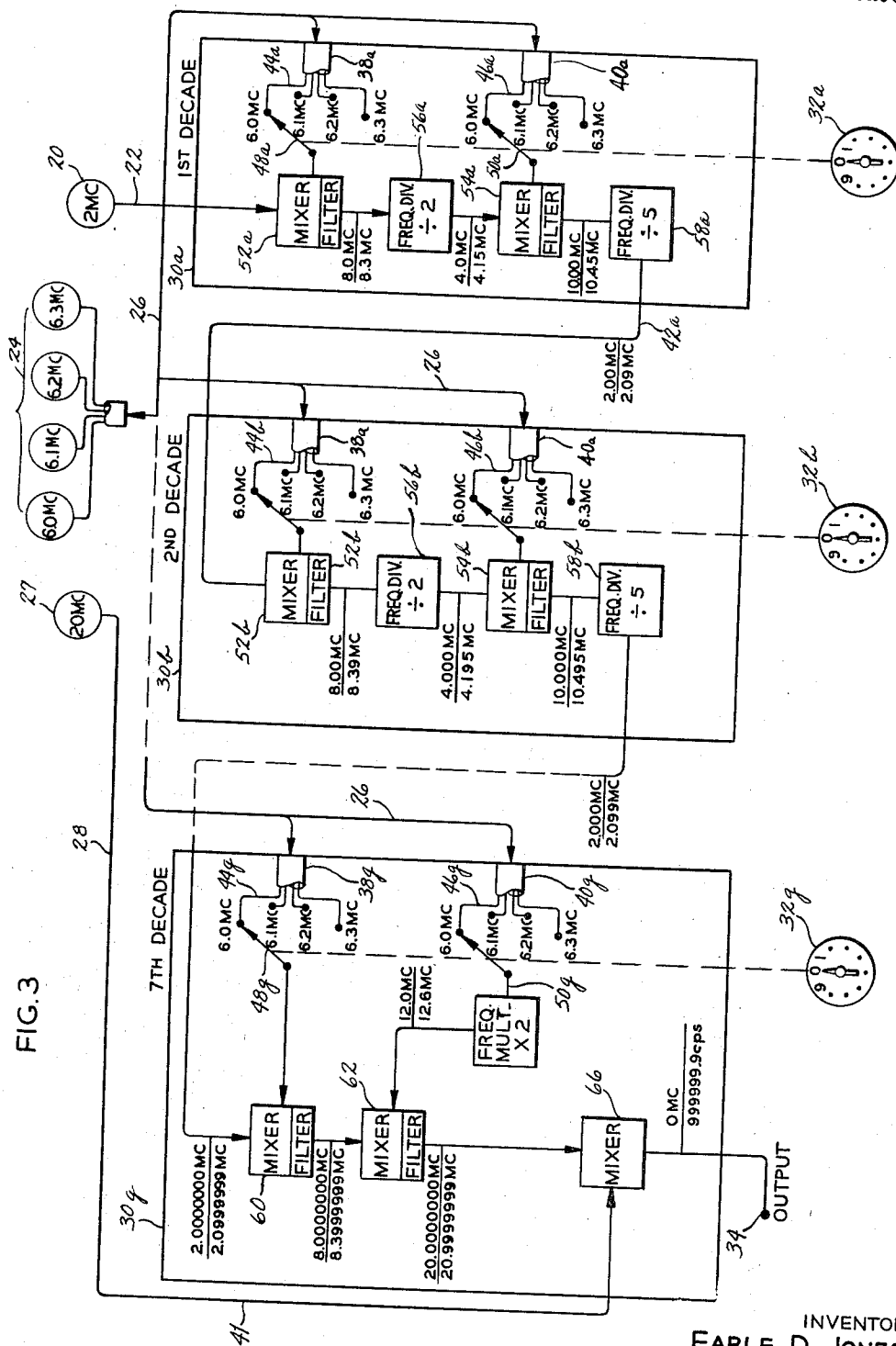
March 5, 1968

E. D. JONES ETAL
FREQUENCY SYNTHESIZER EMPLOYING MINIMAL
NUMBER OF DRIVING FREQUENCIES

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3 Sheets-Sheet 3



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3,372,347

FREQUENCY SYNTHESIZER EMPLOYING MINIMAL NUMBER OF DRIVING FREQUENCIES

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11 Claims. (Cl. 331-39)

ABSTRACT OF THE DISCLOSURE

A frequency synthesizer having modular-type digit selector units consisting of two mixers and two dividers connected in series, the mixers being separated by one divider and the other divider serving as the selector unit output stage. Each mixer has one of its inputs connected through a switch to one of four auxiliary reference signals. In the decade embodiment of the frequency synthesizer one of the dividers provides division-by-two and the other provides division-by-five. In this arrangement only four auxiliary reference signals are required for mixing with a basic reference signal to provide a synthesized signal frequency the lowest digit of which may be one of ten unique digits. The particular synthesized digit results from the particular combination of auxiliary inputs selected by the digit selector unit and applied to the mixer input terminals.

The present invention relates generally to frequency synthesizers, and more specifically to a frequency synthesizer particularly suited to modular construction, wherein each modular unit is available for selecting a digit of a desired frequency to be synthesized. Furthermore, this invention pertains to a frequency synthesizer wherein the number of driving frequencies is minimal, the filtering requirements are greatly eased, and the rejection of spurious components and signals is maximized without substantially compromising rapid switching of the output frequency.

Digital frequency synthesizers are rapidly finding more and more applications in modern electronic environments. Not only are they extremely useful as general-purpose laboratory signal generators for testing highly selective components, both active and passive, but they are also employed as generating units in communication systems where high precision is important; for example, for providing frequency synthesized signals to the oscillators of a receiver or a transmitter. In addition, they find application in process control and digital computer systems where they can be remotely programmed and where their response time is compatible with that of the system.

Heretofore, digital frequency synthesizers of the general type have required that there be available many driving signals from which the desired signal could be synthesized. For example, in decade-type frequency synthesizers (that is, radix or base 10, where each modular unit sets one place or digit of the desired synthesized signal), ten or more auxiliary harmonic signals had to be generated and selected as inputs to the digit selector units in order to synthesize the desired frequency signals, see for example U.S. Patents 2,829,255 and 3,227,963 to V. W. Bolie and R. R. Dimmick, respectively. Furthermore, in conventional frequency synthesizers, a single mixer circuit or a phase-locked, closed-loop circuit is often employed at each decade module to generate the desired digits of the resulting synthesized signal. The single mixer approach presents a serious filtering problem, because the input frequency spectrum presented to the filter associated with such mixer is very close to the desired output frequency. To avoid this problem requires

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the use of complicated and expensive high-Q filters to eliminate the undesired sideband frequencies, and the like. In the case of the phase-locked, closed-loop type decade, the time required to switch the output frequency becomes excessive and therefore renders such a system incompatible with extremely high speed electronic systems.

The general purpose of this invention is to provide a digital frequency synthesizer which has the purity and stability normally associated with crystal-reference signal generators and embraces all the advantages of heretofore employed synthesizers, yet does not possess the afore-described disadvantages. To attain this, the present invention utilizes a multiplicity of substantially identical and unique electronic circuits consisting essentially of electronic signal mixers, relatively low-Q filters, and dividers. These circuits are arranged to form a plurality of cascaded digit selector units such that signals having a wide frequency range may be synthesized from a relatively few number of selectable driving signals.

Among the objects of the present invention is the provision of a novel digital frequency synthesizer amenable to modular-type construction, wherein only a relatively few driving signals are required to provide a wide range of synthesized frequencies.

Another object is to provide a multi-unit digital frequency synthesizer, wherein the filtering requirements necessary to obtain the desired signal frequencies at each of the several units are rendered less stringent by maintaining substantially large sideband separations throughout.

A further object of the invention is the provision of a digital frequency synthesizer which generates a synthesized signal determined by the selected application of a predetermined combination of driving signals to each of a plurality of cascaded digital selector units.

A still further object is to provide a digital frequency synthesizer whose output signal is pure and stable and may be rapidly switched from one frequency to another.

Still another object is to provide a digital frequency synthesizer whose several driving signals may be derived from a single or relatively few number of crystal reference signal generators without employing expensive, multi-section filters.

In the present invention these purposes (as well as others apparent herein) are achieved generally by providing signal generating circuitry which generates a basic reference driving signal of a selected frequency and a plurality of auxiliary reference driving signals of different frequencies. Digit selector units are cascaded together and arranged in an order of increasing digit significance from a least-significant selector unit to a most-significant selector unit, from which the synthesized output is taken. Each of the digit selector units includes appropriate electronic or mechanical switching means to connect it to the auxiliary reference driving signals, the least-significant selector unit being further furnished with the basic reference driving signal. By appropriately selecting and supplying a combination of auxiliary reference driving signals to the digit selector units, a signal having a desired frequency is synthesized and appears at the output of the most-significant selector unit.

The signal synthesis is accomplished by the electronic circuitry of the digital selector units, the circuitry preferably comprising two mixers including associated filters, and appropriate frequency dividers. The combining of the reference driving signals is brought about by the mixers, while the dividers provide a division of the combined signals corresponding to the radix of the particular number system employed. It has been found that the mixers and dividers can be so arranged that relatively

few reference driving signals are required and substantial separation of sideband frequencies is maintained.

Utilization of the invention will become apparent to those skilled in the art from the disclosures made in the following description of a preferred embodiment of the invention as illustrated in the accompanying drawings, in which:

FIG. 1 is a generalized block diagram representation of the frequency synthesizer circuitry of the present invention;

FIG. 2 is a block diagram representation of the reference signal generating circuitry employed in a decade-type embodiment of the present invention;

FIG. 3 is a block diagram representation of the synthesizing circuitry of a decade-type embodiment of the present invention; and

FIG. 4 is a block diagram representation of an alternative circuit arrangement for the selector units of the frequency synthesizer.

Before commencing a detailed description of the new frequency synthesizer, it should be understood that the specific mixers, dividers, multipliers, filters and like circuits referred to in the synthesizer combination are not critical and in themselves may take various forms or designs well known to those skilled in the art. For ease of explaining and understanding the invention, the description of such circuits will not be taken up in detail. References for such circuits are Terman, *Electronic and Radio Engineering*, McGraw-Hill, 1955, R. F. Shea, *Transistor Circuit Engineering*, Wiley 1957, Millman and Taub *Pulse and Digital Circuits*, McGraw-Hill 1956, and T. S. Gray *Applied Electronics*, 2nd edition, Wiley 1954.

Referring now to the drawings, wherein like reference characters designate like or corresponding parts throughout the several views, there is shown in FIG. 1 a digital frequency synthesizer, generally designated 10. The digital frequency synthesizer 10 consists of two basic units, a signal generating unit, generally designated 12, and a signal synthesis unit, generally designated 14. The general function of the signal generating unit 12 is to produce electrical signals of specified frequencies and deliver them to the signal synthesis unit 14. It is the function of the signal synthesis unit 14 to select certain combinations of the signals so supplied and operate on them to produce a synthesized signal having a desired frequency.

The number of frequencies which can be synthesized, the range of such frequencies, and the magnitude of the incremental steps between discrete adjacent frequencies depends largely upon the number of digit selector units employed in the synthesis unit 14 and the selection of reference driving signals supplied by the signal generating unit 12. For example, in a decade embodiment of the invention to be described hereinafter, six digit selector units are provided to produce 1,000,000 possible frequencies ranging from 2.0 mc. to 2.0999999 mc. in steps of 0.1 c.p.s. A seventh, somewhat different unit, is employed to contribute the most-significant digit to the selected frequency and shift the range to 0 c.p.s. to 999,999.9 c.p.s.

The signal generating unit 12 in essence consists of a standard crystal-reference signal generator 16 which provides a fixed frequency signal to drive a multi-section reference signal generator 18. One section 20 of the reference signal generator 18 delivers a basic driving signal to the lead 22, another section 24 delivers a plurality of fixed auxiliary driving signals of different frequencies to a common bus 26, and still another section 27 delivers a third reference frequency to the lead 28. The signal generating unit 12 will be described in further detail hereinafter with reference to FIG. 2.

The signal synthesizer unit 14 of the digital frequency synthesizer 10 consists of a plurality of cascaded digit selector units 30a, 30b, 30c, 30d, 30e, 30f and 30g, each of such digit selector units 30 being preferably of modular-type construction and having direct-reading, multi-position switches 32a, 32b, 32c, 32d, 32e, 32f and 32g associated

therewith. As will be more fully understood from the operational description hereinafter, each of the multi-position switches 32 may be selectively set by an operator so that a signal having a synthesized frequency will be produced at the output terminal 34 of the frequency synthesizer 10. More precisely, the synthesized output signal will have a frequency corresponding to a number N chosen from a selected number system having a radix R, which number N is suitable for digital representation as determined by the settings of the multi-position switches 32. The digit selector units 30 are cascaded together such that the least-significant selector unit is that designated 30a and the most-significant selector unit corresponds to the unit designated 30g, the intermediate digit selector units 30b-f corresponding to the intermediate digits of the number which corresponds to the signal frequency to be synthesized.

If the number system chosen is the decimal system having a radix R of 10, an operator desiring a signal having a frequency of 723,644.1 c.p.s. would set the control dials of switches 32g, 32f, 32e, 32d, 32c, 32b and 32a to read 7, 2, 3, 6, 4, 4, and 1 respectively. It should be apparent that the smaller the radix R of the particular chosen number system, then the more digit selector units will be required, and conversely, if the radix R is large, fewer digit selector units will be required, but more auxiliary reference frequencies may be needed.

Each of the digit selector units has three input terminals 36, 38 and 40 and an output terminal 42. In addition, the digit selector unit 30g has a fourth input terminal 41 connected to the lead 28. The input terminal 36a of the digit selector unit 30a is connected to lead 22 and the input terminals 36b-36g of the selector units 30b-30g are connected to receive the output signal from the respective output terminal 42 of the preceding digit selector unit. The input terminals 38 and 40 of each selector unit are connected to the common bus 26 so that auxiliary reference driving signals from section 24 of the reference signal generator 18 are supplied to two sets of contacts 44 and 46 provided at each digit selector unit 30a-30g. Each contact of each set receives a different auxiliary reference signal as will be more fully described hereinafter.

Movable contacts 48 and 50 are provided to coact with the individual contacts of sets 44 and 46, respectively. These movable contacts 48 and 50 are "ganged" or mechanically linked to each other and to the control dial of the multi-position switches 32. The mechanical linkage between the two movable contacts 48 and 50 of each digit selector unit 30 is so arranged that each setting of the multi-position switches 32a-32g selects a particular combination of two auxiliary reference driving signals from the reference signal generator 18. Such setting in turn determines the digits of a digitally represented number N corresponding to the frequency of a desired output signal. The setting of multi-position switch 32g controls the most-significant digit of the signal produced at the output terminal 34, the setting of multi-position switch 32f controls the next most-significant digit, the setting of multi-position switch 32e controls the third most-significant digit, etc.

It should be understood that where the term "most-significant" digit is used, it is not intended that the value thereof cannot be "0." Any digit selector unit 30 may be set to correspond to the digit "0," in which case the most-significant digit of the number corresponding to the frequency to be synthesized is determined by the "left-most" selector unit which is set to some digit value other than "0."

Although the embodiment of the invention illustrated includes the mechanical multi-position switches 32a-32g, it should be understood that conventional electronic switching circuits could be incorporated to select the proper reference driving signals. In fact, where the synthesizer 10 is to be remotely programed such electronic switching is highly desirable.

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In addition to the multi-position switches 32a-32g, each of the digit selector units 30a-30g have electronic circuit means for combining the signals applied to its inputs. This electronic circuit means is adapted to provide a synthesized signal at each selector unit having a frequency at least one digit of which corresponds numerically to one of R (the radix) predetermined combinations of the auxiliary reference signals selectively applied to their input terminals 38 and 40. In the case of the digit selector units 30a-30f the electronic circuit means are substantially identical consisting of two frequency mixers 52, 54 and two frequency dividers 56, 58.

Each frequency mixer 52 has two inputs, one of which is connected to the input terminal 36 of the digit selector unit and the other connected to the movable contact 48 of the multi-position switch 32. Associated with each frequency mixer 52 there may be provided a filter section which is designed to pass a predetermined frequency range of the resultant signal from the frequency mixer 52. The frequency divider 56 takes its input from the output of the filter section of frequency mixer 52 and performs a frequency division of X, where X is a rational number factor of the radix R. A filter section may also be associated with the frequency divider 56 where it tends to generate undesired harmonics or other spurious signals. The input terminals of the frequency mixer 54 are connected to the frequency divider 56 and the movable contact 50 of the ganged, multi-position switch 32. A filter section may be provided at the output of the frequency mixer 54 so as to deliver only a predetermined range of frequency signals to the input terminal of the frequency divider 58. The frequency divider 58 provides a frequency division corresponding to a value Y, where Y is a rational number factor of the radix R satisfying the expression

$$X \cdot Y = R$$

A filter section may also be provided at the frequency divider 58 to purify the signal applied to the input terminal 36 of the succeeding digit selector unit.

The digit selector unit 30g serves as the output stage of the digital frequency synthesizer 10 and is somewhat different from the cascaded digit selector units 30a-30f. It includes a frequency mixer 60 which takes its two inputs from the input terminal 36g and the movable contact 48g of the multi-position switch 32g. A filter may be provided to select the output of the frequency mixer 60 and apply the selected signal to one input terminal of a second frequency mixer 62. The other input of the frequency mixer 62 is taken from the output of a harmonic generator or frequency multiplier 63, whose input in turn is connected to the movable contact 50g of the multi-position switch 32g. The frequency mixer 62 has its output terminal connected to one terminal of an output frequency mixer 66, whose other input terminal is connected to the input terminal 41 of the digit selector unit 30g. Its output terminal 34 serves as the output terminal for the frequency synthesizer 10.

The co-action between the signal generating unit 12 and the signal synthesis unit 14, as well as the overall operation of the digital frequency synthesizer 10, can be best understood with reference to a decade-type frequency synthesizer, as illustrated in FIGS. 2 and 3. It should be understood, however, that octave or other suitable type frequency synthesizers may be constructed so as to embody the present invention.

In FIG. 2 there is shown a conventional crystal-controlled oscillator 16 which provides a standard output signal having a frequency of 1,000,000 c.p.s. (1 mc.). Since all the reference driving signals are derived from the crystal-controlled oscillator 16, the frequency of its signal must be extremely stable and care should be taken to render it free from detrimental influences such as temperature changes, circuit aging, and the like. The standard 1 mc. signal is applied by lead 70 to a frequency multiplier 20 which generates a second-harmonic signal, of 2 mc.

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This 2 mc. reference driving signal appears at lead 22 and is also supplied by lead 72 to the section 27 of the reference signal generator 18. There its 10th harmonic (20 mc.) is produced by a cascade circuit consisting of two frequency multipliers 74 and 76. The frequency multipliers 74 and 76 frequency multiply the 2 mc. signal by factors of "5" and "2" respectively to provide the 20 mc. reference signal at lead 28.

The dashed line designated 24 in FIG. 2 encloses that portion of the reference signal generator 18 which produces the four auxiliary reference driving signals (6.0, 6.1, 6.2 and 6.3 mc. in the illustrated embodiment) suitable for use in a decade-type digital frequency synthesizer 10. As may be seen from FIG. 2 a 6.0 mc. auxiliary reference signal is obtained by supplying the 2 mc. signal from the output of the frequency multiplier 20 to a frequency multiplier 78, where its third harmonic is produced by a "times 3" multiplier. The 6.0 mc. signal is then delivered to the common bus 26 by means of a lead 80.

In addition the 6.0 mc. signal is supplied as one input to a single-sideband modulator 82 where it is combined with a 200 kc. signal obtained by passing the 1 mc. signal from the crystal-controlled oscillator 16 through a divide-by-5 frequency divider 84. The single sideband modulator 82 is arranged so that only its upper sideband appears in the output, which is supplied as one input to a conventional phase detector 86 to extract a very pure 6.2 mc. upper sideband signal. The other input to the phase detector 86 is derived from a voltage-controlled oscillator 88 whose input in turn is the filtered output signal from the phase detector 86. The output of the voltage-controlled oscillator 88 is also connected to a power amplifier 90, from which the auxiliary reference driving signal of 6.2 mc. is supplied to the common bus 26.

It should be noted that the combination of the phase detector 86 and the voltage controlled oscillator 88 ensures that an extremely pure 6.2 mc. signal is derived from the single sideband modulator 82 without the need for a complicated filter network. That is, the phase detector 86 compares the output signal from the single sideband modulator 82 to that from the voltage controlled oscillator 88 and provides a D.C. error signal or voltage which in turn controls the voltage-controlled oscillator 88. When the output of the oscillator 88 is an exact 6.2 mc. signal, the error voltage applied thereto is of such value as to maintain it at the desired 6.2 mc. In this manner, any spurious signals which might appear in the output of the modulator 82 are nullified and only the desired 6.2 mc. signal appears at the output of the amplifier 90.

The other auxiliary reference driving signals (6.1 and 6.3 mc.) which are used in the preferred decade-type frequency synthesizer 10 are provided at the single sideband modulator 92. The single sideband modulator 92 is substantially identical to single sideband modulator 82, differing only in the respect that both upper and lower sidebands are made available at its output. The single sideband modulator 92 has as one of its inputs, the pure 6.2 mc. signal derived from the output of the voltage controlled oscillator 88. Its other input is a 100 kc. signal derived by applying the 200 kc. signal from the output of frequency divider 84 to a frequency divider 94, which divides such signal by a factor of "2." The upper and lower 6.1 mc. and 6.3 mc. signals from the sideband modulator 92 are purified in the same manner as that employed to purify the 6.2 mc. signal derived from the single-sideband modulator 82. Since the phase-locked loops (identified by the prime, and double-prime notations in FIG. 2) employed to purify the 6.1 and 6.3 mc. signals are substantially identical to those used to purify the 6.2 mc. signal, their operation is not described in detail. The purified 6.1 and 6.3 mc. auxiliary reference driving signals are taken from the output of the amplifiers 90' and 90'' respectively and delivered to the signal synthesis unit 14 by means of the common bus 26.

In FIG. 3 there are shown the first, second and seventh

cascaded decades of the signal synthesis unit 14 of a decade-type digital frequency synthesizer 10. The 6.0 mc., 6.1 mc., 6.2 mc., and 6.3 mc. auxiliary reference driving signals are supplied to the sets of contacts 44 and 46 of each of the digit selector units 30 by means of the common bus 26. The 2 mc. reference driving signal is supplied as one input to the signal mixer 52a of the first decade selector unit 30a. The other input to the mixer 52a is taken from the movable contact 48a of the multi-position switch 32a. It may be seen that the filtered output supplied to the frequency divider 56a from the mixer 52a may be any one of the four upper sideband signals 8.0, 8.1, 8.2 or 8.3 mc. depending upon the position of the movable contact 48a. The frequency divider 56a in the decade-type synthesizer 10 is chosen such that a division of "2" is performed upon its input signal. Thus, the signal supplied to the second mixer 54a of the selector unit 30a may be any one of the four signals 4.0, 4.05, 4.1 or 4.15 mc. Any one of these signals may be mixed with any one of the four auxiliary reference driving signals at the set of contacts 46. That is, depending upon the position of movable contact 50a, it is possible to obtain any one of the ten upper sideband signals 10.00, 10.05, 10.10, 10.15, 10.20, 10.25, 10.30, 10.35, 10.40, or 10.45 mc.

The frequency divider 58a is adapted to provide a division by "5" so that the signal appearing at the output terminal 42a of the first decade selector unit 30a may be any one of the ten signals in the range of from 2.00 to 2.09 mc. in steps of 0.01 mc.

It should be noted that for the decade-type synthesizer 10, the auxiliary reference signals 6.0 . . . 6.3 mc. are of the order of three times greater than the basic reference signal 2.0 mc. Stated generally, where the basic reference signal is some value M c.p.s. then the auxiliary reference signals are within the range of from 3M to (3M+r) c.p.s. where r is the nominal range of the basic decade unit. For the embodiment illustrated, the basic reference signal is 2 mc. and the range of each basic selector unit is .1 mc.; thus the auxiliary reference signals are within the range of from 6 mc. to 6.3 mc. Only four auxiliary reference signals are required to provide all of the ten synthesizable signals 2.00, 2.01, 2.02 . . . 2.09 mc. at the first decade selector unit 30a. This is brought about by the unique decade arrangement employing the two mixers 52a, 54a, each having an input that is switchable to receive one of the auxiliary reference signals 6.0, 6.1, 6.2 or 6.3 mc. and combine it with its other input. The movable contacts 48a and 50a are linked together so that, for example, if the indicator dial is set to the numeral "8," then contact 48a is set to engage the 6.2 mc. contact of set 44a and contact 50a is set to engage the 6.3 mc. contact of set 46a. Such setting results in a 2.08 mc. signal at output terminal 42a and the desired digit "8" has been synthesized.

It can be demonstrated mathematically that for the general two mixer case, i.e. where a number system having a radix of some arbitrary value R is chosen, the dividers 56a and 58a can be chosen to provide divisions corresponding to rational number factors of the radix R, and the number of auxiliary reference signals P required can be determined by the expression:

$$2^P \geq R \quad (P \text{ being an exponent})$$

For example, where R is 10, as it will be in a decade type synthesizer, the minimum number of auxiliary reference signals (P) will be four (4).

A constraint placed upon the auxiliary reference signals is that their numerical values, when digitally represented, must contain a set of digits in a designated place such that the set of numbers obtained by multiplying each digit by the value X (the value of the first frequency divider 56) and adding digits of the resultant product set with digits of the original set will include a set of digits corresponding to the integers from 0 to R-1, where R is the radix of the chosen number system. For

example in the illustrated embodiment the original set of digits are the 0, 1, 2 and 3 of the 6.0, 6.1, 6.2 and 6.3 mc. signals. When these digits are multiplied by 2 (the value of the first divider 56), a product set of digits 0, 2, 4, and 6 is obtained. Sixteen sums may be obtained by adding each digit of the original digit set (0, 1, 2 and 3) to all of the digits of the product set (0, 2, 4, and 6). Ten of these summations will be the integers from 0 to 9, and the remaining six will merely be duplicates of certain of the other integers.

The second decade selector unit 30b has electrical components corresponding to those of the first decade selector unit 30a, but instead of the first mixer 52b receiving its one input from the 2 mc. reference source, it takes its input from the output terminal 42a of the first decade unit 30a. In operation the unit 30b performs substantially identical to the unit 30a and adds an additional digit to the right of the decimal place of the signal which is supplied to its input terminal 36b from the decade selector unit 30a. The value of the digit so added, like the value of the digit synthesized by unit 30a, may be any of the ten integers from 0 to 9 and is determined by the setting of switch 32b. Thus, the output signal at terminal 42b may be any one of the one hundred signals 2.000, 2.001, 2.002 . . . 2.099 mc.

It should be apparent from the foregoing description of the 1st, and 2nd decade selector units that each unit thereafter adds an additional place to the right of the decimal point of the number corresponding to the synthesized signal, and the value of digit occupying such place is determined by the setting of the multi-position switches 32 at each unit. The output signal from the sixth decade 30f would therefore be one of the 10^6 signals ranging from 2.0000000 to 2.0999999 mc.

If desired, the output signal from the sixth decade 30f may be mixed with a 2 mc. signal and filtered to provide the synthesizer output. However, we have discovered that the range can be extended by an order of magnitude if a seventh decade unit 30g is provided. Unlike the other units, decade unit 30g requires no frequency dividers. It takes as its input one of the 10^6 input signals from the sixth decade 30f and mixes it at a frequency mixer 60 with one of the four auxiliary reference signals 6.0, 6.1, 6.2, or 6.3 mc. supplied to its other input by the movable contact 48g of the switch 32g. The upper sideband output signal of the mixer 60 is one of the 4 million signals whose frequencies range from 8.0000000 to 8.3999999 mc., which signal is mixed at a second frequency mixer 62 with one of the second-harmonic signals of the four auxiliary reference signals 6.0 . . . 6.3 mc. These second-harmonic signals are obtained by selectively applying one of the auxiliary reference signals to a frequency multiplier 63, whose output is connected to one input of the mixer 62. As indicated in FIG. 3, the output of the mixer 62 is one of the 10^7 frequency signals ranging from 20.0000000 to 20.9999999.

The 20 mc. reference signal from section 27 of the reference signal generator 18 is delivered to the output mixer 66 where it serves to heterodyne down the purified signal supplied from the frequency mixer 62. The lower sideband output signal from mixer 66 constitutes the output of the synthesizer. It will have a selected frequency within the range of from 0 to 999,999.9 c.p.s. and appears at the output terminal 34.

An alternative digit selector unit 106, which may be employed instead of the decade selector units 30a-30f, is shown in FIG. 4. Here again, two mixers are employed but instead of separating them by a divider, they are directly coupled together. The division is accomplished after the two stages of mixing has taken place and the second mixer has a modified reference signal source. The input mixer 52 of the selector unit 106 takes its inputs from the same sources as the input mixers 52 of the digit selector units 30. However, the upper sideband output signal from the mixer 52 is applied directly as one input

to the second mixer 54. The other input of the mixer 54 is furnished by a frequency multiplier 108 which produces a second-harmonic signal of one of the auxiliary reference signals as determined by the setting of the movable contact 50.

The output signal from the mixer 54 is then divided by a frequency divider circuit 110, which in the case of a decade frequency synthesizer will provide a division of 10.

Many modifications and variations will be apparent to those skilled in the art from the above teachings. For example, various filter sections may be eliminated where the mixers, dividers, multipliers and the like are designed such that substantially all the undesired signals are eliminated. In addition it should be apparent that the frequency multipliers 63 and 108 employed to provide a second harmonic of the auxiliary reference driving signals 6.0, 6.1, 6.2, and 6.3 mc. to the frequency mixers 62 and 54, respectively, could instead be employed to provide such second harmonic signals to the frequency mixers 60 and 52. Therefore, it is to be understood that the invention may be practiced otherwise than as specifically described.

We claim:

1. A frequency synthesizer of the type providing the selectable setting of digits of a number N corresponding to a signal frequency to be synthesized and selected from a number system having a radix of value R, comprising:
 - means for generating a basic reference driving signal having a fixed predetermined frequency,
 - means for generating a plurality of auxiliary reference driving signals of substantially lesser number than the radix R of the selected number system, each signal having a different fixed predetermined frequency, together with
 - a plurality of cascaded digit selector means having first, second and third input terminals and an output terminal, said first and second input terminals being electrically connected to selectively receive said signals from said auxiliary reference signal generating means, each digit selector means being cascaded in an order of increasing significance of digits from a least-significant selector means to a most-significant selector means, said third input terminal of said least-significant selector unit being coupled to receive said basic reference driving signal,
 - each of said digit selector means including circuit means for combining said auxiliary reference signals with the signal applied to its third input terminal and generating at said output terminal a synthesized signal having a frequency at least one digit of which corresponds numerically to one of R predetermined combinations of said auxiliary reference signals selectively applied thereto.
2. The frequency synthesizer as defined in claim 1, wherein:
 - said circuit means of said most-significant selector means, comprises:
 - first mixing means for selectively mixing said auxiliary reference driving signals with the output signal from the preceding digit selector means, multiplier means electrically connected to selectively receive said auxiliary reference driving signals and generate an output signal whose frequency is a multiple of that of said signal received thereby, and
 - second mixing means for mixing said output signal of said multiplier means with the output signal from said first mixing means.
3. The frequency synthesizer as defined in claim 1, wherein:
 - each of said digit selector means having a nominal frequency range corresponding substantially to the difference between the highest frequency and the lowest frequency which may be generated thereby,

said basic reference driving signal generating means generates a fixed frequency of M cycles per second, and

said auxiliary reference driving signal generating means generates signals whose frequencies are within the range of from approximately 3M cycles per second to approximately $3M+r$ cycles per second where r is said nominal frequency range of said digit selector means.

4. The frequency synthesizer as defined in claim 1, wherein:

the number of said plurality of auxiliary reference driving signals is equal to or greater than P and less than R, where P is determined from the expression

$$2^P \geq \text{said radix value R}$$

5. The frequency synthesizer as defined in claim 4, wherein:

said circuit means of all of said digit selector means except said most-significant digit selector means, comprises:

- means for mixing said auxiliary reference driving signals with said signal applied to said third input terminal of said digit selector means and providing therefrom an output signal having different frequency,

- means electrically connected to receive and filter said output signal from said mixing means, and
- means connected in series with said mixing means and said filtering means for frequency dividing said output signals therefrom, said frequency dividing means providing a frequency division of said mixed signals corresponding to the value of the radix R,

whereby the most significant digit of the synthesized output frequency of each selector means is substantially identical with that of said basic reference driving signal.

6. The frequency synthesizer as defined in claim 5, wherein:

- said mixing means includes at least first and second electrical digital frequency mixers, said first frequency mixer of said least-significant digit selector means being connected to receive as one of its inputs said basic reference driving signal and as its other input said selectable auxiliary reference driving signals, said first frequency mixer of the remaining selector means being connected to receive as one of its inputs the output signal of the preceding selector means and as its other input said selectable auxiliary reference driving signals,

- said frequency dividing means including at least first and second electrical digital frequency dividers, said first divider being characterized by providing a division by X and said second divider characterized by providing a division by Y, where X and Y are rational numbers related by the expression

$$X \cdot Y = R, \text{ the value of the radix}$$

- one of said digital frequency dividers being connected to receive its input from said first mixer and supply its output to said second mixer,
- said second mixer being electrically connected to receive its other input from said selectable auxiliary reference driving signals and supply its output to the other said digital frequency divider.

7. The frequency synthesizer as defined in claim 6, wherein:

- the numerical values of the frequencies of said auxiliary driving signals are chosen such that the set of frequencies obtained by adding each digit of a selected place of such frequencies to a designated place of a set of frequencies derived by multiplying said digits by the value corresponding to the division performed by said digital frequency divider connected

between said first and second digital frequency mixers includes a set of frequencies having a designated place which includes the integers from 0 to $R-1$, where R is the value of the radix.

8. The frequency synthesizer as defined in claim 6, wherein the numerical values of X and Y are 2 and 5 respectively and that of R is 10.

9. The frequency divider as defined in claim 7, wherein: said mixing means includes at least first and second electrical digital frequency mixers,

said first mixer of said least-significant selector means being connected to receive said basic reference driving signal as one of its inputs and said selectable auxiliary signals as its other input, said first mixer of said remaining selector means being electrically connected to receive as one of its inputs said output signal from the preceding selector means and as its other input one of said selectable auxiliary reference driving signals,

said second digital frequency mixer being electrically coupled to receive one of its inputs from the output of said first digital frequency mixer,

said frequency divider means being a digital frequency divider electrically coupled to the output of said second digital frequency mixer means and characterized by providing a division corresponding to the value of the radix R , and

frequency multiplying means electrically connected to receive as its inputs said selectable auxiliary driving signals and having its output coupled to the other input of said second digital frequency mixer.

10. The frequency synthesizer as defined in claim 9, wherein:

the numerical values of the radix R is 10 and said frequency multiplying means provides at its output a signal having a frequency of twice that of its input frequency.

11. For use as one of a plurality of substantially identical digit selector units in a digital frequency synthesizer

for synthesizing an output signal from an input signal and auxiliary reference driving signals, the circuitry comprising:

first and second electrical digital frequency mixers, each mixer having two input terminals and an output terminal for providing a signal whose frequency is the sum of frequencies applied to said input terminals thereof, one of said input terminals of said first mixer being connectable to such input signal,

switching means electrically connectable to such auxiliary reference driving signals and said first and second mixers for selectively applying one of such auxiliary reference signals to said other input terminal of each of said mixers, and

first and second electrical digital frequency dividers, said first divider being electrically connected to receive the output signal from said first mixer and deliver a signal whose frequency has been reduced by a first predetermined magnitude to said second mixer, said second divider being electrically connected to receive the output signal from said second mixer and produce such digit selector unit output signal whose frequency is reduced by a second predetermined magnitude from that of the said second mixer output signal;

said output signal of said second divider having a frequency one, and only one, digit of which is determined by the application of selected auxiliary reference signals to said first and second mixers by said switching means.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,372,347

March 5, 1968

Earle D. Jones et al.

It is certified that error appears in the above identified patent and that said Letters Patent are hereby corrected as shown below:

Column 11, line 8, the claim reference numeral "7"
should read -- 6 --.

Signed and sealed this 19th day of August 1969.

(SEAL)

Attest:

Edward M. Fletcher, Jr.

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Commissioner of Patents