US 20090165706A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2009/0165706 A1**

(43) **Pub. Date: Jul. 2, 2009**

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(54) **METHOD FOR FORMING A PLURALITY OF METAL LINES IN A SEMICONDUCTOR DEVICE USING DUAL INSULATING LAYER**

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(21) Appl. No.: **12/397,169**

(22) Filed: **Mar. 3, 2009**

Related U.S. Application Data

(62) Division of application No. 11/320,408, filed on Dec. 29, 2005, now Pat. No. 7,517,799.

(30) **Foreign Application Priority Data**

Dec. 29, 2004 (KR) 10-2004-0115538

Publication Classification

(51) **Int. Cl.**
B05C 11/00 (2006.01)
C23C 14/34 (2006.01)

(52) **U.S. Cl.** **118/75**; 204/298.02

(57) **ABSTRACT**

A method for forming a plurality of metal lines in a semiconductor device including forming first insulating layer patterns on a semiconductor substrate, the first insulating patterns being spaced from each other; depositing a metal layer on and between the first insulating layer patterns; planarizing the metal layer; patterning the planarized metal layer to form the plurality of metal lines between the first insulating layer patterns; and forming a second insulating layer on and between the metal lines.

FIG. 1A

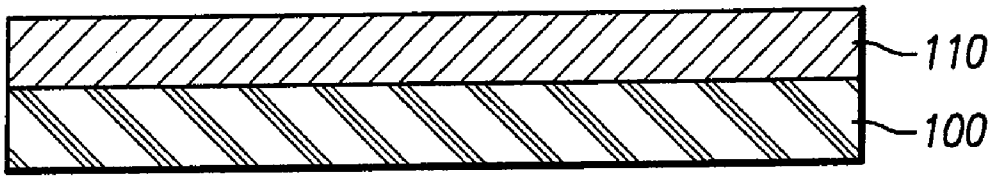


FIG. 1B

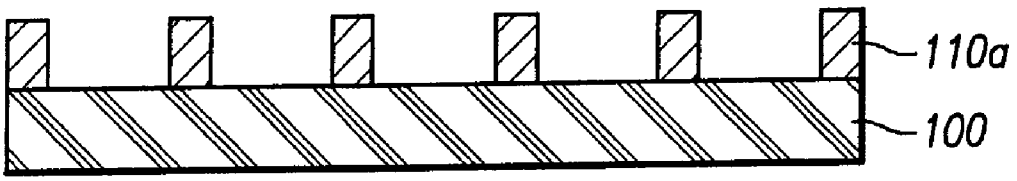


FIG. 1C

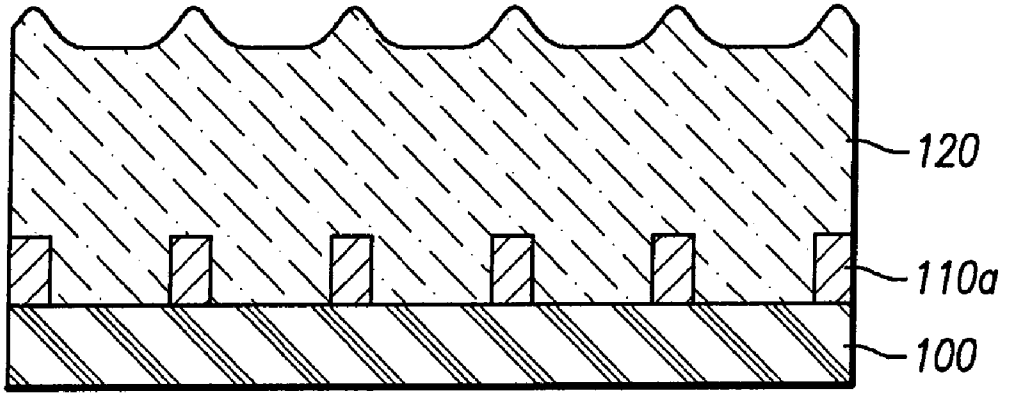


FIG. 1D

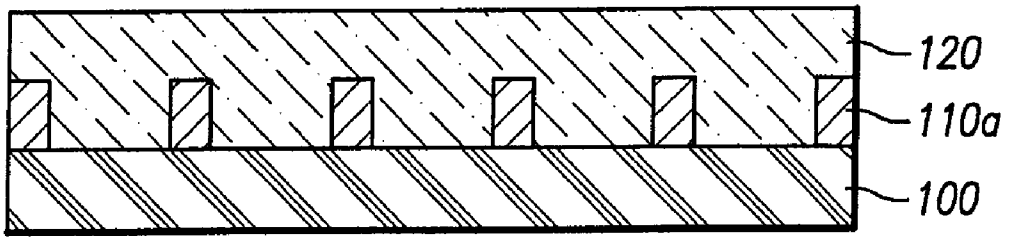


FIG. 1E

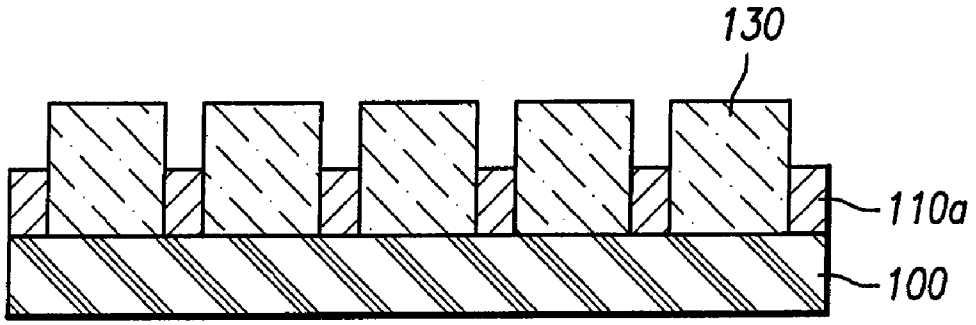


FIG. 1F

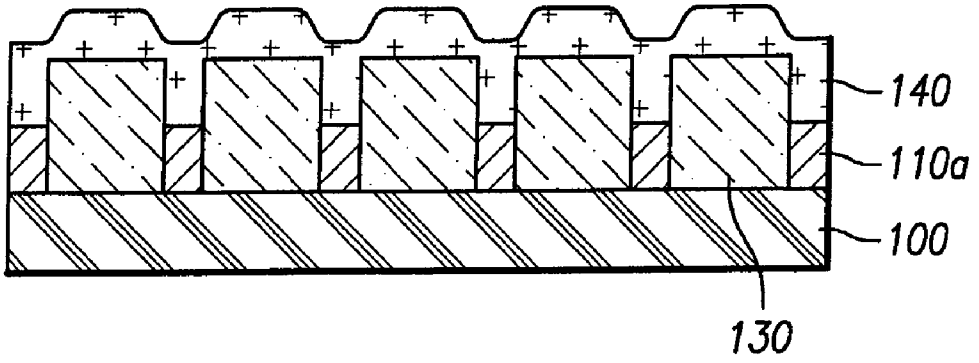


FIG. 1G

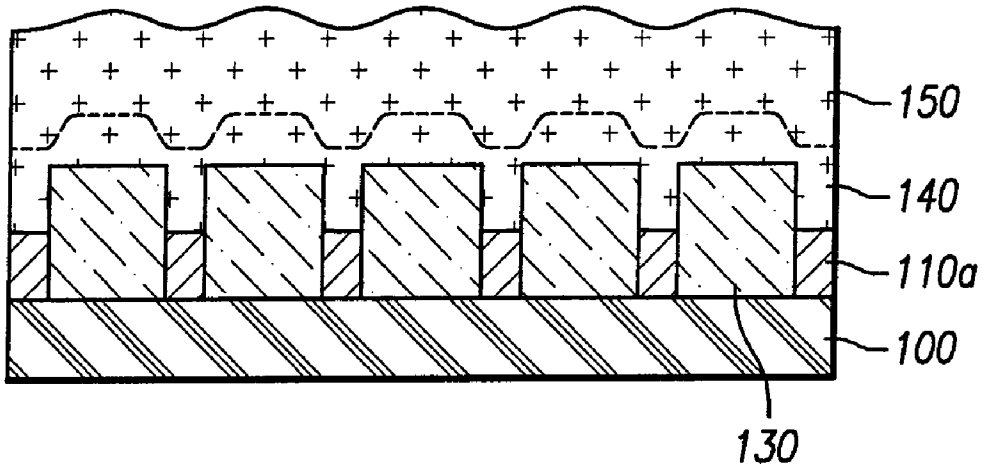
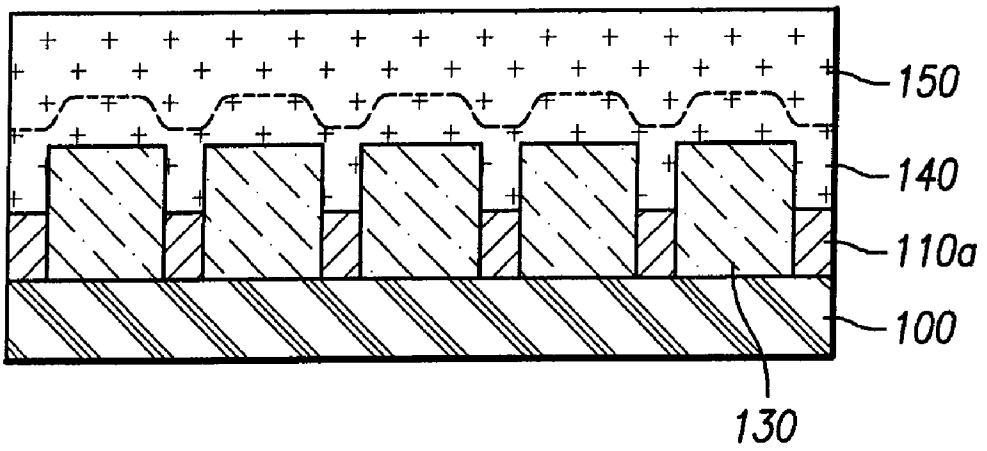


FIG. 1H



METHOD FOR FORMING A PLURALITY OF METAL LINES IN A SEMICONDUCTOR DEVICE USING DUAL INSULATING LAYER

[0001] This application claims the benefit of Korean Application No. 10-2004-0115538, filed on Dec. 29, 2004, which is incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention generally relates to a metallization method of a semiconductor device, and particularly to a method for forming a plurality of metal lines on a semiconductor substrate using a dual insulating layer.

[0004] 2. Description of the Related Art

[0005] As the integration and miniaturization of semiconductor devices are increased, the dimension of a metal line for interconnecting circuits is decreased more and more. For a higher operational speed of devices, metal interconnecting lines need to be designed to have a low electric resistivity. In general, the electric resistivity is proportional to the width and height of the metal line, and inversely proportional to length thereof. The height of the metal line, as well as the width thereof, should be reduced to a minimum. However, the height and width have a critical value in view of limitations of the metal line formation process. Therefore, an aspect ratio (i.e., a ratio of height-to-diameter) of the gaps between the metal lines, which may be filled with an insulating material, is increased according to the miniaturization of the devices.

[0006] Conventionally, low resistivity metals such as aluminum, copper and their alloys have been widely used as fine metal lines in semiconductor manufacturing. As a typical example, aluminum alloyed with copper of about 1~4 wt % is used for the fine metal line, which is resistant to electromigration. The aluminum metal line is generally formed by a physical vapor deposition (PVD) process, also known as a sputtering process, which involves the steps of: depositing a metal thin film on a substrate; etching the metal thin film to form metal lines; and filling gaps between the metal lines with an insulating material.

[0007] However, today's emphasis on scaling down line width dimension of the metal lines has led to gap-fill problems due to a high aspect ratio of the gaps. A variety of alternative approaches have been explored for forming fine metal lines in a semiconductor substrate.

[0008] One approach is to utilize a damascene method, but it may incur increase of electric resistivity of the metal line owing to the diffusion of chemical impurities. Another approach is to employ an aluminum gap-fill process using chemical vapor deposition (CVD), but this may lead to reliability problems including electromigration.

[0009] In order to solve these problems, Korean Patent Publication No. 10-2003-005600 discloses a multilayered metallization structure with a barrier metal layer. The barrier metal layer is formed on an upper surface and sidewall of an insulating layer and a contact plug is formed to interconnect with an underlying metal line in a bottom portion of the insulating layer. This metallization structure can reduce the electric resistivity of metal lines, because the insulating layer is disposed between metal lines. Yet, it is difficult for metal to fill a high aspect ratio of the gaps present in the insulating layer.

SUMMARY OF THE INVENTION

[0010] It is, therefore, an object of the present invention to provide a method for forming a plurality of metal lines in a semiconductor device using a dual insulating layer. The metal deposition can be easily performed without gap-fill problems, even by a PVD sputtering process generally known as having inferior step coverage.

[0011] To achieve the above objects, an embodiment of a method for forming a plurality of metal lines in a semiconductor device, according to the present invention includes: (a) forming first insulating layer patterns on a semiconductor substrate, the first insulating patterns being spaced to each other; (b) depositing a metal layer on and between the first insulating layer patterns; (c) planarizing the metal layer; (d) patterning the planarized metal layer to form the plurality of metal lines between the first insulating layer patterns; and (e) forming a second insulating layer on and between the metal lines.

[0012] It is to be understood that both the foregoing general description of the invention and the following detailed description are exemplary, but are not restrictive of the invention.

BRIEF DESCRIPTION OF DRAWINGS

[0013] These and other aspects of the present invention will become evident by reference to the following description of the invention, often referring to the accompanying drawings.

[0014] FIGS. **1**A to **1**H are cross-sectional views of a semiconductor substrate, illustrating an embodiment of a method for forming metal lines in a semiconductor device, according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] The present invention utilizes a couple of insulating layers to reduce an aspect ratio of gaps into which metal lines may be deposited. It should be understood that the techniques and resulting structures are not limited to using any specific substrates and dielectric or insulating overlays. Moreover, the present invention is not restricted to any particular metal or metal alloys. Hereinafter, an exemplary embodiment of the present invention will be described in detail, with reference to FIGS. **1**A to **1**H.

[0016] Referring to FIG. **1**A, a first insulating layer **110** is formed on a semiconductor substrate **100**. Preferably, a thickness or height of the first insulating layer **110** is from about ⅓ to about ⅔ of that of a resulting metal line (see a metal line **130** in FIG. **1**E) that may be formed in the subsequent steps.

[0017] Next, the first insulating layer **110** is patterned to form insulating layer patterns **110***a* by a photolithography and etch processes, as shown in FIG. **1**B.

[0018] Subsequent to the formation of the insulating layer patterns **110***a*, metal material **120** such as aluminum is deposited over the entire substrate, filling gaps between the insulating layer patterns **110***a*, as shown in FIG. **1**C. The deposition of the metal material **120**, preferably aluminum, is performed by a PVD sputtering process. In this case, the metal material **120** is deposited thicker than the resulting metal line **130**, sufficiently covering the insulating layer patterns **110***a*. Since the insulating layer patterns **110***a* are

formed to be much lower than the resulting metal line **130**, the gaps between the insulating layer patterns **110***a* may have a relatively low aspect ratio. As a result, a PVD-Al layer **120** can fill the gaps without gap-fill issues such as voids.

[0019] As shown in FIG. **1**D, the metal layer **120** is continuously planarized via chemical-mechanical polishing (CMP) or an etch-back process until it has a desired thickness or height.

[0020] Referring to FIG. **1**E, the planarized metal layer **120** is patterned to form metal lines **130** by a photolithography and etching processes using a photo mask. The photo mask defines openings over regions in which the insulating layer patterns **110***a* are formed. Namely, portions of the metal layer **120** over the insulating layer patterns **110***a* may be removed. In this case, the etching process is controlled to expose upper surfaces of each of insulating layer patterns **110***a*.

[0021] Next, as shown in FIG. **1**F, a second insulating layer **140** is formed over the entire substrate **100**, thus covering the metal lines **130** and filling gaps between the metal lines **130**. The gaps between the metal lines **130**, in which the first insulating layer patterns **110***a* remains, may have a relatively low aspect ratio. Preferably, the gap filling with the second insulating material is performed by high-density plasma CVD.

[0022] A capping layer **150** may be selectively formed on the second insulating layer **140**, as shown in FIG. **1**G, and the substrate is then planarized by a CMP process, as shown in FIG. **1**H.

[0023] While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

1-7. (canceled)

8. An apparatus for forming a plurality of metal lines in a semiconductor device, comprising:

means for forming first insulating layer patterns on a semiconductor substrate, the first insulating patterns being spaced from each other;

means for depositing a metal layer on and between the first insulating layer patterns;

means for planarizing the metal layer;

means for patterning the planarized metal layer to form the plurality of metal lines between the first insulating layer patterns;

means for forming a second insulating layer on and between the metal lines.

9. The apparatus of claim **8**, wherein the means for forming first insulating layer patterns includes means for forming first insulating layer patterns lower than the metal lines.

10. The apparatus of claim **9**, wherein the means for forming first insulating layer patterns includes means for forming first insulating layer patterns with a height of ⅓ to ⅔ of that of the metal lines.

11. The apparatus of claim **9**, further comprising means for planarizing the second insulating layer.

12. The apparatus of claim **9**, wherein means for depositing a metal layer includes means for depositing a metal layer comprising aluminum.

13. The apparatus of claim **9**, wherein means for depositing a metal layer includes a sputtering apparatus.

14. The apparatus of claim **9**, wherein means for forming a second insulating layer includes a high-density plasma CVD apparatus.

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