US 20030205480A1

(19) **United States**
(12) **Patent Application Publication**
Sakaguchi et al.
(10) **Pub. No.: US 2003/0205480 A1**
(43) **Pub. Date: Nov. 6, 2003**

(54) **ANODIZING METHOD AND APPARATUS AND SEMICONDUCTOR SUBSTRATE MANUFACTURING METHOD**

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(21) Appl. No.: **10/459,044**

(22) Filed: **Jun. 11, 2003**

Related U.S. Application Data

(62) Division of application No. 09/251,668, filed on Feb. 17, 1999, now abandoned.

(30) **Foreign Application Priority Data**

Feb. 26, 1998 (JP) 10-045309

Publication Classification

(51) **Int. Cl.**[7] **C25D 5/00**
(52) **U.S. Cl.** **205/159**; 205/333; 205/171

(57) **ABSTRACT**

A porous layer having a multilayered structure is formed. An Si substrate (**102**) to be processed is anodized in a first electrolytic solution (**141, 151**) while being held between an anode (**106**) and a cathode (**104**) in an anodizing bath (**101**). The first electrolytic solution (**141, 151**) is exchanged with a second electrolytic solution (**142, 152**). The Si substrate (**102**) is anodized again, thereby forming a porous layer having a multilayered structure on the Si substrate (**102**).

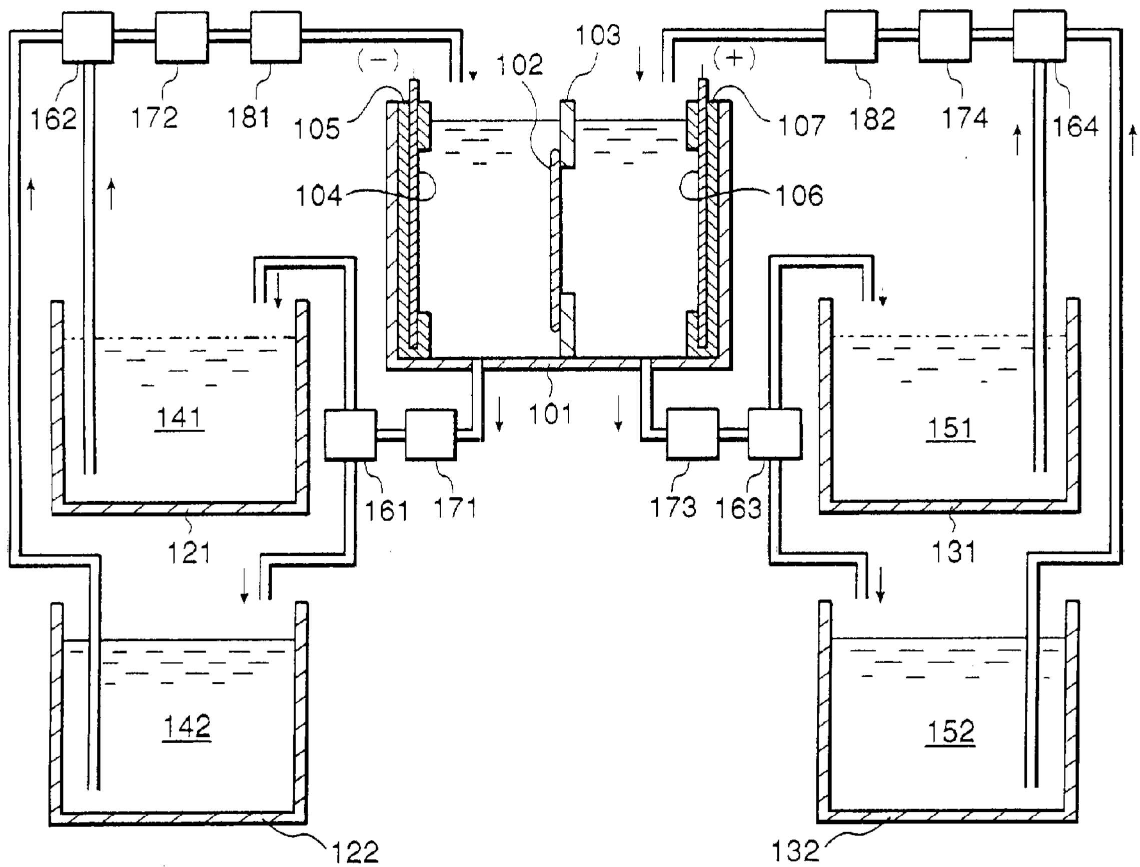


FIG. 1A

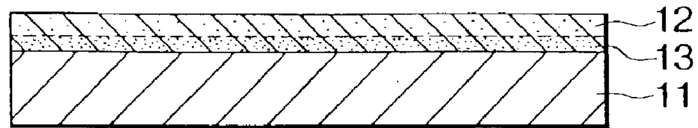


FIG. 1B

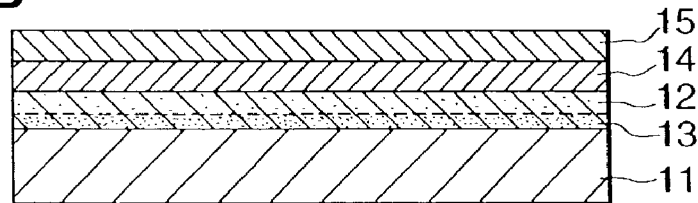


FIG. 1C

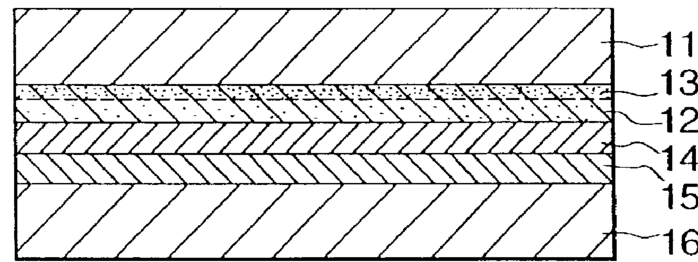


FIG. 1D

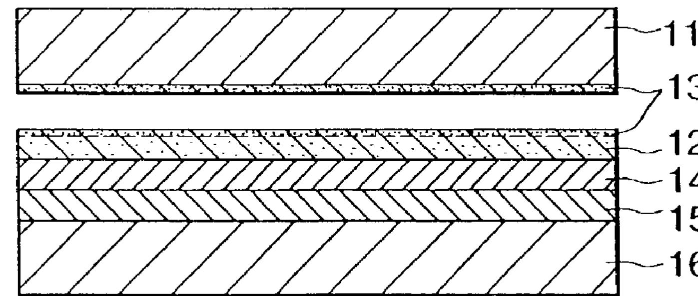


FIG. 1E

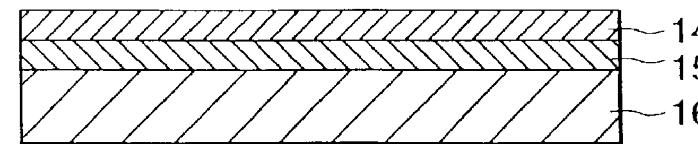


FIG. 1F

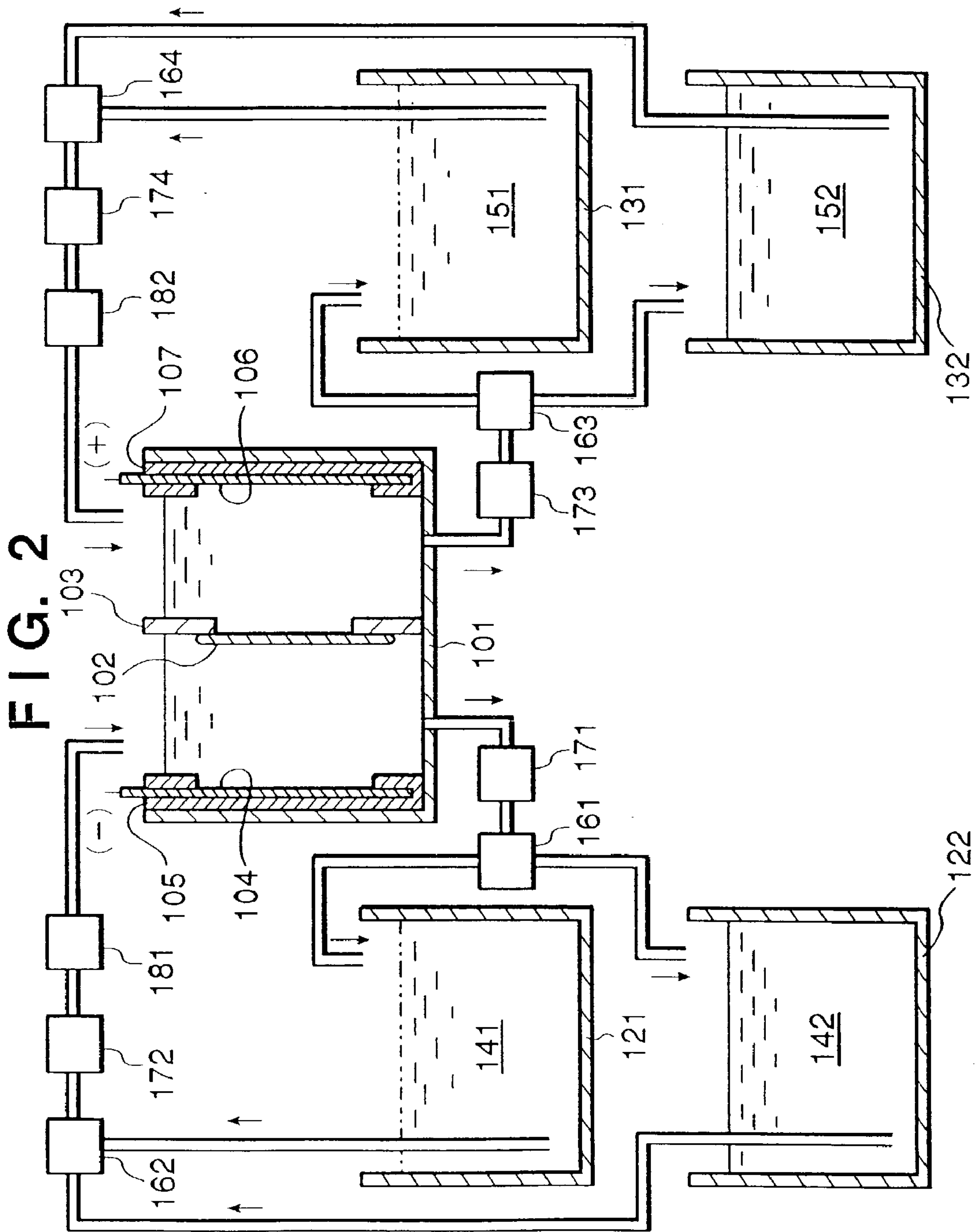


FIG. 2
164
174
182
107
106
(+)
151
131
152
132
163
173
103
102
101
171
161
(−)
105
104
122
181
172
162
141
121
142

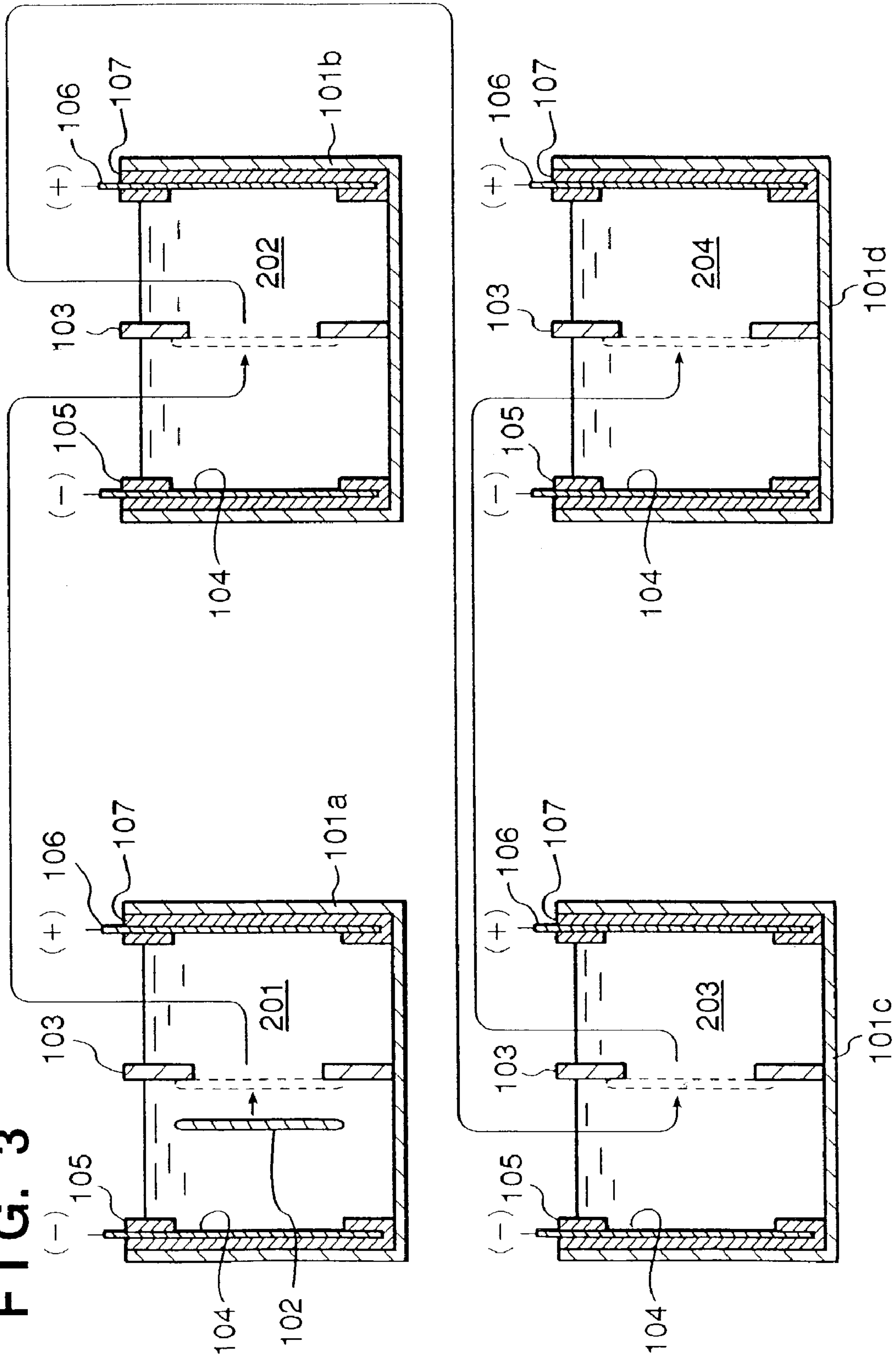
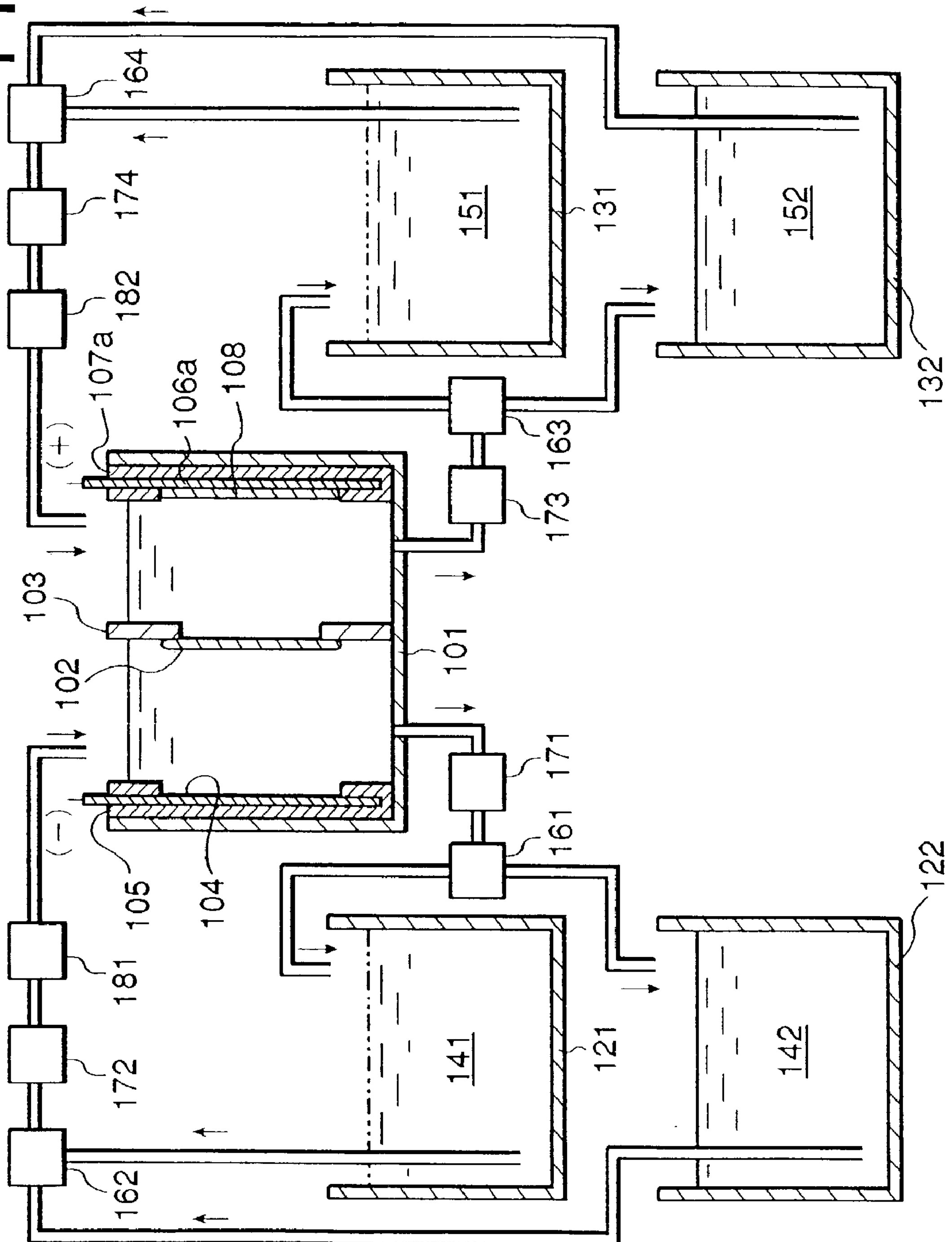


FIG. 3
(+)
(−)
106
107
101a
101b
101c
101d
103
105
104
102
201
202
203
204


F I G. 4
164
174
182
107a
106a
108
(+)
103
102
101
173
163
131
151
152
132
171
161
(−)
105
104
181
172
162
141
121
142
122

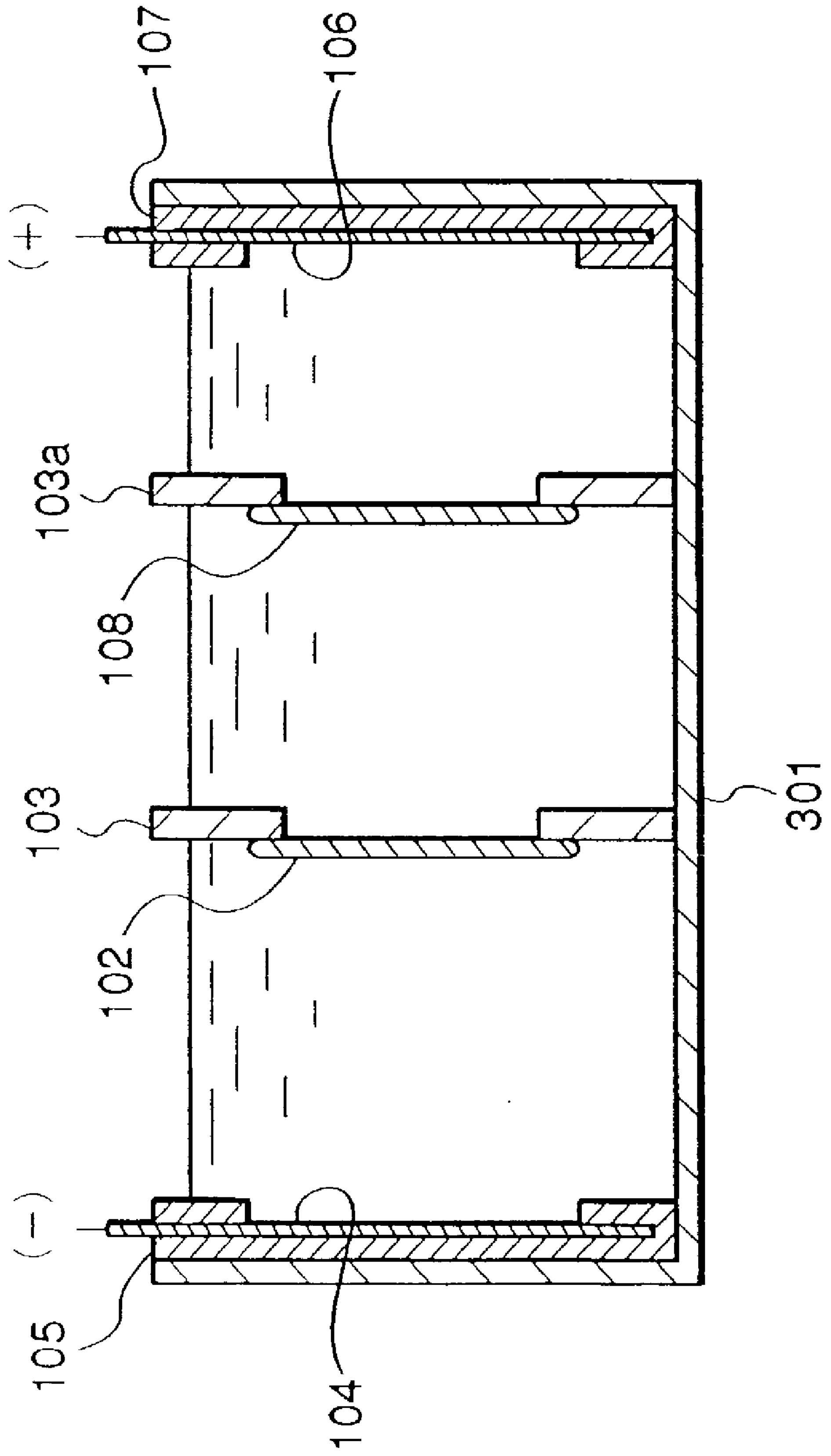


FIG. 5
107
106
(+)
103a
108
103
102
301
(−)
105
104

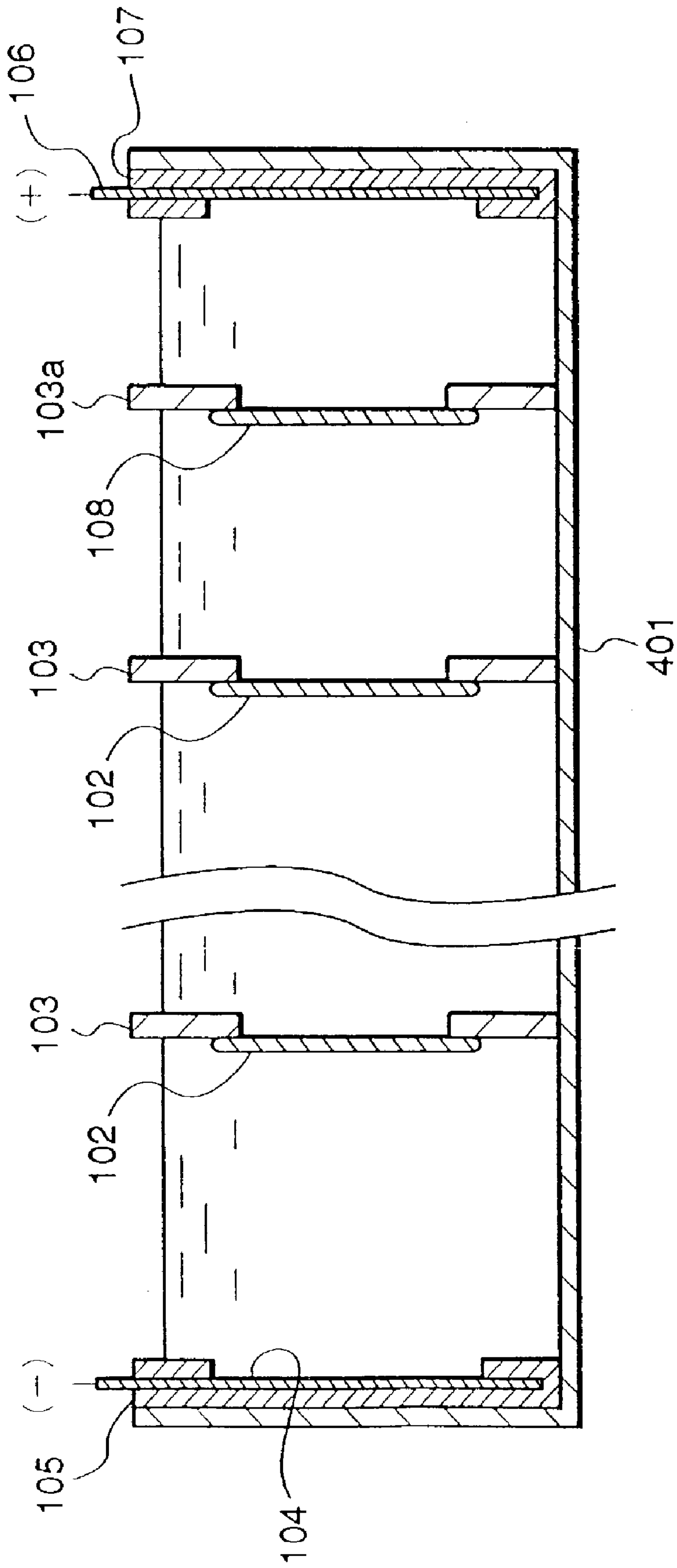


FIG. 6
106
107
(+)
103a
108
103
102
401
103
102
(−)
105
104

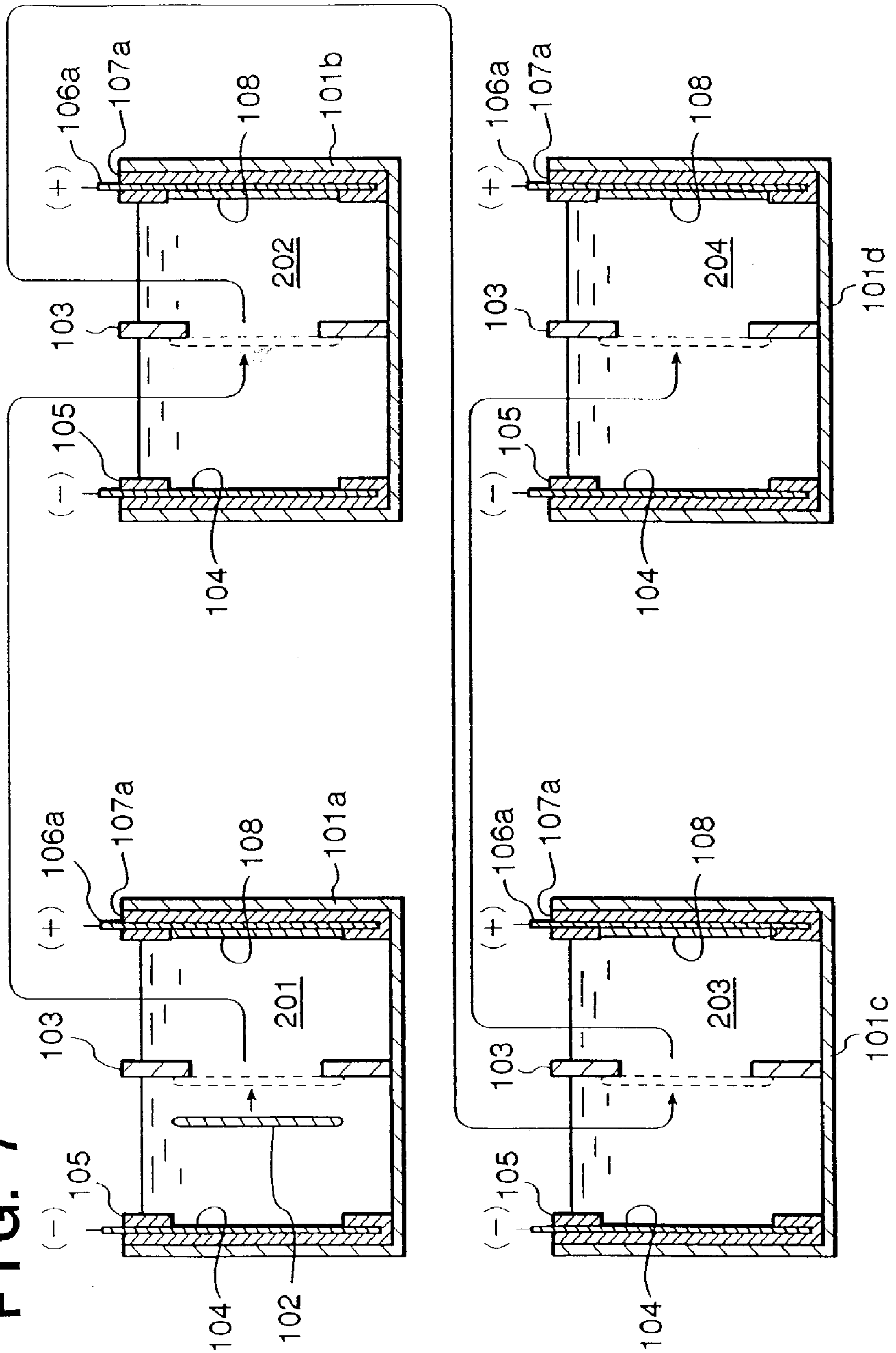
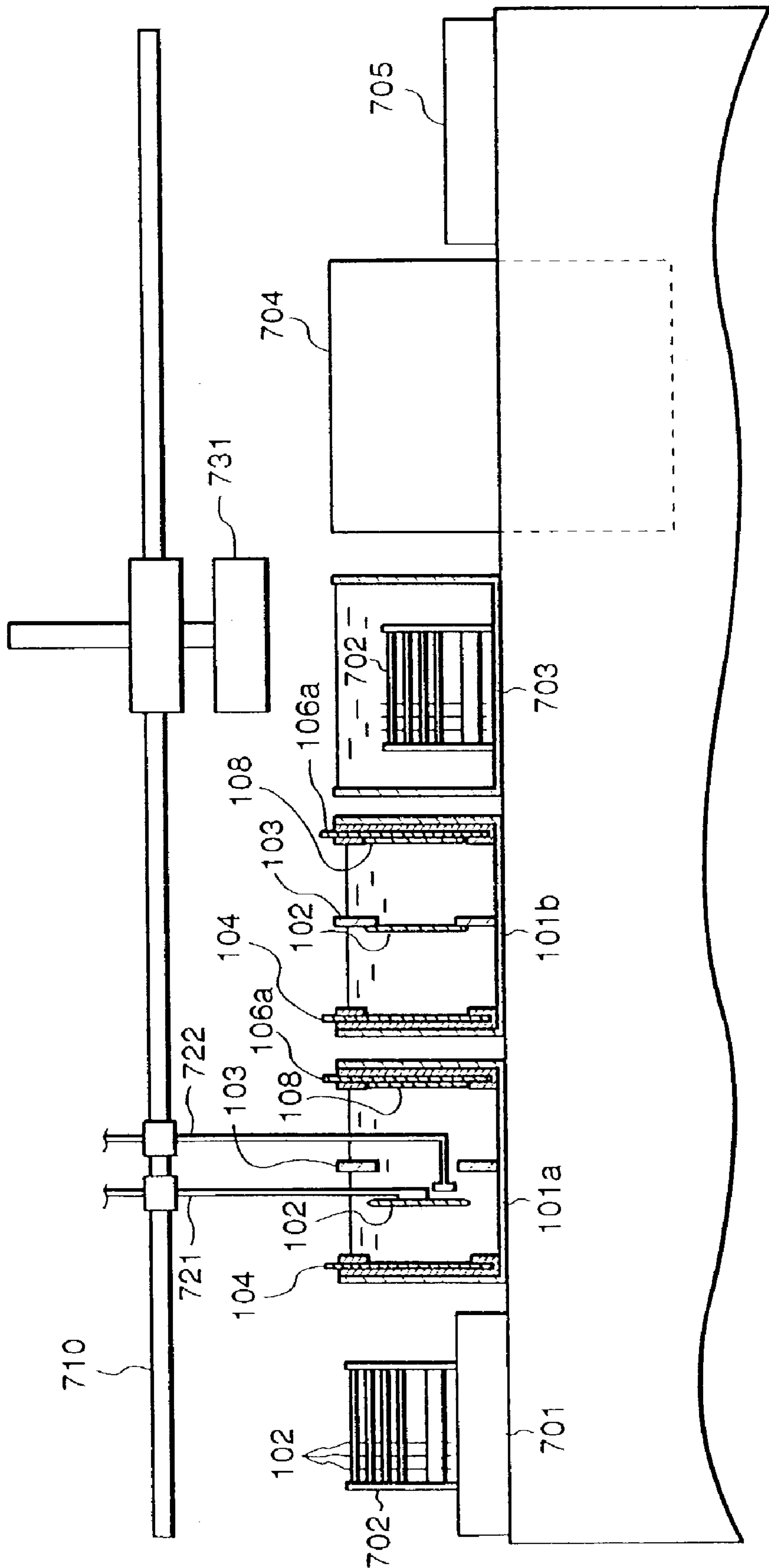


FIG. 7
(−)
(+)
105
104
102
103
201
106a
107a
108
101a
202
101b
203
101c
204
101d

FIG. 8



ANODIZING METHOD AND APPARATUS AND SEMICONDUCTOR SUBSTRATE MANUFACTURING METHOD

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an anodizing method and apparatus and a semiconductor substrate manufacturing method and, more particularly, to an anodizing method and apparatus for forming a porous layer on a substrate, and a semiconductor substrate manufacturing method using the anodizing method as part of the process.

[0003] 2. Description of the Related Art

[0004] A substrate (SOI substrate) having an SOI (Silicon On Insulator) structure is known as a substrate having a single-crystal Si layer on an insulating layer. A device using this SOI substrate has many advantages that cannot be achieved by ordinary Si substrates. Examples of the advantages are as follows.

[0005] (1) The integration degree can be increased because dielectric isolation is easy.

[0006] (2) The radiation resistance can be increased.

[0007] (3) The operating speed of the device can be increased because the stray capacitance is small. (

[0008] 4) No well step is necessary.

[0009] (5) Latch-up can be prevented.

[0010] (6) A completely depleted field-effect transistor can be formed by thin film formation.

[0011] Since an SOI structure has the above various advantages, researches have been made on its formation method for several decades.

[0012] As one SOI technology, the SOS (Silicon On Sapphire) technology by which Si is heteroepitaxially grown on a single-crystal sapphire substrate by CVD (Chemical Vapor Deposition) has been known for a long time. This SOS technology once earned a reputation as the most matured SOI technology. However, the SOS technology has not been put into practical use to date because, e.g., a large amount of crystal defects are produced by lattice mismatch in the interface between the Si layer and the underlying sapphire substrate, aluminum that forms the sapphire substrate mixes in the Si layer, the substrate is expensive, and it is difficult to obtain a large area.

[0013] Attempts have recently been made to realize the SOI structure without using any sapphire substrate. The attempts are roughly classified into two methods.

[0014] In the first method, the surface of a single-crystal Si substrate is oxidized, and a window is formed in the oxide film (SiO_2 layer) to partially expose the Si substrate. Single-crystal Si is epitaxially grown laterally using the exposed portion as a seed, thereby forming a single-crystal Si layer on SiO_2 (in this method, an Si layer is deposited on an SiO_2 layer).

[0015] In the second method, a single-crystal Si substrate itself is used as an active layer, and an SiO_2 layer is formed on the lower surface of the substrate (in this method, no Si layer is deposited) .

[0016] As a means for realizing the first method, a technique of directly epitaxially growing single-crystal Si in the horizontal direction from the single-crystal Si layer by CVD (CVD), a technique of depositing amorphous Si and epitaxially growing single-crystal Si laterally in the solid phase by annealing (solid phase epitaxial growth), a technique of irradiating an amorphous silicon layer or a polysilicon layer with a focused energy beam such as an electron beam or laser beam to grow a single-crystal Si layer on an SiO_2 layer by melting recrystallization (beam annealing), or a method of scanning band-shaped melting regions by a rod-like heater (zone melting recrystallization) is known.

[0017] All of these methods have both advantages and disadvantages and many problems of controllability, productivity, uniformity, and quality, and therefore have not been put into practical use in terms of industrial applications. For example, CVD requires sacrifice oxidation to form a flat thin film. Solid phase epitaxial growth is poor in crystallinity. In beam annealing, the process time required to scan the focused beam and controllability for beam superposition or focal point adjustment pose problems. Zone melting recrystallization is the most matured technique, and relatively large-scaled integrated circuits have been fabricated on a trial basis. However, since a number of crystal defects such as a subboundary undesirably remain, minority carrier devices cannot be created.

[0018] As the above second method, i.e., as the method without using the Si substrate as a seed for epitaxial growth, the following four techniques can be used.

[0019] As the first technique, an oxide film is formed on a single-crystal Si substrate having a V-shaped groove formed in the surface by anisotropic etching. A polysilicon layer having nearly the same thickness as that of the single-crystal Si substrate is deposited on the oxide film. After this, the single-crystal Si substrate is polished from the lower surface, thereby forming, on the thick polysilicon layer, a substrate having a single-crystal Si region surrounded and dielectrically isolated by the V-shaped groove. With this technique, a substrate having satisfactory crystallinity can be formed. However, there are problems of controllability and productivity in association with the process of depositing polysilicon as thick as several hundred micron or the process of polishing the single-crystal Si substrate from the lower surface to leave the isolated Si active layer.

[0020] The second technique is SIMOX (Separation by Ion Implanted Oxygen). In this technique, oxygen ions are implanted into a single-crystal Si substrate to form an SiO_2 layer. In this technique, to form an SiO_2 layer in a substrate, oxygen ions must be implanted at a dose of 10^{18} (ions/cm^2) or more. This implantation takes a long time to result in low productivity and high manufacturing cost. In addition, since a number of crystal defects are generated, the quality is too low to manufacture minority carrier devices.

[0021] As the third technique, an SOI structure is formed by dielectric isolation by oxidizing a porous Si layer. In this technique, an n-type Si island is formed on the surface of a p-type single-crystal Si substrate by proton ion implantation (Imai et al., J. Crystal Growth, vol. 63, 547 (1983)) or epitaxial growth and patterning. This substrate is anodized in an HF solution to convert only the p-type Si substrate around the n-type Si island into a porous structure. After this, the n-type Si island is dielectrically isolated by accelerated

oxidation. In this technique, since the Si region to be isolated must be determined before the device process, the degree of freedom in device design is limited.

[0022] As the fourth technique, an SOI structure is formed by bonding a single-crystal Si substrate to another thermally oxidized single-crystal Si substrate by annealing or an adhesive. In this technique, an active layer for forming a device must be uniformly thin. More specifically, a single-crystal Si substrate having a thickness of several hundred micron must be thinned down to the micron order or less.

[0023] To thin the substrate, polishing or selective etching can be used.

[0024] A single-crystal Si substrate can hardly be uniformly thinned by polishing. Especially, thinning to the submicron order, the variation range is several ten %. As the wafer size becomes large, this difficulty becomes more pronounced.

[0025] Selective etching is effective to uniformly thin the substrate. However, the selectivity ratio is as low as about 10^2, the surface planarity after etching is poor, and the crystallinity of the SOI layer is unsatisfactory.

[0026] A transparent substrate represented by a glass substrate is important in forming a contact sensor as a light-receiving element or a projection liquid crystal display device. To realize highly precise pixels (picture elements) having higher density and resolution for the sensor or display device, a high-performance driving element is required. For this purpose, a demand has arisen for a technique of forming a single-crystal Si layer having excellent crystallinity on a transparent substrate.

[0027] However, when an Si layer is deposited on a transparent substrate represented by a glass substrate, only an amorphous Si layer or a polysilicon layer is obtained. This is because the transparent substrate has an amorphous crystal structure, and the Si layer formed on the substrate reflects the disorderliness of the crystal structure of the transparent substrate.

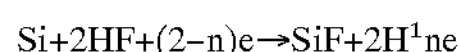
[0028] The present applicant has disclosed a new SOI technology in Japanese Patent Laid-Open No. 5-21338. In this technique, a first substrate obtained by forming a porous layer on a single-crystal Si substrate and a non-porous single-crystal layer on its surface is bonded to a second substrate via an insulating layer. After this, the bonded substrate stack is separated into two substrates at the porous layer, thereby transferring the non-porous single-crystal layer to the second substrate. This technique is advantageous because the film thickness uniformity of the SOI layer is good, the crystal defect density in the SOI layer can be decreased, the surface planarity of the SOI layer is good, no expensive manufacturing apparatus with special specifications is required, and SOI substrates having about several hundred angstrom to 10-μm thick SOI films can be manufactured by a single manufacturing apparatus.

[0029] The present applicant has also disclosed, in Japanese Patent Laid-Open No. 7-302889, a technique of bonding first and second substrates, separating the first substrate from the second substrate without destroying the first substrate, smoothing the surface of the separated first substrate, forming a porous layer again, and reusing the porous layer. Since the first substrate is not wasted, this technique is advantageous in largely reducing the manufacturing cost and simplifying the manufacturing process.

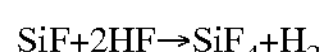
[0030] To separate the bonded substrate stack into two substrates while destroying neither of the first and second substrates, for example, the two substrates are pulled in opposite directions while applying a force in a direction perpendicular to the bonding interface, shearing stress is applied parallel to the bonding interface (for example, the two substrates are moved in opposite directions in a plane parallel to the bonding interface, or the two substrates are rotated in opposite directions while applying a force in the circumferential direction), a pressure is applied in a direction perpendicular to the bonding interface, a wave energy such as an ultrasonic wave is applied to the separation region, a peeling member (e.g., a sharp blade such as knife) is inserted into the separation region parallel to the bonding interface from the side surface side of the bonded substrate stack, the expansion energy of a substance filling the pores of the porous layer functioning as the separation region is used, the porous layer functioning as the separation region is thermally oxidized from the side surface of the bonded substrate stack to expand the volume of the porous layer and separate the substrates, or the porous layer functioning as the separation region is selectively etched from the side surface of the bonded substrate stack to separate the substrates.

[0031] Porous Si was found in 1956 by Uhlir et al. who were studying electropolishing of semiconductors (A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956)). Porous Si can be formed by anodizing an Si substrate in an HF solution.

[0032] Unagami et al. studied the dissolution reaction of Si upon anodizing and reported that holes were necessary for anodizing reaction of Si in an HF solution, and the reaction was as follows (T. Unagami, J. Electrochem. Soc., vol. 127, 476 (1980)).



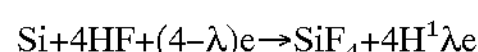
$$Si+2HF+(2-n)e \rightarrow SiF+2H^{1}ne$$



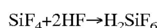
$$SiF+2HF \rightarrow SiF_4+H_2$$

$$SiF_4+2HF \rightarrow H_2SiF_6$$

[0033] or



$$Si+4HF+(4-\lambda)e \rightarrow SiF_4+4H^{1}\lambda e$$



$$SiF_4+2HF \rightarrow H_2SiF_6$$

[0034] where e and e each represent a hole and an electron, respectively, and n and λ are the number of holes necessary to dissolve one Si atom. According to them, when $n>2$ or $\lambda>4$, porous Si is formed.

[0035] The above fact suggests that p-type Si having holes is converted into porous Si while n-type Si is not converted. The selectivity in this conversion has been reported by Nagano et at. and Imai (Nagano, Nakajima, Anno, Onaka, and Kajiwara, IEICE Technical Report, vol. 79, SSD79-9549 (1979)), (K. Imai, Solid-State Electronics, vol. 24, 159 (1981)).

[0036] However, it has also been reported that n-type at a high concentration is converted into porous Si (R. P. Holmstrom and J. Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983)). Hence, it is important to select a substrate which can be converted into a porous Si substrate independently of p- or n-type.

[0037] To form a porous layer on an Si substrate, a pair of electrodes are supported in a process bath filled with an HF

solution, the Si substrate is held between the electrodes, and a current is flowed across the electrodes. In this process, the metal element of the anode dissolves into the HF solution to contaminate the Si substrate. The present applicant has disclosed an anodizing apparatus for solving this problem in Japanese Patent Laid-Open No. 6-275598. In the anodizing apparatus disclosed in Japanese Patent Laid-Open No. 6-275598, a conductive diaphragm formed from an Si material is inserted between an Si substrate and an anode, and contamination of the Si substrate by the metal element of the anode is prevented by this conductive electrode.

[**0038**] To facilitate separation of the bonded substrate stack, the porosity of the porous layer is preferably made large to some degree. To form a high-quality single-crystal Si layer on a porous layer, the porosity is preferably made small to some degree. Therefore, to facilitate separation of the bonded substrate stack and simultaneously form a high-quality single-crystal Si layer on the porous layer, a porous layer with a multilayered structure in which porous layers having different porosities are stacked is preferably formed.

SUMMARY OF THE INVENTION

[**0039**] The present invention has been made in consideration of the above requirement, and has as its object to provide a method and apparatus suitable to form a porous region with a multilayered structure, and a semiconductor substrate manufacturing method using this method.

[**0040**] According to an aspect of the present invention, there is provided an anodizing method of forming a porous layer on a substrate, characterized by comprising preparing an anodizing bath used to anodize a substrate, anodizing the substrate to be processed in a first electrolytic solution while holding the substrate between an anode and a cathode in the anodizing bath, exchanging the first electrolytic solution with a second electrolytic solution, and anodizing the substrate in the second electrolytic solution, thereby forming a porous layer having a multilayered structure on the substrate.

[**0041**] In the anodizing method, a current density of a current to be flowed across the anode and the cathode is preferably changed between anodizing using the first electrolytic solution and anodizing using the second electrolytic solution.

[**0042**] In the anodizing method, a conductive diaphragm is preferably inserted between the anode and the substrate to be processed to prevent contamination of the substrate by the anode.

[**0043**] In the anodizing method, the conductive diaphragm is preferably arranged to flow the whole current from the anode to the substrate to be processed through the conductive diaphragm.

[**0044**] In the anodizing method, the conductive diaphragm is preferably arranged to cover a surface of the anode that opposes a backside surface of the substrate to be processed.

[**0045**] In the anodizing method, the conductive diaphragm is preferably arranged to isolate an electrolytic solution in contact with a surface of the substrate to be processed, that is on the anode side, from an electrolytic solution in contact with the anode.

[**0046**] In the anodizing method, at least a surface of the conductive diaphragm that opposes the substrate to be processed is preferably formed from a silicon material.

[**0047**] The anodizing method preferably further comprises changing the conductive diaphragm every time an anodizing condition is changed.

[**0048**] The anodizing method preferably further comprises preparing a conductive diaphragm corresponding to each anodizing condition, and every time the anodizing condition is changed, using a conductive diaphragm corresponding to the condition.

[**0049**] The anodizing method preferably further comprises forming a porous layer having a relatively low porosity as a surface layer of the substrate to be processed, and forming a porous layer having a relatively high porosity as an underlayer of the surface layer.

[**0050**] The anodizing method preferably further comprises anodizing to form a porous layer having a porosity of not more than 30% as the surface layer.

[**0051**] The anodizing method preferably further comprises anodizing to form a porous layer having a porosity of not less than 30% as the underlayer of the surface layer.

[**0052**] The anodizing method preferably further comprises anodizing to form a porous layer having a thickness of not more than 5 μm as the underlayer of the surface layer.

[**0053**] According to another aspect of the present invention, there is provided an anodizing method of forming a porous layer on a substrate, characterized by comprising preparing at least two anodizing baths used to anodize a substrate, anodizing the substrate to be processed while holding the substrate between an anode and a cathode in one anodizing bath, and anodizing the substrate while holding the substrate between an anode and a cathode in the next anodizing bath, thereby forming a porous layer having a multilayered structure on the substrate.

[**0054**] In the other anodizing method, different electrolytic solutions are preferably used as electrolytic solutions used for anodizing in all or some of the at least two anodizing baths.

[**0055**] In the other anodizing method, a current density of a current to be flowed across the anode and the cathode is preferably changed in anodizing in all or some of the at least two anodizing baths.

[**0056**] In the other anodizing method, a conductive diaphragm is preferably inserted between the anode and the substrate to be processed to prevent contamination of the substrate by the anode.

[**0057**] In the other anodizing method, the conductive diaphragm is preferably arranged to flow the whole current from the anode to the substrate to be processed through the conductive diaphragm.

[**0058**] In the other anodizing method, the conductive diaphragm is preferably arranged to cover a surface of the anode that opposes a backside surface of the substrate to be processed.

[**0059**] In the other anodizing method, the conductive diaphragm is preferably arranged to isolate an electrolytic solution in contact with a surface of the substrate to be

processed, that is on the anode side, from an electrolytic solution in contact with the anode.

[0060] In the other anodizing method, at least a surface of the conductive diaphragm that opposes the substrate to be processed is preferably formed from a silicon material.

[0061] The other anodizing method preferably further comprises changing the conductive diaphragm every time an anodizing condition is changed.

[0062] The other anodizing method preferably further comprises preparing a conductive diaphragm corresponding to each anodizing condition, and every time the anodizing condition is changed, using a conductive diaphragm corresponding to the condition.

[0063] The other anodizing method preferably further comprises forming a porous layer having a relatively low porosity as a surface layer of the substrate to be processed, and forming a porous layer having a relatively high porosity as an underlayer of the surface layer.

[0064] The other anodizing method preferably further comprises anodizing to form a porous layer having a porosity of not more than 30% as the surface layer.

[0065] The other anodizing method preferably further comprises anodizing to form a porous layer having a porosity of not less than 30% as the underlayer of the surface layer.

[0066] The other anodizing method preferably further comprises anodizing to form a porous layer having a thickness of not more than 5 μm as the underlayer of the surface layer.

[0067] According to still another aspect of the present invention, there is provided a semiconductor substrate manufacturing method characterized by comprising the steps of processing a first substrate using any one of the above anodizing methods to form a porous layer having a multilayered structure on the first substrate, forming at least one non-porous layer on the porous layer, bonding a second substrate to a surface of the non-porous layer of the first substrate, separating a bonded substrate stack to a side of the first substrate and a side of the second substrate at a portion of the porous layer, and removing the porous layer left on the side of the separated second substrate.

[0068] The semiconductor substrate manufacturing method preferably further comprises the step of removing the porous layer left on the side of the separated first substrate to allow reuse of the first substrate.

[0069] In the semiconductor substrate manufacturing method, the separation step preferably comprises separating the bonded substrate stack at a portion having a high porosity in the porous layer having the multilayered structure.

[0070] In the semiconductor substrate manufacturing method, the non-porous layer preferably contains a single-crystal silicon layer.

[0071] In the semiconductor substrate manufacturing method, the non-porous layer preferably comprises a single-crystal silicon layer and a silicon oxide layer which are sequentially formed on the porous layer.

[0072] In the semiconductor substrate manufacturing method, the non-porous layer preferably contains a compound semiconductor layer.

[0073] In the semiconductor substrate manufacturing method, the second substrate preferably comprises a silicon substrate.

[0074] In the semiconductor substrate manufacturing method, the second substrate preferably comprises a substrate having a silicon oxide layer formed on a surface to be bonded to the first substrate.

[0075] In the semiconductor substrate manufacturing method, the second substrate preferably comprises a transparent substrate.

[0076] The semiconductor substrate manufacturing method preferably further comprises, after the step of removing the porous layer, the step of planarizing a surface layer on the side of the second substrate.

[0077] In the semiconductor substrate manufacturing method, the planarization step preferably comprises annealing in an atmosphere containing hydrogen.

[0078] In the semiconductor substrate manufacturing method, the step of removing the porous layer preferably comprises selectively etching the porous layer using, as an etchant, any one of

[0079] a) hydrofluoric acid,

[0080] b) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to hydrofluoric acid,

[0081] c) buffered hydrofluoric acid, and

[0082] d) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered hydrofluoric acid.

[0083] In the semiconductor substrate manufacturing method, the step of removing the porous layer preferably comprises selectively etching the porous layer using an etchant whose etching rate for the porous layer is higher than that for a compound semiconductor.

[0084] In the semiconductor substrate manufacturing method, the step of removing the porous layer preferably comprises selectively polishing the porous layer using the non-porous layer as a stopper.

[0085] In the semiconductor substrate manufacturing method, the bonding step preferably comprises the step of bringing the first substrate having the non-porous layer into tight contact with the second substrate.

[0086] In the semiconductor substrate manufacturing method, the bonding step preferably comprises, after the step of bringing the first substrate having the non-porous layer into tight contact with the second substrate, the step of performing a process selected from the group consisting of anode bonding, pressing, heating, and a combination thereof.

[0087] According to still another aspect of the present invention, there is provided an anodizing apparatus for forming a porous layer on a substrate, characterized by comprising an anodizing bath having an anode and a cathode, a plurality of tanks for storing electrolytic solutions to be supplied to the anodizing bath, a supply mechanism for

selectively supplying the electrolytic solution stored in any one of the plurality of tanks to the anodizing bath, and a drain mechanism for draining off the electrolytic solution from the anodizing bath back into the tank which supplied the electrolytic solution.

[**0088**] Preferably, the anodizing apparatus further comprises a holding mechanism for holding a conductive diaphragm between the anode and a substrate to be processed, and the conductive diaphragm prevents contamination of the substrate by the anode.

[**0089**] In the anodizing apparatus, the holding mechanism preferably holds the conductive diaphragm to flow a whole current from the anode to the substrate to be processed through the conductive diaphragm.

[**0090**] In the anodizing apparatus, the holding mechanism preferably holds the conductive-diaphragm to cover a surface of the anode that opposes a backside surface of the substrate to be processed.

[**0091**] In the anodizing apparatus, the holding mechanism preferably holds the conductive diaphragm to isolate an electrolytic solution in contact with a surface of the substrate to be processed, that is on the anode side, from an electrolytic solution in contact with the anode.

[**0092**] In the anodizing apparatus, at least a surface of the conductive diaphragm that opposes the substrate to be processed is preferably formed from a silicon material.

[**0093**] In the anodizing apparatus, the holding mechanism preferably detachably holds the conductive diaphragm.

[**0094**] According to still another aspect of the present invention, there is provided an anodizing apparatus for forming a porous layer on a substrate, characterized by comprising at least two anodizing baths each having an anode and a cathode, and a conveyor mechanism for conveying a substrate anodized in one anodizing bath into the next anodizing bath.

[**0095**] In the other anodizing apparatus, the substrate is preferably anodized in all or some of the at least two anodizing baths under different conditions.

[**0096**] The other anodizing apparatus preferably further comprises a cleaning unit for cleaning the substrate processed in the final anodizing bath of the at least two anodizing baths, and a drier unit for drying the substrate cleaned by the cleaning unit.

[**0097**] In the other anodizing apparatus, preferably each of the anodizing baths comprises a holding mechanism for holding a conductive diaphragm between the anode and the substrate to be processed, and the conductive diaphragm prevents contamination of the substrate by the anode.

[**0098**] In the other anodizing apparatus, the holding mechanism preferably holds the conductive diaphragm to flow a whole current from the anode to the substrate to be processed through the conductive diaphragm.

[**0099**] In the other anodizing apparatus, the holding mechanism preferably holds the conductive diaphragm to cover a surface of the anode that opposes the substrate to be processed.

[**0100**] In the other anodizing apparatus, the holding mechanism preferably holds the conductive diaphragm to isolate an electrolytic solution in contact with a surface of the substrate to be processed, that is on the anode side, from an electrolytic solution in contact with the anode.

[**0101**] In the other anodizing apparatus, at least a surface of the conductive diaphragm that opposes the substrate to be processed is preferably formed from a silicon material.

[**0102**] In the other anodizing apparatus, the holding mechanism preferably detachably holds the conductive diaphragm.

[**0103**] Further objects, features and advantages of the present invention will become apparent from the following detailed description of embodiments of the present invention with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0104**] **FIGS. 1A** to **1F** are views showing the steps of manufacturing a semiconductor substrate according to a preferred embodiment of the present invention;

[**0105**] **FIG. 2** is a view showing the schematic arrangement of an anodizing apparatus according to the first embodiment;

[**0106**] **FIG. 3** is a view showing the schematic arrangement of an anodizing apparatus according to the second embodiment;

[**0107**] **FIG. 4** is a view showing the schematic arrangement of an anodizing apparatus according to the third embodiment;

[**0108**] **FIG. 5** is a view showing a modification of the third embodiment;

[**0109**] **FIG. 6** is a view showing an improved example of an anodizing bath shown in **FIG. 5** which allows batch process of a number of substrates;

[**0110**] **FIG. 7** is a view showing the schematic arrangement of an anodizing apparatus according to the fourth embodiment; and

[**0111**] **FIG. 8** is a view showing the schematic arrangement of an automatic process line incorporating the anodizing apparatus shown in **FIG. 7**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[**0112**] Preferred embodiments of the present invention will be described below with reference to the accompanying drawings.

[**0113**] The steps of manufacturing a semiconductor substrate according to a preferred embodiment of the present invention will be described first. **FIGS. 1A** to **1F** are views showing the steps of manufacturing a semiconductor substrate according to this embodiment. In the step shown in **FIG. 1A, a** single-crystal Si substrate **11** is prepared, and two porous layers **12** and **13** having different porosities are formed on the upper surface side of the single-crystal Si substrate **11**. Three or more porous layers may be formed.

[**0114**] The uppermost porous layer **12** preferably has a low porosity of, e.g., 30% or less to form a high-quality epitaxial layer thereon. On the other hand, the second porous layer **13** preferably has a high porosity of, e.g., 30% or more

to facilitate separation. The thickness of the porous layer **13** is preferably, e.g., 5 μm or less.

[**0115**] In the step shown in **FIG.** 1B, at least one non-porous layer is formed on the uppermost porous layer **12**. The resultant structure is used as a first substrate. In the example shown in **FIG.** 1B, two non-porous layers **14** and **15** are formed. As the lower non-porous layer **14**, for example, a single-crystal Si layer is suitable. This single-crystal Si layer can be used as an active layer. As the non-porous layer **15** on the upper surface side, for example, an SiO_2 layer is suitable. This SiO_2 layer is suitable to separate the active layer from the bonding interface.

[**0116**] As the non-porous layer, a polysilicon layer, an amorphous Si layer, a metal layer, a compound semiconductor layer, or a superconductor layer is also suitable. A device such as a MOSFET may be formed on the non-porous layer at this time point.

[**0117**] In the step shown in **FIG.** 1C, the first substrate and an independently prepared second substrate **16** are brought into tight contact with each other at room temperature while sandwiching the non-porous layers. After this, the first and second substrates are bonded by anode bonding, pressing, heating, or a combination thereof.

[**0118**] When a single-crystal Si layer is formed as the non-porous layer **14**, the first and second substrates are preferably bonded after an SiO_2 layer is formed on the surface of the single-crystal Si layer by, e.g., thermal oxidation, as described above.

[**0119**] As the second substrate, an Si substrate having an SiO_2 layer formed thereon, a transparent substrate consisting of silica glass, quartz or a sapphire wafer is suitably used in addition to the Si substrate. However, the second substrate is not limited to this, and any other substrate can be used as far as it has a sufficiently flat surface to be bonded.

[**0120**] When the non-porous layer **14** is not formed from Si, or no Si substrate is used as the second substrate **16**, the non-porous layer **15** as an insulating layer need not be formed.

[**0121**] In bonding, another insulating thin plate may be inserted between the first and second substrates to form a three-layered structure.

[**0122**] In the step shown in **FIG.** 1D, the bonded substrate stack is separated into two substrates at the porous layer **13**. To separate the bonded substrate stack, for example, a fluid such as water is injected between the substrates, a pressure is applied, an external pressure such as a tensile or shearing force is applied, the porous Si layer **13** is oxidized to expand from the peripheral portion to generate an internal pressure in the porous Si layer **13**, thermal stress is applied to the porous layer **13** by heat changing in a pulse shape, or the porous layer **13** is softened. Any other methods can also be employed.

[**0123**] In the step shown in **FIG.** 1E, the porous layers **12** and **13** on the second substrate **16** are removed. When the non-porous layer **14** is a single-crystal Si layer, only the porous Si layers **12** and **13** are etched by electroless wet chemical etching using at least one etchant selected from a normal etchant for etching Si, hydrofluoric acid as an etchant for selectively etching porous Si, a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, or a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered hydrofluoric acid, thereby leaving the non-porous layers **14** and **15** on the second substrate **16**. Since the non-porous Si layer has a large surface area, only porous Si can be selectively etched even by a normal Si etchant, as described above.

[**0124**] Alternatively, the porous Si layers **12** and **13** may be selectively removed by polishing using the non-porous layer **14** as a polishing stopper.

[**0125**] When a compound semiconductor layer is formed as the non-porous layer **14**, only the porous Si layers **12** and **13** can be selectively chemically etched using an etchant whose etching rate for Si is higher than that for a compound semiconductor to leave a thin single-crystal compound semiconductor layer (non-porous layer **14**) on the second substrate **16**. Alternatively, the porous Si layers **12** and **13** may be selectively removed by polishing using the single-crystal compound semiconductor layer (non-porous layer **14**) as a polishing stopper.

[**0126**] **FIG. 1E** shows the semiconductor substrate manufactured by the above steps. According to the above steps, a flat non-porous thin film (e.g., a single-crystal Si thin film) having a uniform thickness can be formed in the entire region of the second substrate **16**.

[**0127**] For example, a semiconductor substrate having a single-crystal Si layer as the surface-side non-porous layer **14** and an SiO_2 layer as the inner non-porous layer **15** can be used as an SOI substrate. When an insulating substrate is used as the second substrate **16**, a semiconductor substrate suitable for forming an electrically insulated electronic element can be manufactured.

[**0128**] In the step shown in **FIG.** 1F, the porous layer **13** left on the first substrate side, i.e., on the single-crystal Si substrate **11** is removed. If the surface planarity falls outside the allowable range, the surface of the single-crystal Si substrate **11** is planarized. With this process, this substrate can be used as a substrate (single-crystal Si substrate **11**) for forming a first substrate, or the second substrate **16**.

[**0129**] Embodiments of an anodizing apparatus for performing the step shown in **FIG. 1A, i**.e., forming a porous layer having a multilayered structure will be described below.

[**0130**] [First Embodiment]

[**0131**] In an anodizing apparatus of this embodiment, every time one porous layer is formed, the electrolytic solution in an anodizing bath is exchanged to change the anodizing conditions, thereby forming a porous layer having a multilayered structure.

[**0132**] **FIG. 2** is a view showing the schematic arrangement of the anodizing apparatus according to the first embodiment. This anodizing apparatus comprises an anodizing bath **101**, solution tanks **121**, **122**, **131**, and **132**, and solution supply and removal mechanisms.

[**0133**] The anodizing bath **101** has a cathode (consisting of, e.g., platinum) **104**, a cathode holder **105** fixing the cathode **104** in the bath, an anode (consisting of, e.g., platinum) **106**, an anode holder **107** fixing the anode **106** in the bath, and a substrate holder **103** for fixing an Si substrate

102 to be processed between the pair of electrodes **104** and **106**. The substrate holder **103** has an opening portion for bringing the lower surface of the substrate **102** to be processed into contact with the portion of an electrolytic solution on the anode **106** side.

[**0134**] In the anodizing bath **101**, the cathode **104** side of the Si substrate **102** to be processed, i.e., the side on which a porous layer is formed on the Si substrate **102** is isolated from the anode **106** side of the Si substrate **102** when the Si substrate **102** is set on the substrate holder **103**.

[**0135**] The cathode side of the anodizing bath **101** is filled with an electrolytic solution in the tank **121** or **122**. The anode side is filled with an electrolytic solution in the tank **131** or **132**.

[**0136**] The electrolytic solution filling the cathode side of the anodizing bath **101** and that filling the anode side may be the same electrolytic solution or different electrolytic solutions. As the electrolytic solution filling the cathode side of the anodizing bath **101**, an electrolytic solution essential for anodizing, i.e., an electrolytic solution containing HF must be used. However, the electrolytic solution filling the anode side need only have an appropriate conductivity. To prevent any adverse influence resulting from mixing of the electrolytic solution on the cathode side with that on the anode side, the two electrolytic solutions are preferably of the same type.

[**0137**] A description will be made below assuming that first electrolyte solutions **141** and **151** are stored in the first and second tanks **121** and **131**, respectively, and first electrolyte solutions **142** and **152** different from the first electrolytic solution are stored in the third and fourth tanks **122** and **132**, respectively. Different electrolytic solutions mean electrolytic solutions having different mixing ratios of chemical substances or electrolytic solutions having different compositions.

[**0138**] In this anodizing apparatus, first, the Si substrate **102** is anodized using the first electrolyte solutions **141** and **151** to form a first porous layer. Subsequently, the Si substrate **102** is anodized using the second electrolyte solutions **142** and **152** to form a second porous layer.

[**0139**] The flow of process by the anodizing apparatus will be described below in detail.

[**0140**] First, the electrolytic solution in the anodizing bath **101** is drained off, and valves **161** and **163** are closed. In this state, the Si substrate **102** to be processed is conveyed to the substrate holder **103** by an automatic conveyor robot or the like and fixed by a vacuum chuck mechanism (not shown) by chucking.

[**0141**] A valve **162** is opened to the first tank **121** side. The first electrolyte solution **141** is pumped up by a pump **172** and supplied to the cathode side of the anodizing bath **101** through a filter **181**. Simultaneously, a valve **164** is opened to the second tank **131** side. The first electrolyte solution **151** is pumped up by a pump **174** and supplied to the anode side of the anodizing bath **101** through a filter **182**.

[**0142**] When the cathode and anode sides of the anodizing bath **101** are filled with the first electrolyte solutions **141** and **151**, respectively, a current having a first current value is flowed across the cathode **104** and the anode **106** for a predetermined time to anodize the Si substrate **102**, thereby forming a first porous layer on the cathode side of the Si substrate **102**.

[**0143**] Subsequently, to exchange the first electrolytic solutions in the anodizing bath **101** with the second electrolytic solutions, the valve **161** is opened to the first tank **121** side. The first electrolyte solution is drained off by a pump **171** from the lower portion of the anodizing bath **101** on the cathode side into the first tank **121**, and the valve **161** is closed. Simultaneously, the valve **163** is opened to the second tank **131** side. The first electrolyte solution is drained off by a pump **173** from the lower portion of the anodizing bath **101** on the anode side into the second tank **131**, and the valve **163** is closed.

[**0144**] Next, the valve **162** is opened to the third tank **122** side. The second electrolyte solution **142** is pumped up by the pump **172** and supplied to the cathode side of the anodizing bath **101** through the filter **181**. Simultaneously, the valve **164** is opened to the fourth tank **132** side. The second electrolyte solution **152** is pumped up by the pump **174** and supplied to the anode side of the anodizing bath **101** through the filter **182**. The interior of the anodizing bath **101** is preferably cleaned by a cleaning solution such as water before the second electrolyte solutions **142** and **152** are supplied to the anodizing bath **101**. Upon completing cleaning, the cleaning solution is preferably completely drained off from the anodizing bath **101** to prevent any adverse influence on the electrolytic solutions to be supplied next.

[**0145**] When the cathode and anode sides of the anodizing bath **101** are filled with the second electrolyte solutions **142** and **152**, respectively, a current having a second current value is flowed across the cathode **104** and the anode **106** for a predetermined time to anodize the Si substrate **102**, thereby forming a second porous layer on the cathode side of the Si substrate **102**. The second porous layer is formed on the lower side of the first porous layer.

[**0146**] The valve **161** is opened to the third tank **122** side. The second electrolyte solution is drained off by the pump **171** from the lower portion of the anodizing bath **101** on the cathode side into the third tank **122**, and the valve **161** is closed. Meanwhile, the valve **163** is opened to the fourth tank **132** side. The second electrolyte solution is drained off by the pump **173** from the lower portion of the anodizing bath **101** on the anode side into the fourth tank **132**, and the valve **163** is closed. After the second electrolyte solutions **142** and **152** are drained off, the interior of the anodizing bath **101** is preferably cleaned by a cleaning solution such as water. Upon completing cleaning, the cleaning solution is preferably completely drained off from the anodizing bath **101** to prevent any adverse influence on the electrolytic solutions to be supplied next.

[**0147**] After formation of the second porous layer, a third porous layer may be formed by filling the anodizing bath **101** with the first electrolyte solutions **141** and **151** again or another electrolytic solution. More porous layers may be formed by repeating this process.

[**0148**] [Second Embodiment]

[**0149**] An anodizing apparatus of this embodiment has a plurality of anodizing baths. With this arrangement, every time one porous layer is formed, the anodizing bath is exchanged, thereby forming a porous layer having a multi-layered structure.

[0150] **FIG. 3** is a view showing the schematic arrangement of the anodizing apparatus according to the second embodiment. This anodizing apparatus is used to form a porous layer having a four-layered structure and comprises four anodizing baths **101***a*, **101***b*, **101***c*, and **101***d*. Each of the anodizing baths **101***a*, **101***b*, **101***c*, and **101***d* substantially has the same arrangement as that of the anodizing bath **101** shown in **FIG. 2** and comprises a pair of electrodes **104** and **106** and a substrate holder **103**.

[0151] The anodizing baths **101***a*, **101***b*, **101***c*, and **101***d* are filled with first, second, third, and fourth first electrolyte solutions **201**, **202**, **203**, and **204**, respectively. The third electrolyte solution **203** may be the same as the first electrolyte solution **201**. The fourth electrolyte solution **204** may be the same as the first or second electrolyte solution **201** or **202**.

[0152] According to this anodizing apparatus, after an Si substrate **102** is processed in one anodizing bath, the Si substrate **102** is transferred to another anodizing bath filled with a different electrolytic solution to change the anodizing conditions, and the next process is executed. Hence, the electrolytic solution need not be exchanged every time one porous layer is formed In addition, since a free anodizing bath can be used to process the next Si substrate **102**, high throughput can be realized.

[0153] More specifically, first, the Si substrate **102** is set on the substrate holder **103** of the first anodizing bath **101***a* filled with the first electrolyte solution **201** and anodized under the first conditions. Subsequently, the Si substrate **102** is set on the substrate holder **103** of the second anodizing bath **101***b* filled with the second electrolyte solution **202**, and anodized under the second conditions. Then, the Si substrate **102** is set on the substrate holder **103** of the third anodizing bath **101***c* filled with the third electrolyte solution **203** and anodized under the third conditions. Finally, the Si substrate **102** is set on the substrate holder **103** of the fourth anodizing bath **101***d* filled with the fourth electrolyte solution **204** and anodized under the fourth conditions.

[0154] [Third Embodiment]

[0155] This embodiment is an improvement of the anodizing apparatus of the first embodiment. In the anodizing apparatus according to the third embodiment, an Si substrate **102** to be processed is prevented from being contaminated by the metal material (e.g., platinum) of an anode, which is dissolved into an electrolytic solution.

[0156] **FIG. 4** is a view showing the schematic arrangement of the anodizing apparatus according to the third embodiment.

[0157] In this anodizing apparatus, a conductive diaphragm **108** for preventing contamination of the electrolytic solution and the Si substrate **102** to be processed is inserted between an anode **106***a* and the electrolytic solution. This conductive diaphragm **108** is preferably comprised of an Si substrate and, more specifically, an Si substrate having almost the same resistivity as that of the Si substrate **102** to be processed. When the conductive diaphragm **108** is formed from the same material as that of the Si substrate **102** to be processed, the Si substrate **102** to be processed can be prevented from being contaminated.

[0158] The conductive diaphragm **108** is preferably detachable. In the example shown in **FIG. 4**, for example, a vacuum chuck mechanism is preferably arranged on the surface of the anode **106***a* or in an anode holder **107***a* The conductive diaphragm **108** and anode **106***a* need be electrically connected. When a gap is formed between the conductive diaphragm **108** and the anode **106***a*, the gap must be filled with a conductive solution or a conductive material.

[0159] When an Si substrate is to be processed using this anodizing apparatus, the conductive diaphragm **108** is set on the anode holder **107***a*, and then, an anodizing bath **101** is filled with first electrolyte solutions **141** and **151** to process the Si substrate **102**. After this, the Si substrate **102** may be processed after exchanging the first electrolyte solutions **141** and **151** with second electrolyte solutions **142** and **152** without exchanging the conductive diaphragm **108**.

[0160] However, for example, when an Si substrate of the same type as the Si substrate to be processed is used as the conductive diaphragm, and an electrolytic solution (e.g., a solution containing HF) is used as the electrolytic solutions **151** and **152** filling the anode **106***a* side, the conductive diaphragm is preferably exchanged with a diaphragm dedicated to each electrolytic solution every time the electrolytic solution is exchanged. The reason for this is as follows.

[0161] When the space between the Si substrate **102** to be processed and the conductive diaphragm **108** is filled with an electrolytic solution such as a solution containing HF, and anodizing is performed, a porous layer is formed not only on the cathode side of the Si substrate **102** to be processed but also on the cathode side of the conductive diaphragm **108**. When the process of forming a porous layer having a multilayered structure while changing the anodizing conditions is repeated for the number of Si substrates **102**, a thick multilayered structure of a number of porous layers with different porosities is formed on the conductive diaphragm **108**. Finally, the porous layers break to contaminate the interior of the bath or Si substrate to be processed. The probable causes for break of the porous layers on the conductive diaphragm **108** are as follows.

[0162] 1) Since porous layers having different porosities are stacked, the pore walls cannot withstand stress.

[0163] 2) When a porous layer having a high porosity is formed under (inside) a porous layer having a low porosity, the porosity of the porous layer with a high porosity increases in proportion to the depth from the surface of the conductive diaphragm **108** to the porous layer (the total thickness of the porous layers). Hence, when a number of Si substrates are processed, the porosity of the porous layer formed at the deepest portion of the conductive diaphragm **108** reaches the critical value to break the pore walls.

[0164] Break of pore walls hardly occurs when anodizing is repeated under the same condition. This is because a nearly constant porosity is maintained in the direction of depth of the conductive diaphragm **108**.

[0165] A suitable process procedure of forming a porous layer using this anodizing apparatus will be described below. In this case, assume that a porous layer having a multilayered structure is to be formed on each of 25 Si substrates.

[0166] First, the electrolytic solution in the anodizing bath **101** is drained off, and valves **161** and **163** are closed. In this state, the conductive diaphragm **108** for the first electrolyte

solution **151** is conveyed and fixed on the anode holder **107***a* by an automatic conveyor robot or the like.

[**0167**] The first Si substrate **102** to be processed is conveyed and fixed on a substrate holder **103** by an automatic conveyor robot or the like.

[**0168**] A valve **162** is opened to the first tank **121** side. The first electrolyte solution **141** is pumped up by a pump **172** and supplied to the cathode side of the anodizing bath **101** through a filter **181**. Simultaneously, a valve **164** is opened to the second tank **131** side. The first electrolyte solution **151** is pumped up by a pump **174** and supplied to the anode side of the anodizing bath **101** through a filter **182**.

[**0169**] When the cathode and anode sides of the anodizing bath **101** are filled with the first electrolyte solutions **141** and **151**, respectively, a current having a first current value is flowed across a cathode **104** and the anode **106***a* for a predetermined time to anodize the first Si substrate **102**, thereby forming a first porous layer on the cathode side of the Si substrate **102**.

[**0170**] The valve **161** is opened to the first tank **121** side. The first electrolyte solution is drained off by a pump **171** from the lower portion of the anodizing bath **101** on the cathode side into the first tank **121**, and the valve **161** is closed. In the mean time, the valve **163** is opened to the second tank **131** side. The first electrolyte solution is drained off by a pump **173** from the lower portion of the anodizing bath **101** on the anode side into the second tank **131**, and the valve **163** is closed.

[**0171**] The first Si substrate **102** fixed on the substrate holder **103** is exchanged with the second Si substrate **102**.

[**0172**] The valve **162** is opened to the first tank **121** side. The first electrolyte solution **141** is pumped up by the pump **172** and supplied to the cathode side of the anodizing bath **101** through the filter **181**. Also, the valve **164** is opened to the second tank **131** side. The first electrolyte solution **151** is pumped up by the pump **174** and supplied to the anode side of the anodizing bath **101** through the filter **182**.

[**0173**] When the cathode and anode sides of the anodizing bath **101** are filled with the first electrolyte solutions **141** and **151**, respectively, a current having a first current value is flowed across the cathode **104** and the anode **106***a* for a predetermined time to anodize the second Si substrate **102**, thereby forming a first porous layer on the cathode side of the Si substrate **102**.

[**0174**] This process is repeated until the 25th Si substrate **102**.

[**0175**] Subsequently, to exchange the first electrolytic solutions in the anodizing bath **101** with the second electrolytic solutions, the valve **161** is opened to the first tank **121** side. The first electrolyte solution is drained off by the pump **171** from the lower portion of the anodizing bath **101** on the cathode side into the first tank **121**, and the valve **161** is closed. Simultaneously, the valve **163** is opened to the second tank **131** side. The first electrolyte solution is drained off by the pump **173** from the lower portion of the anodizing bath **101** on the anode side into the second tank **131**, and the valve **163** is closed.

[**0176**] The conductive diaphragm **108** for the second electrolyte solution **152** is conveyed and fixed on the anode holder **107***a* by an automatic conveyor robot or the like.

[**0177**] Next, the valve **162** is opened to the third tank **122** side. The second electrolyte solution **142** is pumped up by the pump **172** and supplied to the cathode side of the anodizing bath **101** through the filter **181**. Simultaneously, the valve **164** is opened to the fourth tank **132** side. The second electrolyte solution **152** is pumped up by the pump **174** and supplied to the anode side of the anodizing bath **101** through the filter **182**. The interior of the anodizing bath **101** is preferably cleaned by a cleaning solution such as water before the second electrolyte solutions **142** and **152** are supplied to the anodizing bath **101**. Upon completing cleaning, the cleaning solution is preferably completely drained off from the anodizing bath **101** to prevent any adverse influence on the electrolytic solutions to be supplied next.

[**0178**] When the cathode and anode sides of the anodizing bath **101** are filled with the second electrolyte solutions **142** and **152**, respectively, a current having a second current value is flowed across the cathode **104** and the anode **106***a* for a predetermined time to anodize the Si substrate **102**, thereby forming a second porous layer on the cathode side of the Si substrate **102**. The second porous layer is formed on the lower side of the first porous layer.

[**0179**] The valve **161** is opened to the third tank **122** side. The second electrolyte solution is drained off by the pump **171** from the lower portion of the anodizing bath **101** on the cathode side into the third tank **122**, and the valve **161** is closed. At the same time, the valve **163** is opened to the fourth tank **132** side. The second electrolyte solution is drained off by the pump **173** from the lower portion of the anodizing bath **101** on the anode side into the fourth tank **132**, and the valve **163** is closed.

[**0180**] The first Si substrate **102** fixed on the substrate holder **103** is exchanged with the second Si substrate **102**.

[**0181**] Next, the valve **162** is opened to the third tank **122** side. The second electrolyte solution **142** is pumped up by the pump **172** and supplied to the cathode side of the anodizing bath **101** through the filter **181**. Simultaneously, the valve **164** is opened to the fourth tank **132** side. The second electrolyte solution **152** is pumped up by the pump **174** and supplied to the anode side of the anodizing bath **101** through the filter **182**.

[**0182**] When the cathode and anode sides of the anodizing bath **101** are filled with the second electrolyte solutions **142** and **152**, respectively, a current having a second current value is flowed across the cathode **104** and the anode **106***a* for a predetermined time to anodize the Si substrate **102**, thereby forming a second porous layer on the cathode side of the Si substrate **102**.

[**0183**] This process is repeated until the 25th Si substrate **102**.

[**0184**] Finally, the valve **161** is opened to the third tank **122** side. The second electrolyte solution is drained off by the pump **171** from the lower portion of the anodizing bath **101** on the cathode side into the third tank **122**, and the valve **161** is closed. Also, the valve **163** is opened to the fourth tank **132** side. The second electrolyte solution is drained off by the pump **173** from the lower portion of the anodizing bath **101** on the anode side into the fourth tank **132**, and the valve **163** is closed. After the second electrolyte solutions **142** and **152** are drained off, the interior of the anodizing bath **101** is preferably cleaned by a cleaning solution such as

water. Upon completing cleaning, the cleaning solution is preferably completely drained off from the anodizing bath **101** to prevent any adverse influence on the electrolytic solutions to be supplied next.

[0185] In the above series of processes, every time the Si substrate **102** is exchanged, the electrolytic solutions are temporarily drained off from the anodizing bath **101**. However, when electrolytic solutions of the same type are supplied to both the cathode and anode sides of the anodizing bath **101** and, especially, when corrosion of the automatic conveyor robot for conveying the Si substrate **102** need not be taken into consideration, the Si substrate **102** can be exchanged while keeping the anodizing bath **101** filled with electrolytic solutions.

[0186] After formation of the second porous layer, a third porous layer may be formed by filling the anodizing bath **101** with the first electrolyte solutions **141** and **151** again or another electrolytic solution. More porous layers may be formed by repeating this process.

[0187] **FIG. 5** is a view showing a modification of the third embodiment. An anodizing bath **301** shown in **FIG. 5** has a conductive diaphragm holder **103***a* exclusively used to hold the conductive diaphragm **108** in place. The anodizing bath **301** is used while filling the gap between the conductive diaphragm **108** and the anode **106** with a conductive solution. This conductive solution is used to simply electrically connect the conductive diaphragm **108** and anode **106** and therefore need not be exchanged every time a porous layer having a multilayered structure is formed on the Si substrate **102** to be processed. The anodizing bath **301** is replaced with, e.g., the anodizing bath **101** shown in **FIG. 4**.

[0188] **FIG. 6** is a view showing an improvement example of the anodizing bath shown in **FIG. 5** which allows batch process of a number of substrates. An anodizing bath **401** has a plurality of substrate holders **103**.

[0189] In this embodiment, the conductive diaphragm and Si substrate to be processed are electrically connected by filling the gap therebetween with a conductive solution However, the conductive diaphragm and Si substrate to be processed may be brought into direct contact with each other.

[0190] [Fourth Embodiment]

[0191] This embodiment is an improvement of the anodizing apparatus of the second embodiment. The anodizing apparatus according to the fourth embodiment has a means for preventing an Si substrate **102** to be processed from being contaminated by the metal material (e.g., platinum) of an anode **106***a*, which is dissolved into an electrolytic solution.

[0192] **FIG. 7** is a view showing the schematic arrangement of the anodizing apparatus according to the fourth embodiment.

[0193] In this anodizing apparatus, a conductive diaphragm **108** for preventing contamination of the electrolytic solution and the Si substrate **102** to be processed is inserted between the anode **106***a* and the electrolytic solution. This conductive diaphragm **108** is preferably comprised of an Si substrate and, more specifically, an Si substrate having almost the same resistivity as that of the Si substrate **102** to be processed. When the conductive diaphragm **108** is formed from the same material as that of the Si substrate **102** to be processed, the Si substrate **102** to be processed can be prevented from being contaminated.

[0194] The conductive diaphragm **108** is preferably detachable. In the example shown in **FIG. 7**, for example, a vacuum chuck mechanism is preferably disposed on the surface of the anode **106***a* or in an anode holder **107***a*. The conductive diaphragm **108** and anode **106***a* need be electrically connected. When a gap is formed between the conductive diaphragm **108** and the anode **106***a*, the gap must be filled with a conductive solution or a conductive material.

[0195] The anodizing apparatus of this embodiment has a plurality of anodizing baths. With this arrangement, every time one porous layer is formed, the anodizing bath is exchanged, thereby forming a porous layer having a multilayered structure. Since anodizing can be executed under the same conditions in each anodizing bath, the problem described in the third embodiment, i.e., the problem of break of the conductive diaphragm **108** need not be taken into consideration. Since the conductive diaphragm **108** need not be frequently exchanged, this anodizing apparatus is excellent in throughput.

[0196] The process procedure by this anodizing apparatus is the same as in the second embodiment.

[0197] Each of first anodizing baths **101***a*, **101***b*, **101***c*, and **101***d* of the anodizing apparatus of this embodiment may be replaced with the anodizing bath **301** shown in **FIG. 5** or anodizing bath **401** shown in **FIG. 6**.

[0198] In this embodiment, the conductive diaphragm and Si substrate to be processed are electrically connected by filling the gap therebetween with a conductive solution. However, the conductive diaphragm and Si substrate to be processed may be brought into direct contact with each other.

[0199] **FIG. 8** is a view showing the schematic arrangement of an automatic process line incorporating the anodizing apparatus shown in **FIG. 7**. This automatic manufacturing line has two anodizing baths **101***a* and **101***b* for forming a porous layer having a two layered structure. Three or more anodizing baths may also be used, as a matter of course.

[0200] The process procedure by this automatic manufacture line will be described below.

[0201] A wafer carrier **702** storing Si substrates **102** to be processed is mounted on a loader **701**. The start of the process is instructed by operating a control panel (not shown).

[0202] In response to this, a first conveyor robot **721** extracts one Si substrate **102** from the wafer carrier **702** by chucking it from the lower surface and dips it into the first anodizing bath **101***a* on the cathode **104** side. A second conveyor robot **722** receives the Si substrate **102** by chucking it from the lower surface and moves the Si substrate **102** to a position where the Si substrate **102** comes into contact with the chuck surface of a substrate holder **103**. In this state, the vacuum chuck mechanism of the substrate holder **103** is activated to chuck the Si substrate **102** on the chuck surface.

[0203] A predetermined current is flowed across the electrodes **104** and **106***a* of the first anodizing bath **101***a*, thereby forming a first porous layer on the surface of the Si substrate **102**.

[0204] After the second conveyor robot **722** chucks the Si substrate **102** in the first anodizing bath **101***a* by chucking it from the lower surface, and vacuum chuck by the substrate holder **103** is canceled, the Si substrate **102** is separated from the substrate holder **103**. The Si substrate **102** is transferred from the second conveyor robot **722** to the first conveyor robot **721**.

[0205] The Si substrate **102** is conveyed to the second anodizing bath **101***b* by the first conveyor robot **721**, transferred to the second conveyor robot **722**, and set on the substrate holder **103** of the second anodizing bath **101***b*.

[0206] A predetermined current is flowed across the electrodes **104** and **106***a* of the second anodizing bath **101***b*, thereby forming a second porous layer under the first porous layer on the Si substrate **102**.

[0207] After the second conveyor robot **722** chucks the Si substrate **102** in the second anodizing bath **101***b* by chucking it from the lower surface, and vacuum chuck by the substrate holder **103** is canceled, the Si substrate **102** is separated from the substrate holder **103**. The Si substrate **102** is transferred from the second conveyor robot **722** to the first conveyor robot **721**.

[0208] The Si substrate **102** is stored by the first conveyor robot **721** in the wafer carrier **702** which has been dipped into a washing tank **703** in advance.

[0209] The above process is continuously executed to process all the Si substrates **102** in the wafer carrier **702** on the loader **701** and store them in the wafer carrier **702** in the washing tank **703**. After this, the Si substrates **102** are cleaned.

[0210] Finally, a third conveyor robot **731** extracts the Si substrates **102** in the washing bath **703** while keeping them stored in the wafer carrier **702** and conveys them to a spin drier **704**. After the Si substrates **102** are dried by the spin drier **704**, the third conveyor robot **731** conveys the Si substrates **102** onto an unloader **705** while keeping them stored in the wafer carrier **702**.

[0211] Examples of anodizing by the above anodizing apparatuses will be described next.

EXAMPLE 1

[0212] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a two-layered structure was formed. The first and second anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	11 (min)
Thickness of porous Si layer (target):	12 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	10 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:2:2
Process time:	3 (min)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 35%

[0213] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a two-layered structure could be manufactured. In each of the apparatuses of the second and fourth anodizing apparatuses, two anodizing baths were used.

[0214] In the anodizing apparatus of the third embodiment, after a first porous layer was formed on each of 25 Si substrates, the electrolytic solutions and conductive diaphragm were exchanged, and a second porous layer was formed on each of the 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0215] In the anodizing apparatus of the fourth embodiment, first and second porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

EXAMPLE 2

[0216] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a three-layered structure was formed. The first to third anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	11 (min)
Thickness of porous Si layer (target):	12 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	10 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:2:2
Process time:	3 (min)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 35%
<Third Anodizing Conditions>	
Current density:	7 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	1 (min)
Thickness of porous Si layer (target):	1.1 (μm)
Porosity (target):	to 25%

[0217] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a three-layered structure could be manufactured. In each of the anodizing apparatuses of the first and third embodiments, the anodizing solution for the first and third anodizing processes was supplied from the first and second tanks, and the anodizing solution for the second anodizing process was supplied from the third and fourth tanks. In each of the anodizing apparatuses of the second and fourth embodiments, three anodizing baths were used.

[0218] In the anodizing apparatus of the third embodiment, a first conductive diaphragm was set, and a first porous

layer was formed on each of 25 Si substrates under the first anodizing conditions. Subsequently, a second conductive diaphragm was set, and a second porous layer was formed on each of the 25 Si substrates under the second anodizing conditions. Then, a third conductive diaphragm was set, and a third porous layer was formed on each of the 25 Si substrates under the third anodizing conditions. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0219] In the anodizing apparatus of the fourth embodiment, first to third porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

EXAMPLE 3

[0220] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a two-layered structure was formed. The first and second anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	5 (min)
Thickness of porous Si layer (target):	6 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	30 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	110 (sec)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 40%

[0221] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a two-layered structure could be manufactured. In each of the apparatuses of the second and fourth anodizing apparatuses, two anodizing baths were used.

[0222] In the anodizing apparatus of the third embodiment, after a first porous layer was formed on each of 25 Si substrates, the electrolytic solutions and conductive diaphragm were exchanged, and a second porous layer was formed on each of the 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0223] In the anodizing apparatus of the fourth embodiment, first and second porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

EXAMPLE 4

[0224] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a two-layered structure was formed. The first and second anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	11 (min)
Thickness of porous Si layer (target):	12 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	10 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:2:2
Process time:	3 (min)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 35%

[0225] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a two-layered structure could be manufactured. In each of the apparatuses of the second and fourth anodizing apparatuses, two anodizing baths were used.

[0226] In the anodizing apparatus of the third embodiment, after a first porous layer was formed on each of 25 Si substrates, the electrolytic solutions and conductive diaphragm were exchanged, and a second porous layer was formed on each of the 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0227] In the anodizing apparatus of the fourth embodiment, first and second porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0228] The substrate having a porous layer was oxidized in an oxygen atmosphere at 400° C. for 1 hr. Upon this oxidation, the inner wall of each pore in the porous Si layer was covered by a thermal oxide film.

[0229] Next, a 0.3-μm thick single-crystal Si layer was epitaxially grown on the porous Si layer by CVD (Chemical Vapor Deposition). The growth conditions were as follows. Since the surface of the porous Si layer is exposed to H_2 in the initial stage of epitaxial growth, the surface pores are filled to planarize the surface.

<Epitaxial Growth Conditions>	
Source gas:	SiH_2Cl_2/H_2
Gas flow rate:	0.5/100 (liter/min)
Gas pressure:	80 (Torr)
Temperature:	950 (° C.)
Growth rate:	0.3 (μm/min)

[0230] Subsequently, a 200-nm thick SiO_2 layer was formed on the surface of the epitaxially grown single-crystal Si layer by thermal oxidation (completion of the first substrate).

[0231] The surface of this SiO_2 layer was brought into tight contact with the surface of an independently prepared Si substrate (second substrate), and these substrates were bonded by annealing at 1,000° C. for one hr.

[0232] A water jet with a diameter of 0.2 mm was injected to the beveling gap of the bonded substrate stack to separate the bonded substrate stack into two substrates at the second (lower) porous Si layer.

[0233] The porous Si layer left on the second substrate side was etched using a mixed solution of 49% hydrofluoric acid, 30% hydrogen peroxide, and water. At this time, the single-crystal Si layer functioned as an etching stopper, so the porous Si layer was selectively etched.

[0234] The etching rate of non-porous single-crystal Si by the etchant is very low, and the ratio of the etching rate of porous single crystal Si to non-porous single-crystal Si reaches 10^5 or more. For this reason, the etching amount (about several ten angstrom) of the non porous layer can be neglected for practical use.

[0235] With the above process, an SOI substrate having a 0.2-μm thick single-crystal Si layer on the Si oxide film was obtained. The thickness of the single-crystal Si layer of this SOI substrate was measured at 100 points on the entire surface. The film thickness uniformity was 201 nm±4 nm.

[0236] The resultant structure was annealed in hydrogen at 1,100° C. for 1 hr, and the surface roughness was evaluated with an atomic force microscope. The root mean square roughness in a 50-μm square area was approximately 0.2 nm. This nearly equals that of a commercially available Si wafer.

[0237] Cross section observation with a transmission electron microscope showed that no new crystal defects were formed in the Si layer, and satisfactory crystallinity was maintained.

[0238] The same result as described above was obtained even when no oxide film was formed on the surface of the epitaxially grown single-crystal Si layer.

[0239] Further, the same result as described above was obtained even when oxide film was formed on the surface of the second substrate or both of the surfaces on the first and second substrates.

[0240] The porous Si layer left on the first substrate side was also selectively etched using a mixed solution of 49% hydrofluoric acid, 30% hydrogen peroxide, and water. At this time, the single-crystal Si layer functioned as an etching stopper, so the porous Si layer was selectively etched. This substrate can be used again as a substrate for forming a first substrate in anodizing or as a second substrate in bonding.

[0241] Before the substrate was reused to form a first substrate, the substrate may be annealed in hydrogen at 1,100° C. for 1 hr to restore the surface roughness (microroughness) due to micropores back to normal. However, planarization of the microroughness need not always be performed because when the substrate is to be reused to form a first substrate, surface planarization is performed simultaneously with sealing of pores on the surface of the porous Si layer during prebaking in hydrogen before epitaxial growth.

[0242] The microroughness due to micropores may be planarized not by annealing in hydrogen but by surface touch polishing.

EXAMPLE 5

[0243] Example 5 is a modification of Example 4. More specifically, the first and second anodizing conditions were changed as follows.

<First Anodizing Conditions>	
Current density:	7 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	5 (min)
Thickness of porous Si layer (target):	6 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	30 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	110 (sec)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 40%

EXAMPLE 6

[0244] Example 6 is a modification of Example 4. More specifically, the manufacturing conditions of Example 4 were changed as follows.

[0245] 1) Thickness of epitaxial Si layer: 2 μm

[0246] 2) Thickness of thermal oxide film on epitaxial Si layer: 0.1 μm

[0247] 3) Second substrate: Si substrate having a 1.9-μm thick SiO_2 layer

[0248] 4) Bonding: after the surfaces of first and second substrates were exposed to a nitrogen plasma, the substrates were brought into tight contact with each other and annealed at 400° C. for 10 hrs.

EXAMPLE 7

[0249] Example 7 is a modification of Example 4. More specifically, the manufacturing conditions of Example 4 were changed as follows.

[0250] 1) Second substrate: silica or quartz substrate

[0251] 2) Bonding: after the surfaces of first and second substrates were exposed to a nitrogen plasma or after the surfaces of first and second substrates were rinsed with water, the substrates were brought into tight contact with each other and annealed at 200° C. for 24 hrs.

[0252] 3) Annealing in hydrogen: the resultant structure was annealed in hydrogen at 970° C. for 2 hrs, and the surface roughness was evaluated with an atomic force microscope. The root mean square roughness in a 50-μm square area was approximately 0.2 nm. This nearly equals that of a commercially available Si wafer.

[0253] 4) Reuse: the first substrate side after separation was used in anodizing as a substrate for forming a first substrate.

EXAMPLE 8

[0254] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a two-layered structure was formed. The first and second anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	5 (min)
Thickness of porous Si layer (target):	6 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	30 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	110 (sec)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 40%

[0255] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a two-layered structure could be manufactured. In each of the apparatuses of the second and fourth anodizing apparatuses, two anodizing baths were used.

[0256] In the anodizing apparatus of the third embodiment, after a first porous layer was formed on each of 25 Si substrates, the electrolytic solutions and conductive diaphragm were exchanged, and a second porous layer was formed on each of the 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0257] In the anodizing apparatus of the fourth embodiment, first and second porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0258] The substrate having a porous layer was oxidized in an oxygen atmosphere at 400° C. for 1 hr. Upon this oxidation, the inner wall of each pore in the porous Si layer was covered by a thermal oxide film.

[0259] Next, a 1-μm thick single-crystal GaAs layer was epitaxially grown on the porous Si layer by MOCVD (Metal Organic Chemical Vapor Deposition). The growth conditions were as follows.

<Epitaxial Growth Conditions>	
Source gas:	$TMG/AsH_3/H_2$
Gas pressure:	80 (Torr)
Temperature:	700 (° C.)

[0260] The surface of the GaAs layer was brought into tight contact with the surface of an independently prepared Si substrate (second substrate).

[0261] A water jet with a diameter of 0.2 mm was injected to the beveling gap of the bonded substrate stack to separate the bonded substrate stack into two substrates at the second (lower) porous Si layer.

[0262] The porous Si layer left on the second substrate side was etched at 110° C. using a mixed solution (etchant) of ethylenediamine/pyrocatechol/water (at a ratio of 17 ml:3 g:8 ml). At this time, the single-crystal GaAs layer functioned as an etching stopper, so the porous Si layer was selectively etched.

[0263] The etching rate of single-crystal GaAs by the etchant is very low, and the etching amount (about several ten angstrom) of the single-crystal GaAs can be neglected for practical use.

[0264] With the above process, a substrate having a 1-μm thick single crystal GaAs layer on the single-crystal Si layer was obtained. The thickness of the single-crystal GaAs layer of this substrate was measured at 100 points on the entire surface. The film thickness uniformity was 1 μm±29.8 nm.

[0265] Cross section observation with a transmission electron microscope revealed that no new crystal defects were formed in the GaAs layer, and satisfactory crystallinity was maintained.

[0266] When an Si substrate having an oxide film was used as a support substrate, a substrate having a GaAs layer on an insulating film could be formed.

[0267] The porous Si layer left on the first substrate side was also selectively etched using a mixed solution of 49% hydrofluoric acid and 30% hydrogen peroxide under stirring. At this time, the single-crystal Si layer functioned as an etching stopper, so the porous Si layer was selectively etched. This substrate can be used again as a substrate for forming a first substrate in anodizing or as a second substrate in bonding.

[0268] Before the substrate was reused to form a first substrate, the substrate may be annealed in hydrogen at 1,100° C. for 1 hr to restore the surface roughness (microroughness) due to micropores back to normal. However, planarization of the microroughness need not always be performed because when the substrate is to be reused to form a first substrate, surface planarization is performed simultaneously with sealing of pores on the surface of the porous Si layer during prebaking in hydrogen before epitaxial growth.

[0269] The microroughness due to micropores may be planarized not by annealing in hydrogen but by surface touch polishing.

EXAMPLE 9

[0270] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a two-layered structure was formed. The first and second anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	11 (min)
Thickness of porous Si layer (target):	12 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	10 ($mA \cdot cm^{-2}$)
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:2:2
Process time:	3 (min)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 35%

[0271] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a two-layered structure could be manufactured. In each of

the apparatuses of the second and fourth anodizing apparatuses, two anodizing baths were used.

[0272] In the anodizing apparatus of the third embodiment, after a first porous layer was formed on each of 25 Si substrates, the electrolytic solutions and conductive diaphragm were exchanged, and a second porous layer was formed on each of the 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0273] In the anodizing apparatus of the fourth embodiment, first and second porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0274] The substrate having a porous layer was oxidized in an oxygen atmosphere at 400° C. for 1 hr. Upon this oxidation, the inner wall of each pore in the porous Si layer was covered by a thermal oxide film.

[0275] A 1-μm thick single-crystal InP layer was epitaxially grown on the porous Si layer by MOCVD (Metal Organic Chemical Vapor Deposition).

[0276] After the surfaces of the InP layer and an independently prepared silica or quartz substrate (second substrate) were exposed to a nitrogen plasma, these surfaces were brought into tight contact with each other and annealed at 200° C. for 10 hrs.

[0277] A water jet with a diameter of 0.2 mm was injected to the beveling gap of the bonded substrate stack to separate the bonded substrate stack into two substrates at the second (lower) porous Si layer.

[0278] The porous Si layer left on the second substrate side was selectively etched using a mixed solution of 49% hydrofluoric acid and 30% hydrogen peroxide under stirring. At this time, the single-crystal InP layer functioned as an etching stopper, so the porous Si layer was selectively etched.

[0279] The etching rate of single-crystal InP by the etchant is very low, and the etching amount (about several ten angstrom) of the single-crystal InP can be neglected for practical use.

[0280] With the above process, a substrate having a 1-μm thick single-crystal InP layer on the silica or quartz substrate was obtained. The thickness of the single-crystal InP layer of this substrate was measured at 100 points on the entire surface. The film thickness uniformity was 1 μm±29.0 nm.

[0281] Cross section observation with a transmission electron microscope indicated that no new crystal defects were formed in the InP layer, and satisfactory crystallinity was maintained.

[0282] The porous Si layer left on the first substrate side was also selectively etched using a mixed solution of 49% hydrofluoric acid and 30% hydrogen peroxide under stirring. At this time, the single-crystal Si layer functioned as an etching stopper, so the porous Si layer was selectively etched. This substrate can be used again as a substrate for forming a first substrate in anodizing.

[0283] Before the substrate was reused to form a first substrate, the substrate may be annealed in hydrogen at 1,100° C. for 1 hr to restore the surface roughness (microroughness) due to micropores back to normal. However, planarization of the microroughness need not always be performed because when the substrate is to be reused to form a first substrate, surface planarization is performed simultaneously with sealing of pores on the surface of the porous Si layer during prebaking in hydrogen before epitaxial growth.

[0284] The microroughness due to micropores may be planarized not by annealing in hydrogen but by surface touch polishing.

EXAMPLE 10

[0285] In Example 10, the bonded substrate stack separation method in Examples 4 to 9 was changed. More specifically, in Example 10, instead of using the water jet method, a thin resin wedge was inserted into the beveling gap of the bonded substrate stack to separate the bonded substrate stack into two substrates at the second (lower) porous Si layer.

EXAMPLE 11

[0286] In Example 11, the processes described in Examples 4 to 9 were performed for both surfaces of a single-crystal Si substrate for forming a first substrate.

EXAMPLE 129

[0287] A single-crystal Si substrate was set in each of the anodizing apparatuses of the above embodiments, and a porous layer having a four-layered structure was formed. The first to fourth anodizing conditions were as follows.

<First Anodizing Conditions>	
Current density:	7 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	5 (min)
Thickness of porous Si layer (target):	6 (μm)
Porosity (target):	to 24%
<Second Anodizing Conditions>	
Current density:	10 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:2:2
Process time:	3 (min)
Thickness of porous Si layer (target):	3 (μm)
Porosity (target):	to 35%
<Third Anodizing Conditions>	
Current density:	7 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	5 (min)
Thickness of porous Si layer (target):	6 (μm)
Porosity (target):	to 25%
<Fourth Anodizing Conditions>	
Current density:	20 (mA · cm^{-2})
Anodizing solution:	$HF:H_2O:C_2H_5OH$ = 1:1:1
Process time:	80 (sec)
Thickness of porous Si layer (target):	1 (μm)
Porosity (target):	to 45%

[0288] In each of the anodizing apparatuses of the first to fourth embodiments, a substrate having a porous layer with a four-layered structure could be manufactured. In each of the anodizing apparatuses of the first and third embodiments, the anodizing solution for the first, third, and fourth

anodizing processes was supplied from the first and second tanks, and the anodizing solution for the second anodizing process was supplied from the third and fourth tanks. In each of the anodizing apparatuses of the second and fourth embodiments, four anodizing baths were used.

[0289] In the anodizing apparatus of the third embodiment, a first conductive diaphragm was set, and a first porous layer was formed on each of 25 Si substrates under the first anodizing conditions. Subsequently, a second conductive diaphragm was set, and a second porous layer was formed on each of the 25 Si substrates under the second anodizing conditions. Then, a third conductive diaphragm was set, and a third porous layer was formed on each of the 25 Si substrates under the third anodizing conditions. Finally, a fourth conductive diaphragm was set, and a fourth porous layer was formed on each of the 25 Si substrates under the fourth anodizing conditions. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0290] In the anodizing apparatus of the fourth embodiment, first to fourth porous layers were sequentially formed on each of 25 Si substrates. Porous layers sequentially formed on each Si substrate used as the conductive diaphragm did not break.

[0291] [Others]

[0292] In the above examples, to epitaxially grow a non-porous layer such as a single-crystal Si layer on the porous Si layer, not only CVD but also MBE, sputtering, or liquid phase epitaxial growth can be employed.

[0293] The etchant for selectively etching the porous Si layer is not limited to the mixed solution of 49% hydrofluoric acid and 30% hydrogen peroxide. For example,

[0294] 1) a mixed solution of hydrofluoric acid and water

[0295] 2) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to a mixed solution of hydrofluoric acid and water

[0296] 3) buffered hydrofluoric acid

[0297] 4) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered hydrofluoric acid, or

[0298] 5) a mixed solution of hydrofluoric acid, nitric acid, and acetic acid can be used. The porous Si layer has a large surface area and therefore can be selectively etched using various etchants.

[0299] To separate the bonded substrate stack, various methods can be employed in addition to the separation method using a fluid as an application of the water jet method.

[0300] The remaining processes can be performed not only by the methods of the above examples but also by various methods.

[0301] As described above, by exchanging the electrolytic solution for anodizing every time one porous layer is formed, the porosity of the resultant porous layer can be precisely controlled.

[0302] In addition, when one conductive diaphragm is used under the same anodizing conditions, break of the conductive diaphragm can be suppressed.

[0303] According to the present invention, a porous layer having a multilayered structure can be formed.

[0304] The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore, to apprise the public of the scope of the present invention, the following claims are made.

What is claimed is:

1. An anodizing method of forming a porous layer on a substrate, comprising the steps of:

preparing an anodizing bath used to anodize a substrate,

anodizing said substrate to be processed in a first electrolytic solution while holding said substrate between an anode and a cathode in said anodizing bath,

exchanging the first electrolytic solution with a second electrolytic solution, and

anodizing said substrate in the second electrolytic solution, thereby forming a porous layer having a multilayered structure on said substrate.

2. The method according to claim 1, wherein a current density of a current to be flowed across said anode and said cathode is changed between anodizing using the first electrolytic solution and anodizing using the second electrolytic solution.

3. The method according to claim 1, wherein a conductive diaphragm is inserted between said anode and said substrate to be processed to prevent contamination of said substrate by said anode.

4. The method according to claim 3, wherein said conductive diaphragm is arranged to flow the whole current from said anode to said substrate to be processed through said conductive diaphragm.

5. The method according to claim 3, wherein said conductive diaphragm is arranged to cover a surface of said anode that opposes a backside surface of said substrate to be processed.

6. The method according to claim 3, wherein said conductive diaphragm is arranged to isolate an electrolytic solution in contact with a surface of said substrate to be processed, that is on said anode side, from an electrolytic solution in contact with said anode.

7. The method according to claim 4, wherein at least a surface of said conductive diaphragm that opposes said substrate to be processed is formed from a silicon material.

8. The method according to claim 4, further comprising the step of changing said conductive diaphragm every time an anodizing condition is changed.

9. The method according to claim 4, further comprising the step of preparing a conductive diaphragm corresponding to each anodizing condition, and every time the anodizing condition is changed, using a conductive diaphragm corresponding to the condition.

10. The method according to claim 1, further comprising the step of forming a porous layer having a relatively low porosity as a surface layer of said substrate to be processed, and forming a porous layer having a relatively high porosity as an underlayer of said surface layer.

11. The method according to claim 10, further comprising the step of anodizing to form a porous layer having a porosity of not more than 30% as said surface layer.

12. The method according to claim 10, further comprising the step of anodizing to form a porous layer having a porosity of not less than 30% as said underlayer of said surface layer.

13. The method according to claim 10, further comprising the step of anodizing to form a porous layer having a thickness of not more than 5 nm as said underlayer of said surface layer.

14. An anodizing method of forming a porous layer on a substrate, comprising the step of:

preparing at least two anodizing baths used to anodize a substrate, anodizing said substrate to be processed while holding said substrate between an anode and a cathode in one anodizing bath, and anodizing said substrate while holding said substrate between an anode and a cathode in the next anodizing bath, thereby forming a porous layer having a multilayered structure on said substrate.

15. The method according to claim 14, wherein different electrolytic solutions are used as electrolytic solutions used for anodizing in all or some of said at least two anodizing baths.

16. The method according to claim 14, wherein a current density of a current to be flowed across said anode and said cathode is changed in anodizing in all or some of said at least two anodizing baths.

17. The method according to claim 14, wherein a conductive diaphragm is inserted between said anode and said substrate to be processed to prevent contamination of said substrate by said anode.

18. The method according to claim 17, wherein said conductive diaphragm is arranged to flow the whole current from said anode to said substrate to be processed through said conductive diaphragm.

19. The method according to claim 17, wherein said conductive diaphragm is arranged to cover a surface of said anode that opposes a backside surface of said substrate to be processed.

20. The method according to claim 17, wherein said conductive diaphragm is arranged to isolate an electrolytic solution in contact with a surface of said substrate to be processed, that is on said anode side, from an electrolytic solution in contact with said anode.

21. The method according to claim 17, wherein at least a surface of said conductive diaphragm that opposes said substrate to be processed is formed from a silicon material.

22. The method according to claim 21, further comprising the step of changing said conductive diaphragm every time an anodizing condition is changed.

23. The method according to claim 21, further comprising the step of preparing a conductive diaphragm corresponding to each anodizing condition, and every time the anodizing condition is changed, using a conductive diaphragm corresponding to the condition.

24. The method according to claim 14, further comprising the step of forming a porous layer having a relatively low porosity as a surface layer of said substrate to be processed, and forming a porous layer having a relatively high porosity as an underlayer of said surface layer.

25. The method according to claim 24, further comprising the step of anodizing to form a porous layer having a porosity of not more than 30% as said surface layer.

26. The method according to claim 24, further comprising the step of anodizing to form a porous layer having a porosity of not less than 30% as said underlayer of said surface layer.

27. The method according to claim 24, further comprising the step of anodizing to form a porous layer having a thickness of not more than 5 μm as said underlayer of said surface layer.

28. A semiconductor substrate manufacturing method comprising the steps of:

processing a first substrate using the anodizing method of claim 1 to form a porous layer having a multilayered structure on said first substrate;

forming at least one non-porous layer on said porous layer;

bonding a second substrate to a surface of said non-porous layer of said first substrate;

separating a bonded substrate stack to a side of said first substrate and a side of said second substrate at a portion of said porous layer; and

removing said porous layer left on the side of said separated second substrate.

29. The method according to claim 28, further comprising the step of removing said porous layer left on the side of said separated first substrate to allow reuse of said first substrate.

30. The method according to claim 28, wherein the separation step comprises separating said bonded substrate stack at a portion having a high porosity in said porous layer having the multilayered structure.

31. The method according to claim 28, wherein said non-porous layer contains a single-crystal silicon layer.

32. The method according to claim 28, wherein said non-porous layer comprises a single-crystal silicon layer and a silicon oxide layer which are sequentially formed on said porous layer.

33. The method according to claim 28, wherein said non-porous layer contains a compound semiconductor layer.

34. The method according to claim 28, wherein said second substrate comprises a silicon substrate.

35. The method according to claim 28, wherein said second substrate comprises a substrate having a silicon oxide layer formed on a surface to be bonded to said first substrate.

36. The method according to claim 28, wherein said second substrate comprises a transparent substrate.

37. The method according to claim 28, further comprising, after the step of removing said porous layer, the step of planarizing a surface layer on the side of said second substrate.

38. The method according to claim 37, wherein the planarization step comprises annealing in an atmosphere containing hydrogen.

39. The method according to claim 28, wherein the step of removing said porous layer comprises selectively etching said porous layer using, as an etchant, any one of

a) hydrofluoric acid,

b) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to hydrofluoric acid,

c) buffered hydrofluoric acid, and

d) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered hydrofluoric acid.

40. The method according to claim 33, wherein the step of removing said porous layer comprises selectively etching said porous layer using an etchant whose etching rate for said porous layer is higher than that for a compound semiconductor.

41. The method according to claim 28, wherein the step of removing said porous layer comprises selectively polishing said porous layer using said non-porous layer as a stopper.

42. The method according to claims **28**, wherein the bonding step comprises the step of bringing said first substrate having said non-porous layer into tight contact with said second substrate.

43. The method according to claim 28, wherein the bonding step comprises, after the step of bringing said first substrate having said non-porous layer into tight contact with said second substrate, the step of performing a process selected from the group consisting of anode bonding, pressing, heating, and a combination thereof.

44. A semiconductor substrate capable of being manufactured by the manufacturing method of claim 28.

45. A semiconductor substrate in a process of executing the manufacturing method of claims **28**.

46. A substrate having a porous layer formed by the anodizing method of claims **1**.

47. An anodizing apparatus for executing the anodizing method of claim 1.

48. An anodizing apparatus for forming a porous layer on a substrate, comprising:

an anodizing bath having an anode and a cathode;

a plurality of tanks for storing electrolytic solutions to be supplied to said anodizing bath;

a supply mechanism for selectively supplying the electrolytic solution stored in any one of said plurality of tanks to said anodizing bath; and

a drain mechanism for draining off the electrolytic solution from said anodizing bath back into said tank which supplied the electrolytic solution.

49. The apparatus according to claim 48, wherein said apparatus further comprises a holding mechanism for holding a conductive diaphragm between said anode and a substrate to be processed, and said conductive diaphragm prevents contamination of said substrate by said anode.

50. The apparatus according to claim 49, wherein said holding mechanism holds said conductive diaphragm to flow a whole current from said anode to said substrate to be processed through said conductive diaphragm.

51. The apparatus according to claim 49, wherein said holding mechanism holds said conductive diaphragm to cover a surface of said anode that opposes a backside surface of said substrate to be processed.

52. The apparatus according to claim 49, wherein said holding mechanism holds said conductive diaphragm to isolate an electrolytic solution in contact with a surface of said substrate to be processed, that is on said anode side, from an electrolytic solution in contact with said anode.

53. The apparatus according to claim 49, wherein at least a surface of said conductive diaphragm that opposes said substrate to be processed is formed from a silicon material.

54. The apparatus according to claim 49, wherein said holding mechanism detachably holds said conductive diaphragm.

55. An anodizing apparatus for forming a porous layer on a substrate, comprising:

at least two anodizing baths each having an anode and a cathode; and

a conveyor mechanism for conveying a substrate anodized in one anodizing bath into the next anodizing bath.

56. The apparatus according to claim 55, wherein said substrate is anodized in all or some of said at least two anodizing baths under different conditions.

57. The apparatus according to claim 55, further comprising

a cleaning unit for cleaning said substrate processed in said final anodizing bath of said at least two anodizing baths, and

a drier unit for drying said substrate cleaned by said cleaning unit.

58. The apparatus according to claim 55, wherein each of said anodizing baths comprises a holding mechanism for holding a conductive diaphragm between said anode and said substrate to be processed, and said conductive diaphragm prevents contamination of said substrate by said anode.

59. The apparatus according to claim 58, wherein said holding mechanism holds said conductive diaphragm to flow a whole current from said anode to said substrate to be processed through said conductive diaphragm.

60. The apparatus according to claim 58, wherein said holding mechanism holds said conductive diaphragm to cover a surface of said anode that opposes said substrate to be processed.

61. The apparatus according to claim 58, wherein said holding mechanism holds said conductive diaphragm to isolate an electrolytic solution in contact with a surface of said substrate to be processed, that is on said anode side, from an electrolytic solution in contact with said anode.

62. The apparatus according to claim 59, wherein at least a surface of said conductive diaphragm that opposes said substrate to be processed is formed from a silicon material.

63. The apparatus according to claim 55, wherein said holding mechanism detachably holds said conductive diaphragm.

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