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(54) **Databus architecture for accelerated column access in RAM.**

(57) The present invention relates to a method of writing or reading a semiconductor random access memory (DRAM or SRAM) having plural sense amplifiers connected to bit lines and having data bus read and write amplifiers, comprised of providing a pair of data buses for access by each sense amplifier and each read and write amplifier, reading or writing one data bus while precharging the other data bus during a first read or write cycle, and reading or writing the other data bus while precharging the first data bus in a second read or write cycle following the first read or write cycle.

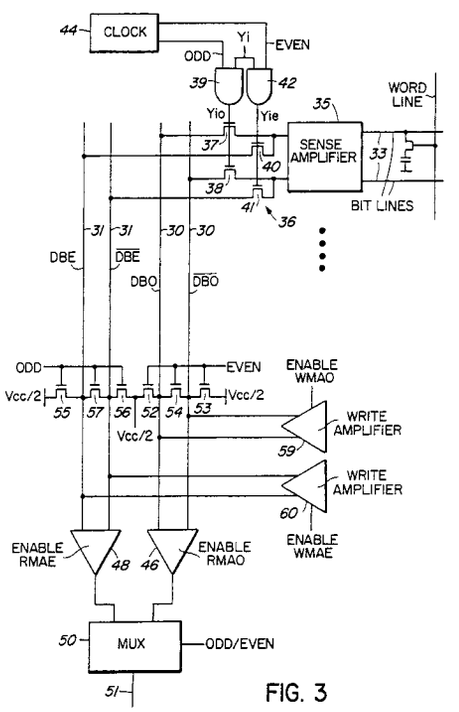


FIG. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 94 30 9205

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 13 no. 375 (P-921) ,21 August 1989 & JP-A-01 128292 (MATSUMOTO)	1-6	G11C7/00
A	* abstract *	7,9	
P,X	US-A-5 371 716 (MUTSUMI) * the whole document *	1-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 September 1995	Degraeve, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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