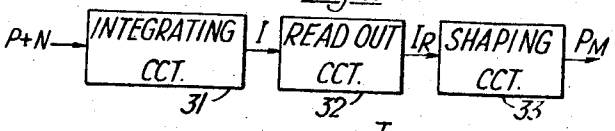
May 27, 1969 SUKEHIRO ITO ET AL 3,447,086

RECTANGULAR-CODE REGENERATOR

Filed July 22, 1964 Sheet 1 of 5

Fig. 1.



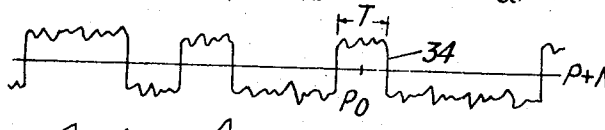


Fig. 2.

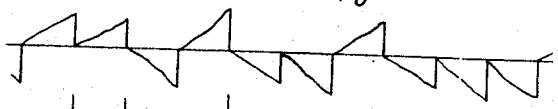


Fig. 3.

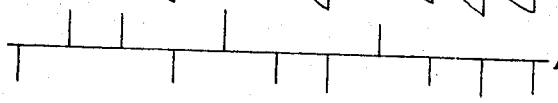


Fig. 4.

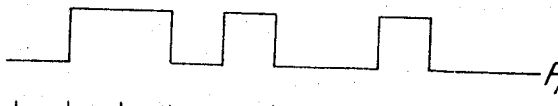


Fig. 5.

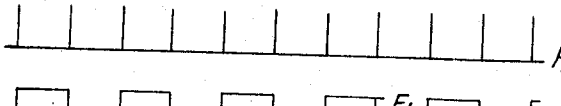


Fig. 7.

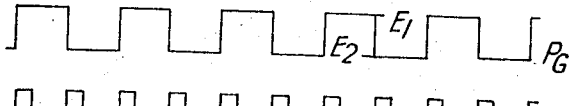


Fig. 8.

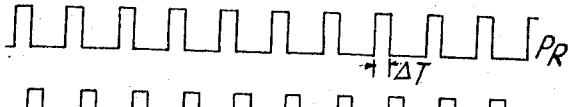


Fig. 9.

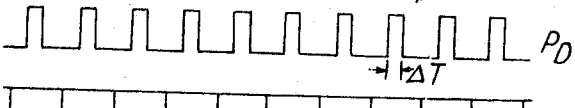


Fig. 10.

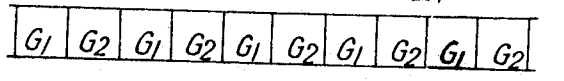


Fig. 11.

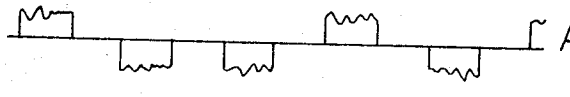
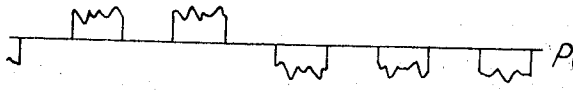


Fig. 12.



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May 27, 1969 SUKEHIRO ITO ET AL 3,447,086

RECTANGULAR-CODE REGENERATOR

Filed July 22, 1964 Sheet 2 of 5

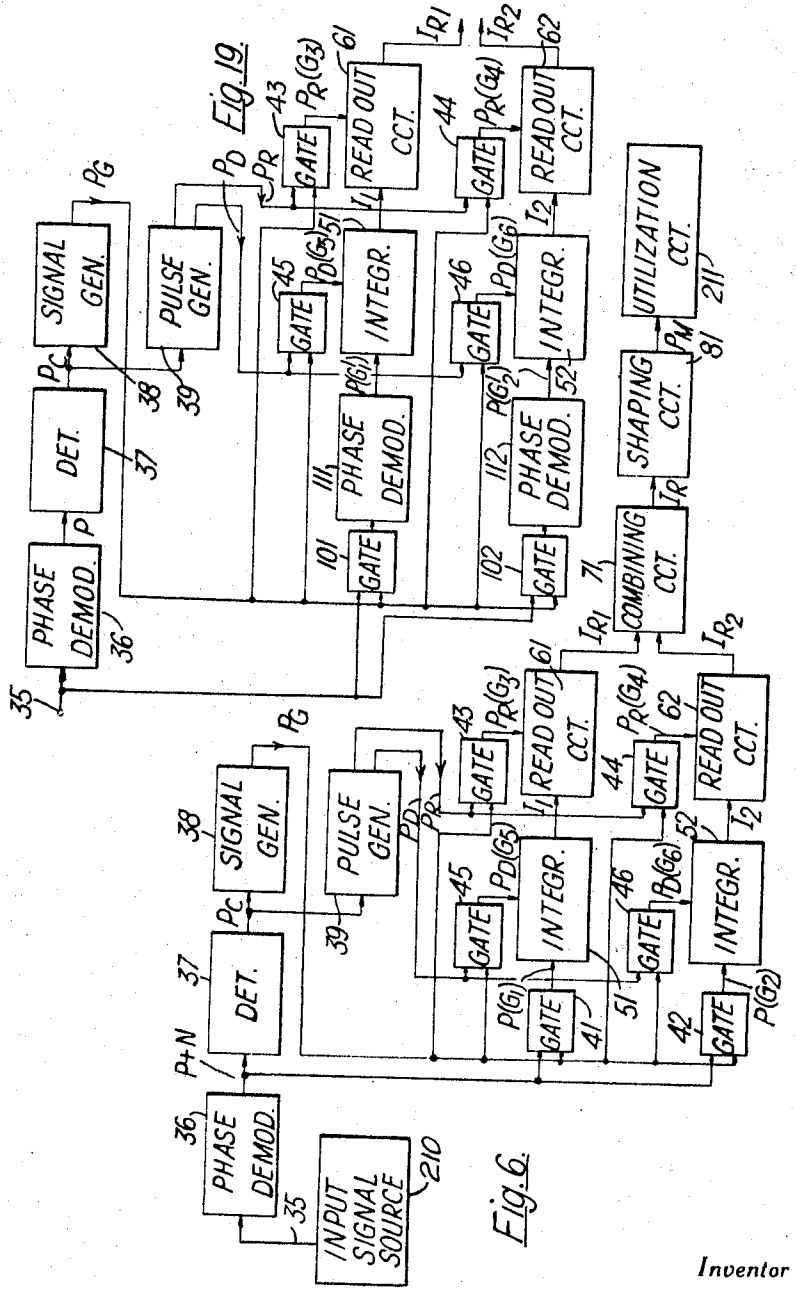


Fig. 6.

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G_4	G_3	G_4	G_3	G_4	G_3	G_4	G_3	G_4	G_3
G_6	G_5	G_6	G_5	G_6	G_5	G_6	G_5	G_6	G_5

Fig. 13.

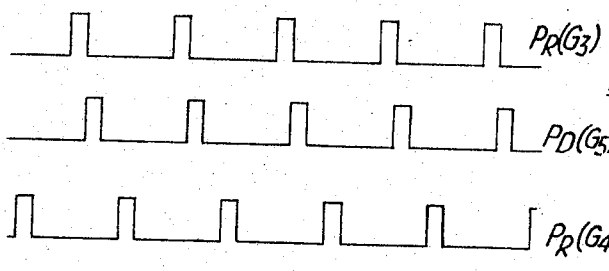


Fig. 14.

Fig. 15.

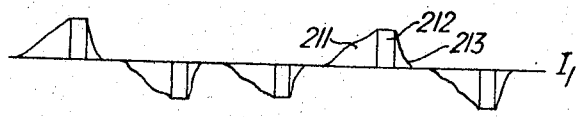
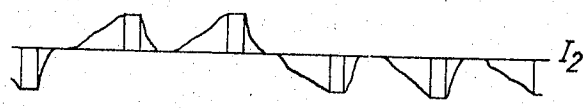


Fig. 16.



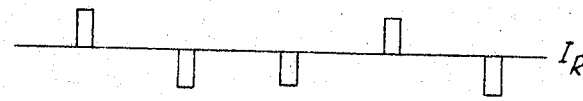
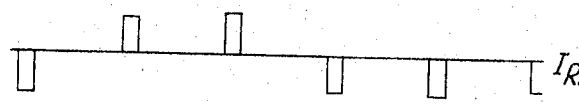


Fig. 17.



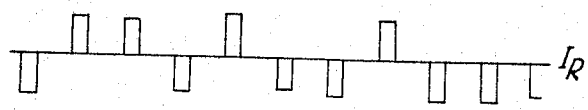


Fig. 18.

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May 27, 1969 SUKEHIRO ITO ET AL 3,447,086

RECTANGULAR-CODE REGENERATOR

Filed July 22, 1964

Sheet 4 of 5

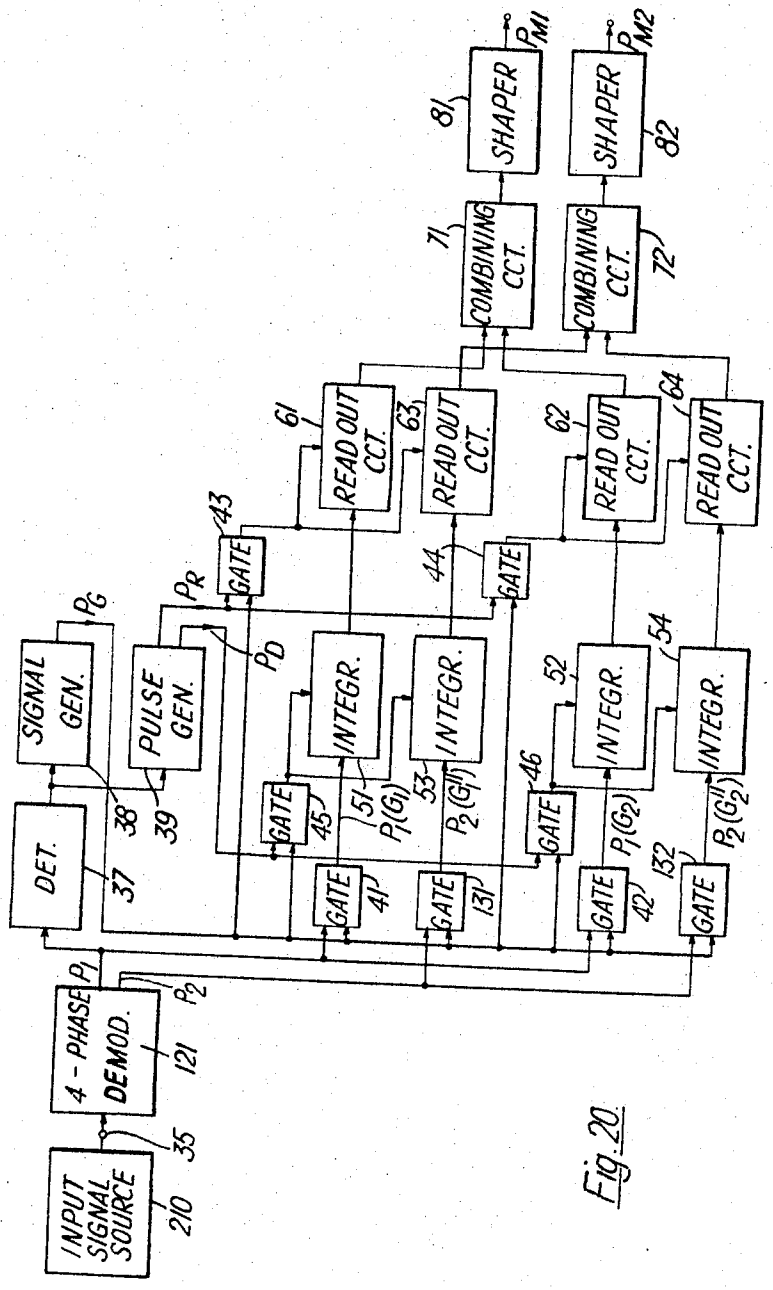


Fig. 20

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May 27, 1969 SUKEHIRO ITO ET AL. 3,447,086

RECTANGULAR-CODE REGENERATOR

Filed July 22, 1964 Sheet 5 of 5

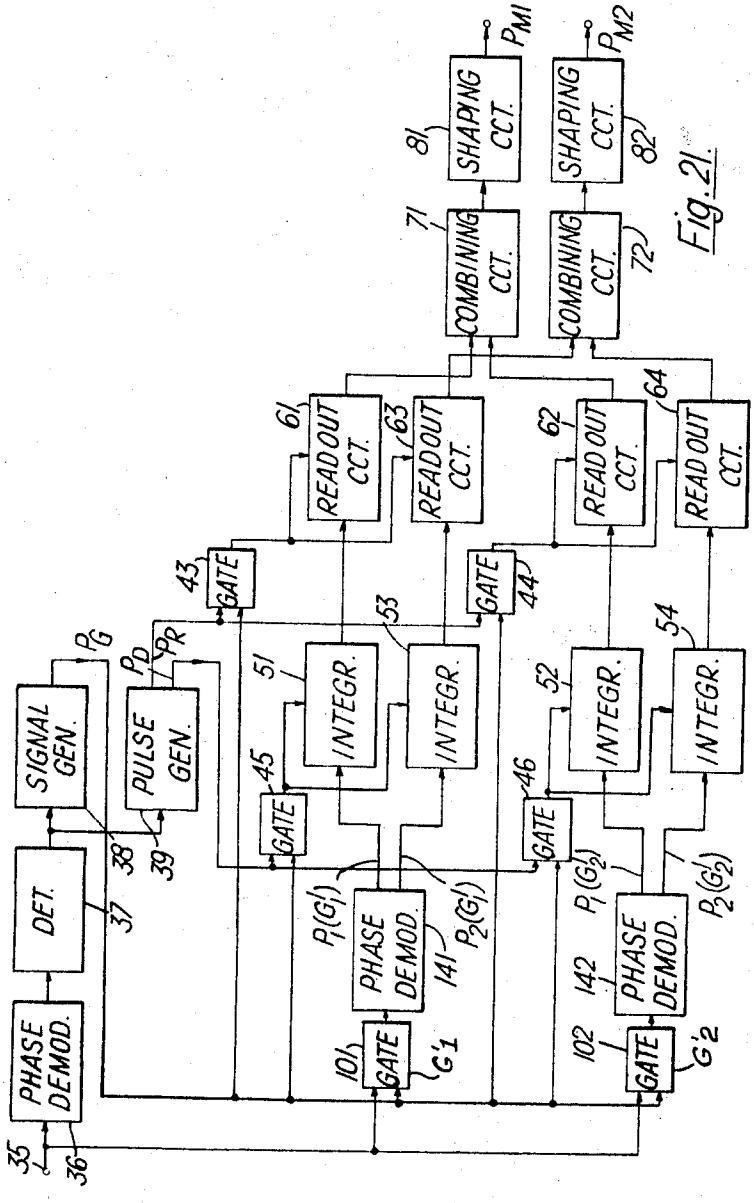


Fig. 21.

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United States Patent Office 3,447,086
Patented May 27, 1969

3,447,086

RECTANGULAR-CODE REGENERATOR

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Filed July 22, 1964, Ser. No. 384,493
Claims priority, application Japan, July 29, 1963, 38/39,987
Int. Cl. H04b 1/10; H04l 15/24
U.S. Cl. 325—323
12 Claims

ABSTRACT OF THE DISCLOSURE

A rectangular code pulse regenerator for translating an input signal two-phase modulated with a modulating train of two-phase rectangular binary-code pulses or an input signal four-phase modulated with two modulating trains of different two-phase rectangular binary-code pulses into an output signal comprising a replica first and third binary-code pulse train or into an output signal comprising a replica first and third phase rectangular binary-code pulse train and a replica second and fourth phase rectangular binary-code pulse train.

This invention relates to a code regenerator for demodulating and regenerating a received wave which has been modulated by one or more rectangular code trains.

The rectangular-code regenerator of this invention includes: a clock frequency detector responsive to a modulated wave modulated by at least a train of rectangular codes for producing a clock pulse series having a recurrence period equal to the duration of an elementary code constituting the rectangular code train; demodulating and separating means responsive to said clock pulse series and the modulated wave for producing (with reference to the time position of the elementary codes constituting the rectangular code train contained in the modulated wave) a predetermined number of partial demodulated code trains which are demodulated and separated from one another. The separation is performed in such a manner that only one of the elementary codes may be present (in accordance with the sequence of successive time intervals determined by the clock pulse series) within each of the time periods, each consisting of the predetermined number of the time intervals. Integrating circuits are also provided and each is responsive to one of the partial demodulated code trains and the clock pulse series for integrating (within the preceding one of any successive two of the time periods) the value of the one of said partial demodulated code trains. This integration produces an integrated value which is discharged in the succeeding time period (and before the integration substantially takes place within the succeeding one of the successive two time periods) to produce an integrated value train having one integrated value, for each of the time periods. Reading-out circuits are also provided, each of which is responsive to one of the integrated value trains and the clock pulse series for reading out the integrated values (before the discharging of the integrated value to be read out substantially takes place) to produce a partial read-out value train consisting of read-out values each representing the read-out integrated value. A combining circuit is also provided, which is responsive to a plurality of the partial read-out value trains for producing a read-out value train corresponding to the rectangular code train. A shaping circuit responsive to the read-out signal train produces the replica of said rectangular code train. The modulated wave may be either amplitude-modulated, frequency-modulated, or phase-modulated signals.

In a multichannel telephone communication system

(wherein information is quantized, converted into digital signals, and transmitted on a carrier wave which is modulated by digital signals and, in which on the receiver side, the digital signals are detected in the modulated wave and returned to the initial information or in a telegraph communication system wherein the carrier wave is modulated by the information which by itself is in the form of digital signals) it is desirable to reduce as far as possible, disturbances to the detected digital signals caused by noise which increases to relatively large values with decreases of the carrier wave input level. In order to extract the signal from a combination of signal and noise (with the disturbance of the noise reduced to a minimum) it suffices to make the weighting function of the filter used be equal to the waveform of the signal. In other words, the use of a matched filter is required whose transfer function is given by the complementary imaginary number of the spectrum of the signal. If the signal to be recovered is a rectangular binary-code train, the matched filter for the rectangular binary-code train may be obtained (as is already known in principle) by arranging the filter so that each of the elementary codes constituting the rectangular binary-code train can be integrated within the whole duration T of the sampled elementary code without any influence on the remaining elementary codes. Moreover, the results of integration should be read out to determine the state or condition of the concerned elementary code. Furthermore, these processes should be successively repeated for each elementary code. In order to realize such an ideal matched filter for a rectangular binary-code train, it is necessary to reduce (so as to be completely negligibly short as compared with the duration T of the elementary code) the sum of the time required for reading out the result of integration of one of the elementary codes and the time needed for discharging the result of integration, down to a predetermined level, thereby to prepare for the integration of the succeeding elementary code. The time demanded for reading-out and discharging, however, is dependent on the speed and ability of the circuit elements and for example may not be shorter than 0.1 microsecond. Consequently, with this assumption the duration T of an elementary code (which must be sufficiently longer than and for example may be ten times, as long as this 0.1 microsecond) can not be shorter than 1 microsecond. This means that the transmission speed can never be raised above one megabit per second. It becomes difficult therefore to detect by means of a matched filter, high-speed codes, such as pulse code modulated multichannel telephone signals. In this connection, the conventional method of reception which is widely adopted, is to allow the code train containing the noise to pass through a low-pass filter, to read out successively the values of the elementary codes at the proximity of their respective centers, and to recover the code train by shaping. With this method, the low-pass filter serves to reduce the noise. It is, however, impossible to make such a low-pass filter a matched filter. Furthermore, the low-pass filter causes interference among the codes. Therefore, this means that the disturbance caused by the noise is far greater with a low-pass filter than with an ideal matched filter.

An object of this invention is to provide a high speed code regenerator having an ideal matched filter circuit.

Another object of this invention is to provide a code regenerator having an ideal matched filter circuit in which the read out discharge time may be regarded as being substantially zero.

Still another object of this invention is to provide a code regenerator which is capable of substantially unrestricted transmission speeds.

Another object of the invention is therefore to provide

an ideal matched filter circuit which produces low noise among the codes and wherein the read-out and discharge time may be regarded to be substantially zero.

The above-mentioned and other features and objects of this invention and means for attaining them will become more apparent and the invention itself will be best understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of a matched filter according to this invention;

FIGS. 2–5 are waveforms for explaining the operation of the filter of FIG. 1, and plots of time on the abscissa axis vs. amplitude on the ordinate axis;

FIG. 6 is a block diagram of an embodiment of an invention which is adapted for two-phase phase modulation;

FIGS. 7–18 are waveforms for explaining the operation of the embodiment of FIG. 6 and are plots of time on the abscissa axis vs. amplitude on the ordinate axis;

FIG. 19 is a block diagram of another embodiment of the invention;

FIG. 20 is a block diagram of still another embodiment of the invention which is adapted to four-phase phase modulation; and

FIG. 21 is a block diagram of still another embodiment of the invention.

Referring to FIG. 1, a matched filter is shown which includes a terminal for receiving the signal P and noise N; an integrating circuit **31**, an integrated value reading-out circuit **32**, and a shaping circuit **33**. As shown in FIG. 2, a received and demodulated rectangular binary-code train P containing the noise N is composed of a number of elementary codes, each of which has a duration T (as shown above elementary code **34**). The integrating circuit **31** integrates the voltage value of each of the elementary codes for the time during which the elementary code is present. FIG. 3 shows a series I of the thus obtained integrated values. The read-out circuit **32** derives from the integrated value a series of read-out value 1_R shown in FIG. 4. As shown in FIG. 4, a pulse may be derived whenever a zero point occurs in FIG. 3. The shaping circuit **33** transforms the read-out values into the shaped rectangular binary-code train P_M shown in FIG. 5.

To explain the function by which the circuit shown in FIG. 1 serves as a matched filter for a rectangular binary-code train, let it be assumed that an arbitrary elementary code P_0 illustrated by **34** of FIG. 2 alone is to be detected among the elementary codes of a rectangular binary-code train P shown in FIG. 2 and that the duration of the elementary code P_0 is from a time $t_{-0}-T/2$ to another time $t_{-0}+T/2$. Then, the elementary code P_0 is integrated at the integrating circuit **31** for the duration from $t_{-0}-T/2$ to $t_{-0}+T/2$ and thus an integrated value I_0 is obtained which is given by

$$I_0=\int_{t_{-0}-T/2}^{t_{-0}+T/2} P_0 dt \tag{1}$$

If the spectrum of the elementary code P_0 is $S_0(jp)$, the elementary code P_0 is given by the Fourier integral or by

$$P_0=(1/2\pi)\cdot\int_{-\infty}^{\infty} S_0(jp)\ \exp.\ (jpt)dp \tag{2}$$

where p is the angular frequency and j represents the imaginary unit. By substituting Equation 2 into Equation 1, we obtain:

$$I_0=(1/2\pi)\int_{t_{-0}-T/2}^{t_{-0}+T/2}\int_{-\infty}^{\infty} S_0(jp)\ \exp.\ (jpt)\cdot dpdt \tag{3}$$

$$I_0=(1/2\pi)\int_{-\infty}^{\infty} S_0(jp)T\cdot\frac{\sin\ pT/2}{pT/2}\ \exp.\ (jpt_0)dp \tag{4}$$

Equation 4 shows that the value I_0 derived through integration of the elementary code P_0 from the time

$t_{-0}-T/2$ to the time $t_{-0}+T/2$ is equal to the value which would be obtained by causing the elementary code P_0 to pass through a filter whose transfer function is

$$T\ \frac{\sin\ pT/2}{pT/2} \tag{5}$$

and then reading out the same at the center time point t_{-0} of the elementary code P_0. On the other hand, it is already known that the frequency characteristic of a generally rectangular pulse is given by the same formula as Equation 5. Therefore the spectrum $S_0(ip)$ of the elementary code P_0 (which is a rectangular pulse) is of the same frequency characteristic as the transfer function given by the Expression 5. As a result, the circuit of FIG. 1 serves as a matched filter for the rectangular binary-code train.

Now that the theoretical aspects have been clarified concerning the realization of a matched filter for a rectangular binary-code train, the invention for embodying such an ideal matched filter will be explained with further reference to the drawings.

Referring to FIG. 6 a block diagram is indicated of an embodiment of this invention for two-phase, phase demodulation. The modulated wave has been two-phase phase modulated by a rectangular binary-code train to derive the replica of the original rectangular binary code train. The modulated wave which has been two-phase phase modulated by a rectangular binary-code train is supplied from an input terminal **35** connected to input signal source **210**. The input signal is supplied to a two-phase phase demodulator **36** to be demodulated into a demodulated rectangular binary-code train P having superimposed noise N. P and N together have the wave shape shown in FIG. 2. A portion of the demodulated rectangular binary-code train P is supplied to a frequency detector **37** which detects the frequency B which is equal to the reciprocal of the duration T of an elementary code and produces clock pulse output signals P_C having the clock frequency B of the rectangular binary code train. The clock pulse series P_C drives both the gate control signal generator **38** (which may be a flip-flop circuit) and a pulse generator **39**. The output P_G of the gate control signal generator **38** is a rectangular wave which alternatingly assumes, as shown in FIG. 8, two different voltages E_1 and E_2 during each interval T of an elementary code of the demodulated rectangular binary-code train P. The output P_G serves to control transmission gates G_1 (**41**) and G_2 (**42**) for governing transmission of the demodulated rectangular binary-code train P and other gates G_3 (**43**), G_4 (**44**), G_5 (**45**) and G_6 (**46**) for conditioning two signal paths which will be explained hereinafter. The two outputs obtained at the respective output terminals of the pulse generator **39** are two pulse trains consisting of pulses whose duration ΔT is shorter than half of the duration T of an elementary code. One of the outputs from generator **39**, P_R, is phase-synchronized, as shown in FIG. 9, with the demodulated rectangular binary-code train P. The train P_R is a read-out pulse series which is connected through read-out pulse gates **43** and **44** to control read-out circuits **61** and **62** which read out integrated values obtained at integrating circuits **51** and **52**, respectively. The other output P_D of generator **39**, as shown in FIG. 10, lags behind the read-out pulse series P_R by the duration ΔT. The series P_D acts as a discharging pulse series which controls through the discharging pulse gates **45** and **46** the discharge of the above-mentioned integrated values.

Now description will be made of the manner in which the demodulated rectangular binary-code train P, obtained at the two-phase phase demodulator **36**, is successively modified by various pulse signals at the gates, integrating circuits, and reading-out circuits. Gates G_1 (**41**) and G_2 (**42**) alternatingly intermittently allows the demodulated rectangular binary-code train P to pass therethrough. More particularly when the gate control signal P_G assumes the voltage E_1, the gate G_1 (**41**) is open and the gate G_2 (**42**)

is closed. When the gate control signal P_G assumes the value E_2, gate G_1 is closed and gate G_2 is open. FIG. 11 shows with reference to the gate control signal P_G illustrated in FIG. 8 the gate number of that gate which is opened. It follows, therefore, that every other one of these elementary codes of the demodulated rectangular binary-code train P supplied to both of the gates G_1 and G_2 are alternately extracted as shown in FIG. 12. Thus, demodulated rectangular binary-code train P is divided into two partial demodulated rectangular binary-code trains, each of whose duty factor is 50%. In other words, first and second parallel rectangular binary-code train $P(G_1)$ and $P(G_2)$ of FIG. 12 are thus generated.

In order to explain the operation of the gates G_3 (43) and G_4 (44) which select the reading-out pulse series P_R and the gates G_5 (45) and G_6 (46) which select the discharging pulse series P_D reference will be made now to FIG. 13. The gates G_3 (43) and G_5 (45) are closed and the gates G_4 (44) and G_6 (46) are opened when the gate control signal P_G assumes the voltage E_1. When the gate control signal P_G assumes the value of E_2, the gates G_3 (43) and G_5 (45) are open and the gates G_4 (44) and G_6 (46) are closed. FIG. 13 indicates sequentially the number of gates which are open. When FIG. 13 is considered in conjunction with FIG. 9, illustrating the read-out pulse series P_R and FIG. 10 illustrating the discharging pulse series P_D, it is evident that a first read-out pulse series $P_R(G_3)$ and a first discharging pulse series $P_D(G_5)$ shown in FIG. 14 are supplied respectively through the gates G_3 (43) and G_5 (45) to the read-out circuit **61** and to the integrating circuit **51**. Likewise, a second reading-out pulse series $P_R(G_4)$ and a second discharging pulse series $P_D(G_6)$ illustrated in FIG. 15 are applied through the gate G_4 (44) to the reading-out circuit **62** and through the gate G_6 (46) to the integrating circuit **52**, respectively.

Proceeding with the explanation of FIG. 6, the effect caused on the first parallel rectangular binary-code train $P(G_1)$ (of the two parallel rectangular binary-code trains shown in FIG. 12) will now be examined. When the gate control signal P_G assumes the voltage E_1 and the gate G_1 (41) is consequently open, then the integrating circuit **51** integrates the code train $P(G_1)$ to derive first integrated values I_1 which are shown in FIG. 16 by the substantially triangular portions on the left-hand sides of the waveforms. One such portion is indicated by the reference numeral **211**. During these time periods, the gates G_3 (43) and G_5 (45) are closed. When the gate control signal assumes the value E_2 the gate G_1 (41) is closed and the function of the integrating circuit **51** ceases. As a result, the first integrated value I_1 become constant in the manner illustrated in FIG. 16 by the intermediate slant rectangular portions. One such intermediate portion is indicated at **212**. When gate G_3 (43) opens, the first read-out pulse series $P_R(G_3)$ shown in FIG. 14 drives the read-out circuit **61** to read out the first integrated values I_1. As soon as this read-out ends, the first discharging pulse $P_D(G_5)$ of the duration ΔT also shown in FIG. 14, passes through the previously opened gate G_5 (45) to discharge the first integrated values I_1 in the manner shown in FIG. 16 by the right-hand side small triangles (for example **213**) to reset the integrating circuit **51** to the original state from which the integration started. By cycling of the integration, reading-out, and discharging operation, the first parallel read-out values I_{R1} illustrated in FIG. 17 are supplied to a combining circuit **71** one after another. The operation of integrator **52** and read-out circuit **62** in conjunction with the other rectangular binary pulse train $P(G_2)$ is similar to that of integrator **51** and read-out circuit **61**.

The second parallel rectangular binary-code train $P(G_2)$ is supplied to integrator **52**. The opening and closing of the six gates G_1–G_6 by the gate control signal P_G is performed in the manner shown in FIGS. 11 and 13. The shapes and phases of the second read-out pulse series $P_R(G_4)$ supplied through the gate G_4 (44) to the read-out circuit **62** and the second discharging pulse series $P_D(G_6)$ supplied through the gate G_6 (46) to the integrating circuit **52** (the pulse series are shown in FIG. 15) are the same as explained in conjunction with the first parallel rectangular binary-code train $P(G_1)$. Therefore, the second integrated values I_2 are second binary rectangular pulse trains shown in FIG. 16. The second parallel read-out values I_{R2} are illustrated in FIG. 17.

The first and the second read-out values I_{R1} and I_{R2} are both supplied to the combining circuit **71** where they are combined to become the read-out value train I_R, shown in FIG. 18 which is restored at a shaping circuit **81** to a shaped rectangular binary-code train P_M whose form is similar to the original rectangular binary-code train shown in FIG. 5. The output of said shaping circuit is supplied to utilization circuit **211**.

As will be understood from the foregoing, the rectangular code regenerator for the embodiment divides the input signal into two parallel rectangular binary-code trains alternatingly on a time basis of an elementary code. Reading-out and discharging of an integrated value are performed in that blank time interval during the duration of an elementary code which follows the integration of an elementary code in each of the binary-code trains. This arrangement provides a resulting characteristic which is substantially the same as the aforementioned ideal matched filter having a zero read-out and discharge time interval.

Referring now to FIG. 19, there is illustrated therein another embodiment of a rectangular binary-code regenerator according to this invention and which is also used in conjunction with a two-phase phase demodulator. This embodiment is nearly the same as that of the embodiment shown in FIG. 6, except that gates G_1' (**101**) and G_2' (**102**) of FIG. 19 (which correspond to the gates G_1 (41) and G_2 (42) shown in FIG. 6) do not transmit the demodulated rectangular binary-code train therethrough but rather transmits the modulated wave itself. The modulated wave is not formed in two partial or parallel rectangular binary-code trains until the partial modulated waves are demodulated at phase demodulators **111** and **112**. The feature of this embodiment resides in the fact that the construction and adjustment of the gates G_1' (**101**) and G_2' (**102**) are very simple as compared with those of the gates G_1 (41) and G_2 (42) shown in FIG. 6 because it is unnecessary for the former to transmit direct-current components. In other respects the operation of FIG. 19 is similar to that of the embodiment of FIG. 6.

In the description of the embodiment of FIGS. 6 and 19, it has been the underlying assumption that the time required for reading-out and discharging is shorter than the duration T of an elementary code. If the transmission speed is so great that the time for reading-out and discharging is longer than the duration T of an elementary code at that time, it is only necessary to divide the demodulated rectangular binary-code train into three or more parallel rectangular binary-code trains. If division into three is desired, it is possible to achieve the same operation as has been described, by replacing the gate control signal generator **38** shown in FIG. 6 for producing two voltages E_1 and E_2, with a gate control signal generator (not shown) for producing three voltages E_1, E_2, and E_3 and by arranging besides the series comprising the gate G_1 (41), integrating circuit **51**, and reading-out circuit **61**, two additional and similar series.

In the foregoing explanation, the input signal has been a two-phase phase-modulated wave. A similar rectangular binary-code regenerator may be obtained even if the input wave is four-phase phase-modulated.

Referring to FIG. 20, there is illustrated therein a four-phase phase-modulator **121** which is connected to the input signal source **210** and provides at one of its two output terminals a first demodulated rectangular binary-code train P_1 which includes the first and third phases of the four phases and which are separated by 180° from each other. At the other output terminal of demodulator **121**, a second demodulated rectangular binary-code train P_2

is provided which consists of the second and the fourth phases and which are spaced by 90° from the first and the third phases, respectively (and are separated by 180° from each other). Similar to the embodiment of FIG. 6, the first demodulated rectangular binary-code train P_1 is divided at gates G_1 (**41**) and G_2 (**42**) into two parallel rectangular binary-code trains $P_1(G_1)$ and $P_2(G_2)$, which are supplied through the respective integrating circuits **51** and **52** and read-out circuits **61** and **62** to a single combining circuit **71**. The output of combining circuit **71** is supplied to the shaping circuit **81** to be regenerated there into a first shaped rectangular binary-code train P_{M1} consisting of the first and the third phases. The second demodulated rectangular binary-code train P_2 is also divided (at gates G_1'' (**131**) and G_2'' (**132**)) into two parallel rectangular binary-code trains $P_2(G_1'')$ and $P_2(G_2'')$, which are supplied through respective integrating circuits **53** and **54** and reading-out circuits **63** and **64** to a single combining circuit **72**. The output of combining circuit **72** is supplied to a shaping circuit **82** to be regenerated there into a second shaped rectangular binary-code train P_{M2} consisting of the second and the fourth phases. It is to be noted that although the frequency detector **37** of FIG. 20 is supplied the first demodulated rectangular binary-code train P_1, it may be supplied with the second demodulated rectangular binary-code train P_2.

FIG. 21 illustrates another embodiment of this invention. This embodiment is similar to the embodiment of FIG. 19 except that it is adapted for the case of four-phase phase-demodulation. In FIG. 21, a partial four-phase phase-demodulated wave having a duty factor of 50% is derived at gate G_1' (**101**) and is then divided at a four-phase phase-demodulator **141** into a first partial rectangular binary-code train $P_1(G_1')$ (consisting of the first and the third phases) and a second rectangular binary-code train $P_2(G_1')$ (consisting of the second and the fourth phases). Another partial four-phase phase-modulated wave having a duty factor of 50% is derived at the gate G_2' (**102**) and is divided at another four-phase demodulator **142** into another first partial rectangular binary-code train $P_1(G_2')$ (consisting of the first and the third phases) and another second rectangular binary-code train $P_2(G_2')$ (consisting of the second and the fourth phases). Similar to the embodiment of FIG. 20, first and second shaped rectangular binary-code trains P_{M1} and P_{M2} are regenerated from the four parallel rectangular binary-code trains through the respective integrating circuits **51–54**, read-out circuits **61–64**, combining circuits **71** and **72**, and shaping circuits **81** and **82**. Incidentally, it is possible in this embodiment and in the embodiment illustrated in FIG. 20, to use the clock frequency detector **37**, gate control signal generator **38**, pulse generator **39**, and gates G_3, G_4, G_5 and G_6 as common elements for both the first and the second demodulated rectangular-code trains P_1 and P_2.

While we have described above the principles of our invention in connection with specific embodiments, it is to be clearly understood that this description is made only by way of example, and not as a limitation to the scope of our invention as set forth in the objects thereof and in the accompanying claims.

What is claimed is:

1. A rectangular code pulse regenerator, comprising:

a source of an input signal modulated with a modulating train of multi-phase rectangular binary-code pulses;

means for demodulating said multi-phase modulated input signal to produce a modulated rectangular binary-code pulse train;

means for translating a first portion of said demodulated pulse train into a plurality of control rectangular pulse trains; a first of said plurality of control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second alternate square-wave voltage pulses occurring during the time interval of an elementary code of said demodulated binary-code pulse train; and a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said demodulated binary-code pulse train, each of said second control pulses having a time duration shorter than one-half the time duration of said elementary code;

first and second gating means activated by said square-wave pulse trains and a second portion of said demodulated binary-code pulse train in such manner that said first gating means is opened in response to said first alternate square-wave pulse train to transmit first alternate elementary codes of said demodulated binary-code pulse train therethrough to provide a first partial demodulated rectangular binary-code pulse train while said second gating means is closed and further in such manner that said second gating means is opened in response to said second alternate square-wave pulse train to transmit second alternate elementary codes of said demodulated binary-code pulse train therethrough to provide a second partial demodulated rectangular binary-code pulse train while said first gating means is closed;

first means for integrating said first partial demodulated binary-code pulse train to provide a first train of integrated pulses;

second means for integrating said second partial demodulated binary-code pulse train to provide a second train of integrated pulses;

third and fourth gating means activated by said square-wave and second control rectangular pulse trains in such manner that said third gating means is closed during said first alternate square-wave voltage pulse train and is opened in response to said second alternate square-wave voltage and second control pulse trains for reading out said first integrated pulse train to provide a first train of read-out pulses and further in such manner that said fourth gating means is closed during said second alternate square-wave voltage pulse train and is opened in response to said first alternate square-wave voltage and second control pulse trains for reading out said second integrated pulse train to provide a second train of read-out pulses;

means for converting said first and second read-out pulse trains into a multi-phase rectangular binary-code pulse train as a replica of said train of multi-phase rectangular binary-code pulses modulating said input signal;

and means for utilizing said replica multi-phase rectangular binary-code pulse train.

2. The regenerator according to claim **1** in which said plurality of control rectangular pulse trains includes a third rectangular pulse train lagging said second rectangular pulse train by a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses;

and said regenerator also including fifth and sixth gating means responsive to said square-wave and third control pulse trains in such manner that said fifth gating means is closed during said first alternate square-wave pulse train and is opened in response to said second alternate square-wave and third control pulse trains to discharge said first integrated pulse train in said first integrating means and further in such manner that said sixth gating means is closed during said second alternate square-wave voltage pulse train and is opened in response to said first alternate square-wave and third control pulse trains to discharge said second integrated pulse train in said second integrating means.

3. A rectangular code pulse regenerator, comprising:

a source of an input signal modulated with a modulating train of multi-phase rectangular binary-code pulses;

means for demodulating said modulated input signal to produce a demodulated rectangular binary-code pulse train;

means for translating a first portion of said demodulated pulse train into a plurality of control rectangular pulse trains; a first of said plurality of control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses and second alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second alternate square-wave voltage pulses occurring during the time interval of an elementary code of said demodulated binary-code pulse train; a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said demodulated binary-code pulse train, each of said second control pulses having a time duration shorter than one-half the time duration of said elementary code pulse; and a third of said plurality of control pulse trains comprising a rectangular pulse train lagging said second control pulse train by a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses;

first and second gating means activated by said square-wave pulse trains and a second portion of said demodulated binary-code pulse train in such manner that said first gating means is opened in response to said first alternate square-wave pulse train to transmit first alternate elementary codes of said demodulated binary-code pulse train therethrough to provide a first partial demodulated rectangular binary-code pulse train while said second gating means is closed and further in such manner that said second gating means is opened in response to said second alternate square-wave pulse train to transmit second alternate elementary codes of said demodulated binary-code pulse train therethrough to provide a second partial demodulated rectangular binary-code pulse train while said first gating means is closed;

first means for integrating said first partial demodulated binary-code pulse train to provide a first train of integrated pulses;

second means for integrating said second partial demodulated binary-code pulse train to provide a second train of integrated pulses;

third and fourth gating means responsive to said square-wave pulse trains and second and third control pulse trains in such manner that said third and fourth gating means are closed during said first alternate square-wave voltage pulse train while said first integrating means is integrating said first partial demodulated binary-code pulse train and further in such manner that said third gating means is opened in response to said second alternate square-wave and second control pulse trains to read-out said first integrated pulse train to provide a first train of read-out pulses and said fourth gating means is opened in response to said second alternate square-wave and third control pulse trains to discharge said first integrated pulse train in said first integrating means;

fifth and sixth gating means responsive to said square-wave pulse trains and second and third control pulse trains in such manner that said fifth and sixth gating means are closed during said second alternate square-wave voltage train while said second integrating means is integrating said second partial demodulated binary-code pulse train and further in such manner that said fifth gating means is opened in response to said first alternate square-wave voltage and second control pulse trains to read-out said second integrated pulse train to provide a second train of read-out pulses and said sixth gating means is opened in response to said first alternate square-wave and third control pulse trains to discharge said second integrated pulse train in said second integrating means;

means for converting said first and second read-out pulse trains into a multi-phase rectangular binary-code pulse train as a replica of said multi-phase rectangular binary-code pulse train modulating said input signal;

and means for utilizing said replica multi-phase rectangular binary-code pulse train.

4. A rectangular code pulse regenerator, comprising:

a source of an input signal modulated with a modulating train of two-phase rectangular binary-code pulses;

first means for demodulating a first portion of said modulated input signal to produce a demodulated rectangular binary-code pulse train;

means for translating said demodulated binary-code pulse train into a plurality of control rectangular pulse trains; a first of said plurality of control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses and second alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second alternate square-wave voltage pulses occurring during the time interval of an elementary code of said demodulated binary-code pulse train; and a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said demodulated binary-code pulse train, each of said second control pulses having a time duration shorter than one-half the time duration of said elementary code;

first and second gating means activated by said square-wave pulse trains and a second portion of said modulated input signal in such manner that said first gating means is opened in response to said first alternate square-wave pulse train to transmit a train of first alternate elementary codes of said modulated input signal while said second gating means is closed and further in such manner that said second gating means is opened in response to said second alternate square-wave pulse train to transmit a train of second alternate elementary codes of said modulated input signal therethrough to provide a second partial modulated rectangular binary-code pulse train of said modulated input signal while said first gating means is closed;

second means for demodulating said first partial modulated binary-code pulse train to provide a first partial demodulated rectangular binary-code pulse train;

third means for demodulating said second partial modulated binary-code pulse train to provide a second partial demodulated rectangular binary-code pulse train;

first means for integrating said first partial demodulated binary-code pulse train to provide a first train of integrated pulses;

third and fourth gating means actuated by said square-wave and second control pulse trains in such manner that third gating means is closed during said first alternate square-wave voltage pulse train and is opened in response to said second alternate square-wave voltage and second control pulse trains for reading out said first integrated pulse train to provide a first train of read-out pulses and further in such manner that said fourth gating means is closed during said second alternate square-wave voltage pulse train and is opened in response to said first alternate square-wave voltage and second control pulse trains

for reading out said second integrated pulse train to provide a second train of read-out pulses;

means for converting said first and second read-out pulse trains into a two-phase rectangular binary-code pulse train as a replica of said train of two-phase binary code pulses modulating said input signal;

and means for utilizing said replica two-phase rectangular binary-code pulse train.

5. The regenerator according to claim 4 in which said plurality of control rectangular pulse trains includes a third rectangular pulse train lagging said second control pulse train by a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses;

and said regenerator also including fifth and sixth gating means responsive to said square-wave and third control pulse trains in such manner that said fifth gating means is closed during said first alternate square-wave pulse train and is opened in response to said second alternate square-wave and third control pulse trains to discharge said first integrated pulse train in said first integrating means and further in such manner that said sixth gating means is closed during said second alternate square-wave pulse train and is opened in response to said first alternate square-wave and third control pulse trains to discharge said second integrated pulse train in said second integrating means.

6. A rectangular code pulse regenerator, comprising:

a source of an input signal modulated with a modulating train of two-phase rectangular binary-code pulses;

means for demodulating a first portion of said modulated input signal to produce a demodulated rectangular binary-code pulse train;

means for translating said demodulated binary-code pulse train into a plurality of control rectangular pulse trains; a first of said control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses and second alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second alternate square-wave voltage pulses occurring during the time interval of an elementary code of said demodulated binary-code pulse train; a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said demodulated binary-code pulse train, each of said second control pulses having the time duration shorter than one-half the time duration of said elementary code; and a third of said plurality of control pulse trains comprising a rectangular pulse train lagging said second control pulse train by a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses;

first and second gating means actuated by said square-wave pulse trains and a second portion of said modulated input signal in such manner that said first gating means is opened to transmit a train of first alternate elementary codes of said modulated input signal therethrough to provide a first partial modulated rectangular binary-code pulse train of said modulated input signal while said gating means is closed and further in such manner that said second gating means is opened to transmit a train of second alternate elementary codes of said modulated input signal therethrough to provide a second partial demodulated rectangular binary-code pulse train of said modulated input signal while said first gating means is closed;

second means for demodulating said first partial modulated binary-code pulse train to provide a first partial demodulated rectangular binary-code pulse train;

third means for demodulating said second partial modulated binary-code pulse train to provide a second partial demodulated rectangular binary-code pulse train;

first means for integrating said first partial demodulated binary-code pulse train to provide a first train of integrated pulses;

second means for integrating said second partial demodulated binary-code pulse train to provide a second train of integrated pulses;

third and fourth gating means actuated by said square-wave and second and third control pulse trains in such manner that said third and fourth gating means are closed in response to said first alternate square-wave pulse train while said first integrating means is integrating said first partial demodulated binary-code pulse train and further in such manner that said third gating means is opened in response to said second alternate square-wave and second control pulse trains to read-out said first integrated pulse train to provide a first train of read-out pulses and said fourth gating means is opened in response to said alternate square-wave and third control pulse trains to discharge said first integrated pulse train in said first integrating means;

fifth and sixth gating means activated by said square-wave and second and third control pulse trains in such manner that said fifth and sixth gating means are closed in response to said second alternate square-wave pulse train while said second integrating means is integrating said second partial demodulated binary-code pulse train and further in such manner that said fifth gating means is opened in response to said first alternate square-wave and second control pulse trains to read-out said second integrated pulse train to provide a second train of read-out pulses and said sixth gating means is opened in response to said first alternate square-wave and third control pulse trains to discharge said second integrated pulse train in said second integrating means;

means for converting said first and second read-out pulse trains into a two-phase rectangular binary-code pulse train as a replica of said two-phase rectangular binary-code pulse train modulating said input signal; and

means for utilizing said replica two-phase rectangular binary-code pulse train.

7. A rectangular pulse train regenerator, comprising:

a source of an input signal four-phase modulated with two modulating trains of different two-phase rectangular binary-code pulses;

means for demodulating said two different two-phase modulated input signal to provide a first demodulated rectangular binary-code pulse train including first and third phases separated by 180° from each other and a second demodulated rectangular binary-code pulse train including second and fourth phases separated by 180° from each other, said first and third phases separated from said second and fourth phases by 90°;

means for translating a first portion of said first demodulated pulse train into a plurality of control rectangular pulse trains; a first of said control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second alternate square-wave voltage pulses occurring during the time interval of an elementary code of said first demodulated rectangular binary-code pulse train; and a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said first demodulated pulse train, each of said sec-

ond control pulses having a time duration shorter than one-half the time duration of said elementary code;

first and second gating means activated by said square-wave control pulse trains and a second portion of said first demodulated pulse train in such manner that said first gating means is opened in response to said first alternate square-wave pulse train for transmitting first alternate elementary codes of said last-mentioned demodulated pulse train therethrough to provide a first partial demodulated pulse train of said last-mentioned demodulated pulse train while said second gating means is closed and further in such manner that said second gating means is opened in response to said second alternate square-wave pulse train for transmitting second alternate elementary codes of said first demodulated pulse train therethrough to provide a second partial demodulated pulse train of said last-mentioned demodulated pulse train while said first gating means is closed;

third and fourth gating means activated by said square-wave control pulse trains and second demodulated pulse train in such manner that said third gating means is opened in response to said first alternate square-wave pulse train for transmitting first alternate elementary codes of said last-mentioned demodulated pulse train therethrough to provide a first partial demodulated pulse train of said last-mentioned demodulated pulse train when said fourth gating means is closed and further in such manner that said fourth gating means is opened in response to said alternate square-wave pulse train for transmitting second alternate elementary codes of said second demodulated pulse train therethrough to provide a second partial demodulated pulse train of said last-mentioned demodulated pulse train while said third gating means is closed;

first means for integrating said first partial demodulated pulse train of said first demodulated pulse train to provide a first train of integrated pulses;

second means for integrating said first partial demodulated pulse train to provide a second train of integrated pulses;

third means for integrating said second partial demodulated pulse train of said first demodulated pulse train to provide a third train of integrated pulses;

fourth means for integrating said second partial demodulated pulse train of said second demodulated pulse train to provide a fourth train of integrated pulses;

fifth and sixth gating means activated by said square-wave and second control pulse trains in such manner that fifth gating means is closed during said first alternate square-wave pulse train and is opened in response to said second square-wave and second control pulse trains for reading out said first and second integrated pulse trains to provide first and second discrete read-out pulse trains, respectively, and further in such manner that said sixth gating means is closed during said second alternate square-wave pulse train and is opened in response to said first alternate square-wave and second control pulse trains for reading out said third and fourth integrated pulse trains to provide third and fourth discrete read-out pulse trains, respectively;

means for converting said first and third read-out pulse trains into a two-phase rectangular binary-code pulse train as a replica of one of said two two-phase rectangular binary-code pulse trains modulating said input signal and including first and third phases;

means for converting said second and fourth read-out pulse trains into a two-phase rectangular binary-code pulse train as a replica of the other of said two two-phase rectangular binary-code pulse trains modulating said input signal and including second and fourth phases;

and means for utilizing said first and second-mentioned replica pulse trains.

8. The regenerator according to claim 7 in which said plurality of control rectangular pulse trains includes a third rectangular pulse train lagging said second control rectangular pulse train by a time duration equal to the time duration of code of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses; and

said regenerator also including seventh and eighth gating means activated by said square-wave and third control pulse trains in such manner that said seventh gating means is closed during said first alternate square-wave pulse train and is opened in response to said second alternate square-wave and third control pulse trains to discharge said first and second integrated pulse trains in said first and second integrating means, respectively, and further in such manner that said eighth gating means is closed during said second alternate square-wave pulse train and is opened in response to said first alternate square-wave and third control pulse trains to discharge said third and fourth integrated pulse trains in said third and fourth integrating means, respectively.

9. A rectangular pulse train regenerator, comprising:

a source of an input signal four-phase modulated with two modulating trains of different two-phase rectangular binary-code pulses;

means for demodulating said two different two-phase modulated input signal to provide a first demodulated rectangular binary-code pulse train including first and third phases separated by 180° from each other and a second demodulated rectangular binary-code pulse train including second and fourth phases separated by 180° from each other, said first and third phases separated by 90° from said second and fourth phases;

means for translating a first portion of said first demodulated pulse train into a plurality of control rectangular pulse trains; a first of said control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate square-wave pulses constitute identical pulses and second alternate square-wave pulses constitute identical pulses, each of said first and second alternate square-wave pulses occurring during the time interval of an elementary code of said first demodulated pulse train; a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said last-mentioned first demodulated pulse train, each of said second control pulses having a time duration shorter than one-half the time duration of said elementary code; and a third of said plurality of control pulse trains comprising a rectangular pulse train lagging said second control pulse train by a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses;

first and second gating means activated by said square-wave control pulse trains and a second portion of said first demodulated pulse train in such manner that said first gating means is opened in response to said first alternate square-wave pulse train for transmitting first alternate elementary codes of said last-mentioned demodulated pulse train therethrough to provide a first partial demodulated pulse train of said last-mentioned first demodulated pulse train while said second gating means is closed and further in such manner that said second gating means is opened in

response to said second alternate square-wave pulse train for transmitting second alternate elementary codes of said last-mentioned first demodulated pulse trains therethrough to provide a second partial demodualted pulse train of said last-mentioned first demodulated pulse train while said first gating means is closed;

third and fourth gating means activated by said square-wave pulse trains and second demodulated pulse train in such manner that said third gating means is opened in response to said first alternate square-wave pulse train for transmitting first alternate elementary codes of said last-mentioned second demodulated pulse train therethrough to provide a first partial demodulated pulse train of said last-mentioned second demodulated pulse train while said fourth gating means is closed and further in such manner that said fourth gating means is opened in response to said second alternate square-wave pulse train for transmitting second alternate elementary codes of said last-mentioned second demodulated pulse train therethrough to provide a second partial demodulated pulse train of said last-mentioned second demodulated pulse train while said third gating means is closed;

first means for integrating said first partial demodulated pulse train of said first demodulated pulse train to provide a first train of integrated pulses;

second means for integrating said first partial demodulated pulse train of said second demodulated pulse train to provide a second train of integrated pulses;

third means for integrating said second partial demodulated pulse train of said first demodulated pulse train to provide a third train of integrated pulses;

fourth means for integrating said second partial demodulated pulse train of said second demodulated pulse train to provide a fourth train of integrated pulses;

fifth and sixth gating means activated by said square-wave pulse trains and second and third control pulse trains in such manner that said fifth and sixth gating means are closed during said first alternate square-wave pulse train and further in such manner that said fifth gating means is opened in response to said second alternate square-wave and second control pulse trains for reading out said first and second integrated pulse trains as first and second discrete read-out pulse trains, respectively, and said sixth gating means is opened in response to said second alternate square-wave and third control pulse trains to discharge said first and second integrated pulse trains in said first and second integrating means, respectively;

seventh and eighth gating means activated by said square-wave pulse trains and second and third control pulse trains in such manner that seventh and eighth gating means are closed during said second alternate square-wave pulse train and further in such manner that seventh gating means is opened in response to said first alternate square-wave and second control pulse trains for reading out said third and fourth integrated pulse trains as third and fourth discrete read-out pulse trains, respectively, and said eighth gating means is opened in response to said first alternate square-wave and third control pulse trains to discharge said third and fourth integrated pulse trains in said third and fourth integrating means, respectively;

means for converting said first and third read-out pulse trains into a two-phase rectangular binary-code pulse train as a replica of one of said two two-phase rectangular binary-code pulse trains modulating said input signal and including first and third phases;

means for converting said second and fourth read-out pulse trains into a two-phase rectangular binary-code pulse train as a replica of the other of said two two-phase rectangular binary-code pulse trains modulating said input signal and including second and fourth phases; and

means for utilizing said first and second-mentioned replica pulse trains.

10. A rectangular pulse train regenerator, comprising:

a source of an input signal four-phase modulated by two modulating trains of different two-phase rectangular binary-code pulses;

first means for demodulating said input signal as modulated with one of said two two-phase modulating signals to provide a first demodulated rectangular binary-code pulse train including first and third phases separated from each other by 180°;

means for translating said first demodulated pulse train into a plurality of control rectangular pulse trains; a first of said control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second square-wave pulses occurring during the time interval of an elementary code of said first demodulated pulse train; and a second of said plurality of control pulse trains comprising a rectangular pulse train synchronized with said first demodulated pulse train, each of said second control pulses having a time duration shorter than one-half the time duration of said elementary code;

first and second gating means activated by said square-wave pulse trains and four-phase modulated input signal in such manner that said first gating means is opened in response to said first alternate square-wave pulse train to transmit first alternate elementary codes of said four-phase modulated input signal therethrough to provide a first partial train of said last-mentioned four-phase modulated input signal while said second gating means is closed and further in such manner that said second gating means is opened in response to said second alternate square-wave pulse train to transmit second alternate elementary codes of said four-phase modulated input signal therethrough to provide a second partial train of said last-mentioned four-phase modulated input signal while said first gating means is closed;

second means for demodulating said first partial train of said four-phase input signal to provide a first partial demodulated rectangular binary-code pulse train having said first and third phases separated by 180° and a second partial demodulated rectangular binary-code pulse train having second and fourth phases separated from each other by 180°; said first and third phases separated from said second and fourth phases by 90°;

second means for demodulating said second partial train of said four-phase input signal to provide a third partial demodulated rectangular binary-code pulse trains having said first and third phases and a fourth partial demodulated rectangular binary-code pulse train having said second and fourth phases;

first means for integrating said first partial demodulated pulse train to provide a first train of integrated pulses;

second means for integrating said second partial demodulated pulse train to provide a second train of integrated pulses;

third means for integrating said third partial demodulated pulse train to provide a third train of integrated pulses;

fourth means for integrating said fourth partial demodulated pulse train to provide a fourth train of integrated pulses;

third and fourth gating means activated by said square-wave and second control pulse trains in such man-

ner that said third gating means is closed during said first alternate squarewave pulse train and is opened in response to said second alternate squarewave and second control pulse trains for reading out said first and second integrated pulse trains to provide first and second discrete read-out pulse trains, respectively, and further in such manner that said fourth gating means is closed during said second alternate squarewave pulse train and is opened in response to said first alternate squarewave and second control pulse trains for reading out said third and fourth integrated pulse trains to provide third and fourth discrete read-out pulse trains, respectively;

means for converting said first and third read-out pulse trains into a two-phase rectangular binary-code pulse train having said first and third phases as a replica of said one two-phase modulating pulse train having first and third phases;

means for converting said second and fourth read-out pulse trains into a two-phase rectangular binary-code pulse train having said second and fourth phases as a replica of the other of said two two-phase modulating pulse trains having second and fourth phases; and

means for utilizing said first and second-mentioned replica pulse trains.

11. The regenerator according to claim **10** in which said plurality of control rectangular pulse trains includes a third rectangular pulse train lagging said second rectangular pulse train by a time duration equal to the time duration of each of said second control pulses, each third control pulses having a time duration equal to the time duration of each of said second control pulses;

said regenerator also including fifth and sixth gating means activated by said square-wave and third control pulse trains in such manner that said fifth gating means is closed during said first alternate square-wave pulse train and is opened in response to said second alternate squarewave and third control pulse trains to discharge said first and second integrated pulse trains in said first and second integration means, respectively, and further in such manner that sixth gating means is closed during said second alternate square-wave pulse train and is opened in response to said first alternate squarewave and third control pulse trains to discharge said third and fourth integrated pulse trains in said third and fourth integrating means, respectively.

12. A rectangular pulse train regenerator, comprising:

a source of an input signal four-phase modulated with two modulating trains of different two-phase rectangular binary-code pulses;

first means for demodulating said input signal as modulated with one of said two two-phase rectangular binary-code pulse trains to produce a first demodulated rectangular binary-code pulse train including first and third phases separated from each other by 180°;

means for translating said first demodulated pulse train into a plurality of control rectangular pulse trains; a first of said control pulse trains comprising a square-wave pulse train having successively different voltage pulses of which first alternate voltage pulses constitute identical square-wave voltage pulses and second alternate voltage pulses constitute identical square-wave voltage pulses, each of said first and second square-wave pulses occurring during the time interval of an elementary code of said first demodulated pulse train; a second of said plurality of control pulse trains comprising rectangular pulse train synchronized with said first demodulated pulse train, each of said second control pulses having a time duration shorter than one-half the time duration of said elementary code; and a third of said plurality of control pulse trains including a third rectangular pulse train lagging said second rectangular pulse train by a time duration equal to the time duration of each of said second control pulses, each of said third control pulses having a time duration equal to the time duration of each of said second control pulses.

first and second gating means activated by said square-wave pulse trains and four-phase modulated input signal in such manner that said first gating means is opened in response to said first alternate square-wave pulse train to transmit first alternate elementary codes of said four-phase modulated input signal therethrough to provide a first partial train of said last-mentioned four-phase modulated input signal while said second gating means is closed and further in such manner that said second gating means is opened in response to said second alternate square-wave pulse train to transmit second alternate elementary codes of said four-phase modulated input signal therethrough to provide a second partial train of said last-mentioned four-phase modulated input signal while said first gating means is closed;

second means for demodulating said first partial train of said four-phase modulated input signal to produce a first partial demodulated rectangular binary-code pulse train including said first and third phases and a second partial demodulated rectangular binary-code pulse train including second and fourth phases separated from each other by 180°; said first and third phases separated from said second and fourth phases by 90°;

third means for demodulating said second partial train of said four-phase modulated input signal to produce a third partial demodulated rectangular binary-code pulse train including said first and third phases and a fourth partial demodulated rectangular binary-code pulse train including said second and fourth phases;

first means for integrating said first partial demodulated pulse train to provide a first train of integrated pulses;

second means for integrating said second partial demodulated pulse train to provide a second train of integrated pulses;

third means for integrating said third partial demodulated pulse train to provide a third train of integrated pulses;

fourth means for integrating said fourth partial demodulated pulse train to provide a fourth train of integrated pulses;

third and fourth gating means activated by said square-wave and second and third control pulse trains in such manner that third and fourth gating means are closed during said first alternate square-wave pulse train and further in such manner that third gating means is opened in response to said second alternate square-wave and second control pulse trains to read-out said first and second integrated pulse trains as first and second discrete read-out pulse trains, respectively, and said fourth gating means is opened in response to said second alternate square wave and third control pulse trains to discharge said first and second integrated pulse trains in said first and second integrating means, respectively;

fifth and sixth means activated by said square-wave and second and third pulse trains in such manner that said fifth and sixth gating means are closed during said second alternate square-wave pulse train and further in such manner that said fifth gating means is opened in response to said first alternate square-wave and second control pulse trains to read-out said third and fourth discrete read-out pulse trains, respectively, and said sixth gating means is opened in response to said first alternate square-wave and third control pulse trains to discharge said third and fourth

integrated pulse trains in said third and fourth integrating means, respectively;

means for converting said first and third read-out pulse trains into a two-phase rectangular binary-code pulse train including first and third phases as a replica of said one modulating two-phase rectangular binary-code pulse train including said first and third phases;

means for converting said second and fourth read-out pulse trains into a two-phase rectangular binary-code pulse train including second and fourth phases as a replica of the other of said two two-phase rectangular binary-code pulse trains including second and fourth phases; and

means for utilizing said first and second-mentioned replica pulse trains.

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