(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
06 August 2020 (06.08.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/159560 A1

(51) International Patent Classification:
H01L 21/02 (2006.01) *H01L 21/66* (2006.01)
C23C 14/34 (2006.01) *H01L 21/67* (2006.01)

(21) International Application Number:
PCT/US2019/026686

(22) International Filing Date:
10 April 2019 (10.04.2019)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/797,484 28 January 2019 (28.01.2019) US

(71) Applicant: **KLA-TENCOR CORPORATION** [US/US]; Legal Department, One Technology Drive, Milpitas, California 95035 (US).

(72) Inventor: **GHINOVKER, Mark**; 69 HaTsayalim Street, Apt. 2, 20692 Yoqneam Ilit (IL).

(74) Agent: **MCANDREWS, Kevin** et al.; KLA-TENCOR CORPORATION, Legal Deparment, One Technolgy Drive, Milpitas, California 95035 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: MOIRÉ TARGET AND METHOD FOR USING THE SAME IN MEASURING MISREGISTRATION OF SEMICONDUCTOR DEVICES

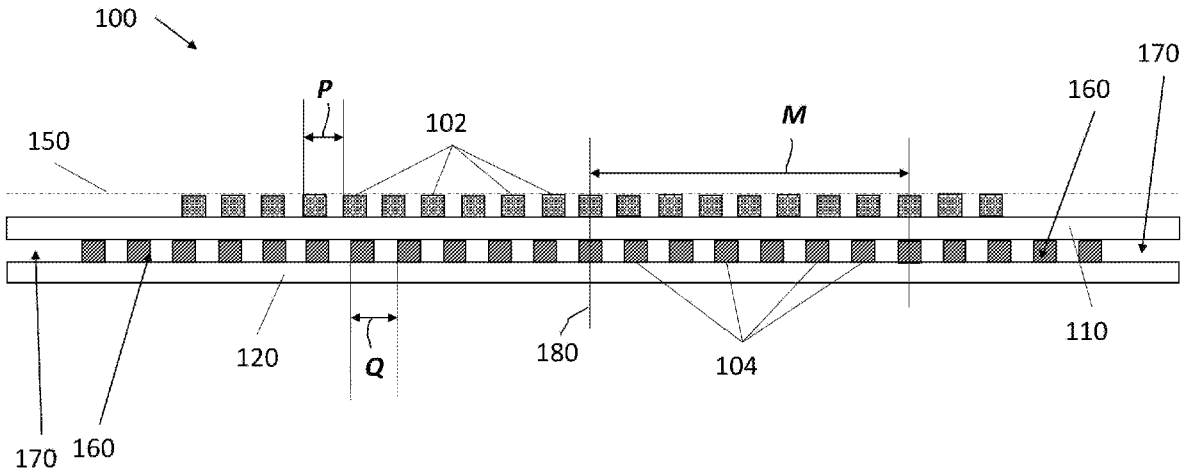

Fig. 1B

(57) Abstract: A target for use in the optical measurement of misregistration in the manufacture of semiconductor devices, the target including a first periodic structure formed on a first layer of a semiconductor device and having a first pitch along an axis and a second periodic structure formed on a second layer of the semiconductor device and having a second pitch along the axis, different from the first pitch, the second periodic structure extending beyond the first periodic structure along the axis.

WO 2020/159560 A1

MOIRÉ TARGET AND METHOD FOR USING THE SAME IN MEASURING MISREGISTRATION OF SEMICONDUCTOR DEVICES

REFERENCE TO RELATED APPLICATIONS

Reference is hereby made to U.S. Provisional Patent Application Serial No. 62/797,484, filed January 28, 2019 and entitled MOIRÉ IN BOX OVERLAY MARK DESIGN FOR REAL ESTATE REDUCTION AND IN DIE MEASUREMENTS, the disclosure of which is hereby incorporated by reference and priority of which is hereby claimed.

Reference is also made to the following patent and patent application, which are related to the subject matter of the present application, the disclosures of which are hereby incorporated by reference:

Applicant's U.S. Patent Publication No. US2018/0188663, filed February 24, 2017, published July 5, 2018 and entitled DEVICE-LIKE METROLOGY TARGETS; and

Applicant's U.S. Patent No. US7,440,105 entitled CONTINUOUSLY VARYING OFFSET MARK AND METHODS OF DETERMINING OVERLAY and issued on October 21, 2008.

FIELD OF THE INVENTION

The present invention relates to the measurement of misregistration in the manufacture of semiconductor devices and more particularly to targets useful in such measurement and methods for measurement of misregistration in the manufacture of semiconductor devices using such targets.

BACKGROUND OF THE INVENTION

Various types of targets are known in the art for the measurement of misregistration in the manufacture of semiconductor devices.

SUMMARY OF THE INVENTION

The present invention seeks to provide improved targets for the measurement of misregistration in the manufacture of semiconductor devices.

There is thus provided in accordance with a preferred embodiment of the present invention a target for use in the optical measurement of misregistration in the manufacture of semiconductor devices, the target including a first periodic structure formed on a first layer of a semiconductor device and having a first pitch along an axis and a second periodic structure formed on a second layer of the semiconductor device and having a second pitch along the axis, different from the first pitch, the second periodic structure extending beyond the first periodic structure along the axis.

Preferably, the first pitch and the second pitch are each smaller than 2000nm. More preferably, the first pitch and the second pitch are each smaller than 650 nm.

In accordance with a preferred embodiment of the present invention the first and second pitches are such that when the target is illuminated by light of at least one wavelength there results a moiré pattern having a third pitch, the third pitch being larger than the at least one wavelength.

Preferably, the target has an area smaller than 50 μm x 50 μm. More preferably, the target has an area smaller than 4 μm x 4 μm. Even more preferably, the target has an area smaller than 2 μm x 2 μm.

In accordance with a preferred embodiment of the present invention the target is rectangular in shape.

In accordance with a preferred embodiment of the present invention the second periodic structure extends beyond the first periodic structure in two opposite directions along the axis.

Preferably, the first periodic structure is defined by lines and spaces between the lines, the lines and the spaces between the lines each having a width equal to 50% of the first pitch. Alternatively, the first periodic structure is defined by lines and spaces between the lines, the lines each having a width of 10% – 90% of the first pitch.

In accordance with a preferred embodiment of the present invention each of the lines is defined by a plurality of sub-lines and sub-spaces between the sub-lines.

Additionally, the sub-lines and sub-spaces between the sub-lines have a pitch of approximately 12 nm – 50 nm.

In accordance with a preferred embodiment of the present invention the second periodic structure is defined by lines and spaces between the lines, the lines and the spaces between the lines each having a width equal to 50% of the second pitch. Alternatively, the second periodic structure is defined by lines and spaces between the lines, the lines each having a width of 10% – 90% of the second pitch.

Preferably, each of the lines of the second periodic structure is defined by a plurality of sub-lines and sub-spaces between the sub-lines. Additionally, the sub-lines and sub-spaces between the sub-lines of the second periodic structure have a pitch of approximately 12 nm – 50 nm.

There is also provided in accordance with another preferred embodiment of the present invention a method of measuring misregistration in the manufacture of semiconductor devices, the method including providing a multilayered semiconductor device including at least a first layer and a second layer, wherein the device includes a target including a first periodic structure formed on the first layer and having a first pitch along an axis and a second periodic structure formed on the second layer and having a second pitch along the axis, different from the first pitch, the second periodic structure extending beyond the first periodic structure along the axis, illuminating the target with light of at least one wavelength, resulting in a moiré pattern characterized by a third pitch and performing analysis of the moiré pattern to ascertain misregistration of the first layer and the second layer along the axis.

Preferably, the target has an area smaller than 50 μm x 50 μm. More preferably, the target has an area smaller than 4 μm x 4 μm. Even more preferably, the target has an area smaller than 2 μm x 2 μm.

In accordance with a preferred embodiment of the present invention the target is rectangular in shape.

In accordance with a preferred embodiment of the present invention the second periodic structure extends beyond the first periodic structure in two opposite directions along the axis.

Preferably, the first pitch and the second pitch are each smaller than the at least one wavelength. Additionally or alternatively, the third pitch is larger than the at

least one wavelength. Alternatively, the first pitch and the second pitch are each larger than the at least one wavelength.

In accordance with a preferred embodiment of the present invention the first periodic structure is defined by lines and spaces between the lines, the lines and the spaces between the lines each having a width equal to 50% of the first pitch.

In accordance with a preferred embodiment of the present invention the first periodic structure is defined by lines and spaces between the lines, the lines each having a width of 10% – 90% of the first pitch.

Preferably, each of the lines is defined by a plurality of sub-lines and sub-spaces between the sub-lines. Additionally, the sub-lines and sub-spaces between the sub-lines have a pitch of approximately 12 nm – 50 nm.

In accordance with a preferred embodiment of the present invention the second periodic structure is defined by lines and spaces between the lines, the lines and the spaces between the lines of the second periodic structure each having a width equal to 50% of the second pitch.

In accordance with a preferred embodiment of the present invention the second periodic structure is defined by lines and spaces between the lines, the lines each having a width of 10% – 90% of the first pitch.

Preferably, each of the lines of the second periodic structure is defined by a plurality of sub-lines and sub-spaces between the sub-lines. Additionally, the sub-lines and sub-spaces between the sub-lines have a pitch of approximately 12 nm – 50 nm.

Preferably, the second periodic structure is characterized by a first center of symmetry, the illuminating of the target results in a signal from the target, the signal including a sinusoidal variation due to the moiré pattern, the sinusoidal variation characterized by a second center of symmetry and the analysis of the moiré pattern to ascertain the misregistration of the first layer and the second layer along the axis includes comparison of locations of the first center of symmetry and the second center of symmetry.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

Figs. 1A and 1B are simplified respective top view and sectional side view illustrations of a target for the measurement of misregistration in the manufacture of semiconductor devices, constructed and operative in accordance with a preferred embodiment of the present invention in a registration operative orientation;

Figs. 2A and 2B are simplified respective top view and sectional side view illustrations of the target of Figs. 1A & 1B in a non-registration operative orientation;

Fig. 3 is a simplified top view illustration of a first target layer, forming part of the target of Figs. 1A – 2B;

Fig. 4 is a simplified top view illustration of a second target layer, forming part of the target of Figs. 1A – 2B; and

Fig. 5 is a simplified flowchart illustrating a method of measuring misregistration in the manufacture of semiconductor devices using the target of Figs. 1A – 4.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference is now made to Figs. 1A – 4, which illustrate a target for the measurement of misregistration in the manufacture of semiconductor devices, constructed and operative in accordance with a preferred embodiment of the present invention. It is appreciated that the target is formed of indicia formed on two patterned layers of a semiconductor device. The layers may be mutually adjacent but need not be, and may be separated by a height ranging from 100 nm to over 10 μm. The upper layer is at least partially transparent to photons.

It is a requirement in the manufacture of most semiconductor devices having multiple patterned layers of conductors that the various layers be maintained in

strict spatial registration, preferably to within a tolerance of less than 10 nm, and more preferably to within a tolerance of less than 3 nm.

The present invention seeks to provide a target, which enables misregistration of patterned layers of a semiconductor device to be optically measured to extremely high accuracy, preferably measuring misregistration in the range of 0 – 1000 nm and more preferably in the range of 0 – 50 nm.

Broadly stated, the target includes a first periodic structure formed on a first layer of a semiconductor device and having a first pitch along an axis and a second periodic structure formed on a second layer of the semiconductor device and having a second pitch along that axis, different from the first pitch, the second periodic structure including extended portions, which extend beyond the first periodic structure for approximately 500 nm in opposite directions along that axis. Additionally, the target preferably includes a pair of unpatterned zones on the second layer of approximately 500 nm in opposite directions along the axis beyond the ends of the second periodic structure. The extended portions of the second periodic structure together with the unpatterned zones make it possible to readily optically detect the ends of the second periodic structure, and thus its center of symmetry.

When suitably illuminated, the first and second periodic structures together form a moiré pattern, and the relative positions of the first and second periodic structures along the axis define the position of the moiré pattern along the axis. As is well known in the art, a small shift between the first and second periodic structures along the axis results in a significantly larger corresponding shift in the position of the moiré pattern relative to the second periodic structure along the axis. More specifically, the shift of the moiré pattern relative to the second periodic structure is larger than the shift between the first and second periodic structures by a factor F, as defined in equation 1:

$$F = \frac{Q}{|P-Q|} \qquad \text{(Eq. 1)}$$

Wherein P is the pitch of the first periodic structure and Q is the pitch of the second periodic structure.

Figs. 1A and 1B show a target 100 including a pair of mutually overlaid first and second periodic structures 102 and 104, shown here as first and second arrays of mutually parallel lines formed on first and second layers 110 and 120 respectively and arranged in registration along an axis 150. First and second periodic structures 102 and

104 have respective first and second pitches P and Q. Target 100 preferably has an area smaller than 50 μm x 50 μm, and more preferably an area smaller than 4 μm x 4 μm, and even more preferably an area smaller than 2 μm x 2 μm. In a preferred embodiment of the present invention, target 100 is rectangular in shape. In another embodiment of the present invention, target 100 is square in shape.

Second periodic structure 104 includes extended portions 160 on second layer 120, which extend beyond first periodic structure 102 on first layer 110 for approximately 500 nm in opposite directions along axis 150. Additionally, the target preferably includes a pair of unpatterned zones 170 on second layer 120 of approximately 500 nm in opposite directions along axis 150 beyond the ends of second periodic structure 104. Extended portions 160 together with unpatterned zones 170 make it possible to readily optically detect the ends of second periodic structure 104, and thus a center of symmetry 180 of second periodic structure 104.

As described hereinabove, it is appreciated that first and second layers 110 and 120 may be mutually adjacent but need not be, and may be separated by a height ranging from 100 nm to over 10 μm. The upper layer, here shown as first layer 110, is at least partially transparent to photons. It is further appreciated that while Figs. 1A – 4 depict first periodic structure 102 arranged above second periodic structure 104, targets 100 and 200 may also be formed with second periodic structure 104 arranged above first periodic structure 102.

Together, when suitably illuminated, first periodic structure 102 and second periodic structure 104 form a moiré pattern 190 having a pitch M. As is well known in the art, pitch M of moiré pattern 190 is determined by pitches P and Q, as defined in equation 2:

$$M = \frac{P \times Q}{|P - Q|} \qquad \text{(Eq. 2)}$$

Also shown in Fig. 1A is a representation of a signal 192 produced by an optical system used to image target 100 and moiré pattern 190 formed thereon. It is noted that moiré pattern 190 appears in signal 192 as a sinusoidal variation 194 having a center of symmetry 196. It is appreciated that signal 192, sinusoidal variation 194 and center of symmetry 196 are not drawn to scale.

Figs. 2A and 2B show the same target as shown in Figs. 1A and 1B, here designated by reference numeral 200, including mutually overlaid first and second

periodic structures 102 and 104, shown here as arrays of mutually parallel lines formed on first and second layers 110 and 120 respectively. Here, in contrast to that shown in Figs. 1A & 1B, first and second periodic structures 102 and 104 are seen to be out of registration along axis 150 by an amount R, where R is up to 1000 nm, in either direction along axis 150.

As described hereinabove with reference to Eq. 1, misregistration between first and second periodic structures 102 and 104 along axis 150 by an amount R results in a larger corresponding shift S in the position of moiré pattern 190 relative to second periodic structure 104 along axis 150.

Specifically, shift S of moiré pattern 190 relative to second periodic structure 104 along axis 150, and more particularly the shift in the position of center of symmetry 196 of sinusoidal variation 194 representing moiré pattern 190 relative to center of symmetry 180 of second periodic structure 104 along axis 150, between the mutual operative orientation of registration shown in Figs. 1A & 1B and the mutual operative orientation of non-registration shown in Figs. 2A & 2B is greater than the relative shift R of the first and second periodic structures by a factor F, as defined hereinabove in equation 1. Thus, the relative position S of moiré pattern 190 is substantially easier to detect by an optical misregistration system than is the relative shift R. It is appreciated that signal 192, sinusoidal variation 194 and center of symmetry 196 are not drawn to scale.

It is appreciated that since targets 100 and 200 enable the measurement of misregistration of first and second layers 110 and 120 only along axis 150, multiple targets 100 and 200 are preferably formed on a single semiconductor device, with axis 150 for each target being formed for useful measurements of misregistration and are arranged with their periodic structures along other axes, which are preferably perpendicular to axis 150.

Turning additionally to Fig. 3, it is seen that first periodic structure 102, such as that formed on first layer 110 in Figs. 1A – 2B is defined by a plurality of mutually parallel lines 210 and a plurality of mutually parallel spaces 212 between mutually parallel lines 210 arranged along axis 150. Preferably lines 210 have a pitch P of 250 – 2000 nm, and more preferably of 250 – 650 nm, and a line width of 10% – 90% of P, most typically 50% of P.

It is appreciated that lines 210 may be segmented, though they need not be. In an embodiment wherein lines 210 are segmented, as seen in enlargement A of Fig. 3, each one of lines 210 is defined by a plurality of sub-lines 214 and sub-spaces 216 between sub-lines 214. Preferably, the pitch of sub-lines 214 and sub-spaces 216 is the same as or close to the pitch of functional features on the semiconductor device on which targets 100 and 200 are printed. For example, a line 210 having a width of 420 nm may be formed of 15 sub-lines 214 and 15 sub-spaces 216 having a pitch U of 14 nm.

Turning additionally to Fig. 4, it is seen that second periodic structure 104, such as that formed on second layer 120 in Figs. 1A – 2B is defined by a plurality of mutually parallel lines 220 and a plurality of mutually parallel spaces 222 between mutually parallel lines 220 arranged along axis 150. Preferably lines 220 have a pitch Q of 250 – 2000 nm, and more preferably of 250 – 650 nm, and a line width of 10% – 90% of Q, most typically 50% of Q.

It is appreciated that lines 220 may be segmented, though they need not be. In an embodiment wherein lines 220 are segmented, as seen in enlargement A of Fig. 4, each one of lines 220 is defined by a plurality of sub-lines 224 and sub-spaces 226 between sub-lines 224. Preferably, the pitch of sub-lines 224 and sub-spaces 226 is the same as or close to the pitch of functional features on the semiconductor device on which targets 100 and 200 are printed. For example, a line 220 having a width of 420 nm may be formed of 15 sub-lines 224 and 15 sub-spaces 226 having a pitch V of 14 nm.

In a preferred embodiment of the present invention, neither P nor Q is optically resolvable by a tool to optically measure misregistration, such as an Archer™ 600, commercially available from KLA-Tencor Corporation of Milpitas, CA, USA. It is appreciated that P and Q are related to each other in such a way that pitch M of resulting moiré pattern 190, as defined hereinabove with reference to equation 2, is optically resolvable by the tool used to measure misregistration, preferably by pitch M being larger than the wavelength of light used to measure misregistration. In another embodiment of the present invention, P and Q are optically resolvable by the tool used to measure misregistration.

Reference is now made to Fig. 5, which is a simplified flowchart illustrating a method 300 of measuring misregistration in the manufacture of semiconductor devices using a target as described hereinabove with reference to Figs. 1A

– 4 either in registered orientation of target 100 or in misregistered orientation of target 200. As seen at a first step 302, a multilayered semiconductor device is provided. The multilayered semiconductor device of step 302 includes at least one target 100 or target 200, as described hereinabove with reference to Figs. 1 – 4.

As seen at a second step 304, a tool to optically measure misregistration, such as an Archer™ 600, commercially available from KLA-Tencor Corporation of Milpitas, CA, USA, is used to illuminate target 100 or target 200 with light having at least one wavelength, resulting in moiré pattern 190. Typical light useful in measuring target 100 or target 200 has a wavelength between 400 – 850 nm, though it is appreciated that light of other wavelengths may also be used. At this stage, signal 192 is detected. It is appreciated that in the region of moiré pattern 190, signal 192 exhibits a sinusoidal variation 194 having a periodicity identical to pitch M of moiré pattern 190.

In a preferred embodiment of the present invention, the light used to measure misregistration in step 304 is polarized light. In some embodiments of the present invention, second periodic structure 104 and moiré pattern 190 are measured with different tool setups, including, inter alia, with different wavelengths of light. In a preferred embodiment of the present invention, the light used to measure misregistration in step 304 is characterized by a wavelength or wavelengths larger than pitches P and Q of target 100 or target 200. In an alternate embodiment of the present invention, the light used to measure misregistration in step 304 is characterized by a wavelength or wavelengths smaller than pitches P and Q of target 100 or target 200.

As seen at a next step 306, signal 192, including sinusoidal variation 194 having center of symmetry 196 due to moiré pattern 190, is analyzed. It is noted that in the case of registration described hereinabove with reference to Figs. 1A and 1B, the center of symmetry 196 of sinusoidal variation 194 of signal 192 is located at the same position as center of symmetry 180 of second periodic structure 104. It is further noted that in the case of misregistration, as described hereinabove with reference to Figs. 2A and 2B, the center of symmetry 196 of sinusoidal variation 194 representing moiré pattern 190 is located at a distance equal to F×R from center of symmetry 180 of second periodic structure 104, where F is the factor defined hereinabove in eq. 1 and R is relative shift R of the first and second periodic structures as described hereinabove with reference to Figs. 2A and 2B.

Thus, at step 306, in the analysis of moiré pattern 190 to ascertain misregistration of first layer 110 and second layer 120 along axis 150, a comparison is made between the location of center of symmetry 180 of second periodic structure 104 and the location of center of symmetry 196 of sinusoidal variation 194 of signal 192, and misregistration between first and second layers 110 and 120 of the semiconductor device of step 302 is ascertained from the difference in the locations between center of symmetry 180 and center of symmetry 196.

For example, in a case wherein first periodic structure has a pitch P of 350 nm, second periodic structure has a pitch Q of 400 nm, and misregistration R is 1 nm, the change in relative position of center of symmetry 196 of sinusoidal variation 194 of signal 192 along axis 150 is 8 nm.

In an additional example, in a case wherein first periodic structure has a pitch P of 312 nm, second periodic structure has a pitch Q of 260 nm, and misregistration R is 4 nm, the change in relative position center of symmetry 196 of sinusoidal variation 194 of signal 192 along axis 150 is 20 nm.

In a further example, in a case wherein first periodic structure has a pitch P of 500 nm, second periodic structure has a pitch Q of 550 nm, and misregistration R is 2 nm, the change in relative position of center of symmetry 196 of sinusoidal variation 194 of signal 192 along axis 150 is 22 nm.

It will be appreciated by persons skilled in the art that the present invention is not limited to what has been particularly shown and described hereinabove. The scope of the present invention includes both combinations and subcombinations of various features described hereinabove as well as modifications thereof, all of which are not in the prior art.

CLAIMS

1. A target for use in the optical measurement of misregistration in the manufacture of semiconductor devices, the target comprising:

a first periodic structure formed on a first layer of a semiconductor device and having a first pitch along an axis; and

a second periodic structure formed on a second layer of said semiconductor device and having a second pitch along said axis, different from said first pitch, said second periodic structure extending beyond said first periodic structure along said axis.

2. A target according to claim 1 and wherein said first pitch and said second pitch are each smaller than 2000 nm.

3. A target according to claim 1 and wherein said first pitch and said second pitch are each smaller than 650 nm.

4. A target according to any of claims 1 – 3 and wherein said first and second pitches are such that when said target is illuminated by light of at least one wavelength there results a moiré pattern having a third pitch, said third pitch being larger than said at least one wavelength.

5. A target according to any of claims 1 – 4 and wherein said target has an area smaller than 50 μm x 50 μm.

6. A target according to any of claims 1 – 4 and wherein said target has an area smaller than 4 μm x 4 μm.

7. A target according to any of claims 1 – 4 and wherein said target has an area smaller than 2 μm x 2 μm.

8. A target according to any of claims 1 – 7 and wherein said target is rectangular in shape.

9. A target according to any of claims 1 – 8 and wherein said second periodic structure extends beyond said first periodic structure in two opposite directions along said axis.

10. A target according to any of claims 1 – 9 and wherein said first periodic structure is defined by lines and spaces between said lines, said lines and said spaces between said lines each having a width equal to 50% of said first pitch.

11. A target according to any of claims 1 – 9 and wherein said first periodic structure is defined by lines and spaces between said lines, said lines each having a width of 10% – 90% of said first pitch.

12. A target according to claim 10 or claim 11 and wherein each of said lines of said first periodic structure is defined by a plurality of sub-lines and sub-spaces between said sub-lines.

13. A target according to claim 12 and wherein said sub-lines and sub-spaces between said sub-lines of said first periodic structure have a pitch of approximately 12 nm – 50 nm.

14. A target according to any of claims 1 – 13 and wherein said second periodic structure is defined by lines and spaces between said lines, said lines and said spaces between said lines each having a width equal to 50% of said second pitch.

15. A target according to any of claims 1 – 13 and wherein said second periodic structure is defined by lines and spaces between said lines, said lines each having a width of 10% – 90% of said second pitch.

16. A target according to claim 14 or claim 15 and wherein each of said lines of said second periodic structure is defined by a plurality of sub-lines and sub-spaces between said sub-lines.

17. A target according to claim 16 and wherein said sub-lines and sub-spaces between said sub-lines of said second periodic structure have a pitch of approximately 12 nm – 50 nm.

18. A method of measuring misregistration in the manufacture of semiconductor devices comprising:

providing a multilayered semiconductor device comprising at least a first layer and a second layer, wherein said device comprises a target comprising:

a first periodic structure formed on said first layer and having a first pitch along an axis; and

a second periodic structure formed on said second layer and having a second pitch along said axis, different from said first pitch, said second periodic structure extending beyond said first periodic structure along said axis;

illuminating said target with light of at least one wavelength, resulting in a moiré pattern characterized by a third pitch; and

performing analysis of said moiré pattern to ascertain misregistration of said first layer and said second layer along said axis.

19. A method of measuring misregistration in the manufacture of semiconductor devices according to claim 18 and wherein said target has an area smaller than 50 μm x 50 μm.

20. A method of measuring misregistration in the manufacture of semiconductor devices according to claim 18 and wherein said target has an area smaller than 4 μm x 4 μm.

21. A method of measuring misregistration in the manufacture of semiconductor devices according to claim 18 and wherein said target has an area smaller than 2 μm x 2 μm.

22. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 21 and wherein said target is rectangular in shape.

23. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 22 and wherein said second periodic structure extends beyond said first periodic structure in two opposite directions along said axis.

24. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 23 and wherein said first pitch and said second pitch are each smaller than said at least one wavelength.

25. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 24 and wherein said third pitch is larger than said at least one wavelength.

26. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 23 and wherein said first pitch and said second pitch are each larger than said at least one wavelength.

27. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 26 and wherein said first periodic structure is defined by lines and spaces between said lines, said lines and said spaces between said lines of said first periodic structure each having a width equal to 50% of said first pitch.

28. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 26 and wherein said first periodic structure is defined by lines and spaces between said lines, said lines of said first periodic structure each having a width of 10% – 90% of said first pitch.

29. A method of measuring misregistration in the manufacture of semiconductor devices according to claims 27 or claim 28 and wherein each of said lines of said first periodic structure is defined by a plurality of sub-lines and sub-spaces between said sub-lines.

30. A method of measuring misregistration in the manufacture of semiconductor devices according to claim 29 and wherein said sub-lines and sub-spaces between said sub-lines of said first periodic structure have a pitch of approximately 12 nm – 50 nm.

31. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 30 and wherein said second periodic structure is defined by lines and spaces between said lines, said lines and said spaces between said lines of said second periodic structure each having a width equal to 50% of said second pitch.

32. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 30 and wherein said second periodic structure is defined by lines and spaces between said lines, said lines of said second periodic structure each having a width of 10% – 90% of said second pitch.

33. A method of measuring misregistration in the manufacture of semiconductor devices according to claims 31 or claim 32 and wherein each of said lines of said second periodic structure is defined by a plurality of sub-lines and sub-spaces between said sub-lines.

34. A method of measuring misregistration in the manufacture of semiconductor devices according to claim 33 and wherein said sub-lines and sub-spaces between said sub-lines of said second periodic structure have a pitch of approximately 12 nm – 50 nm.

35. A method of measuring misregistration in the manufacture of semiconductor devices according to any of claims 18 – 34 and wherein:

said second periodic structure is characterized by a first center of symmetry;

said illuminating of said target results in a signal from said target, said signal comprising a sinusoidal variation due to said moiré pattern, said sinusoidal variation characterized by a second center of symmetry; and

said analysis of said moiré pattern to ascertain said misregistration of said first layer and said second layer along said axis comprises comparison of locations of said first center of symmetry and said second center of symmetry.

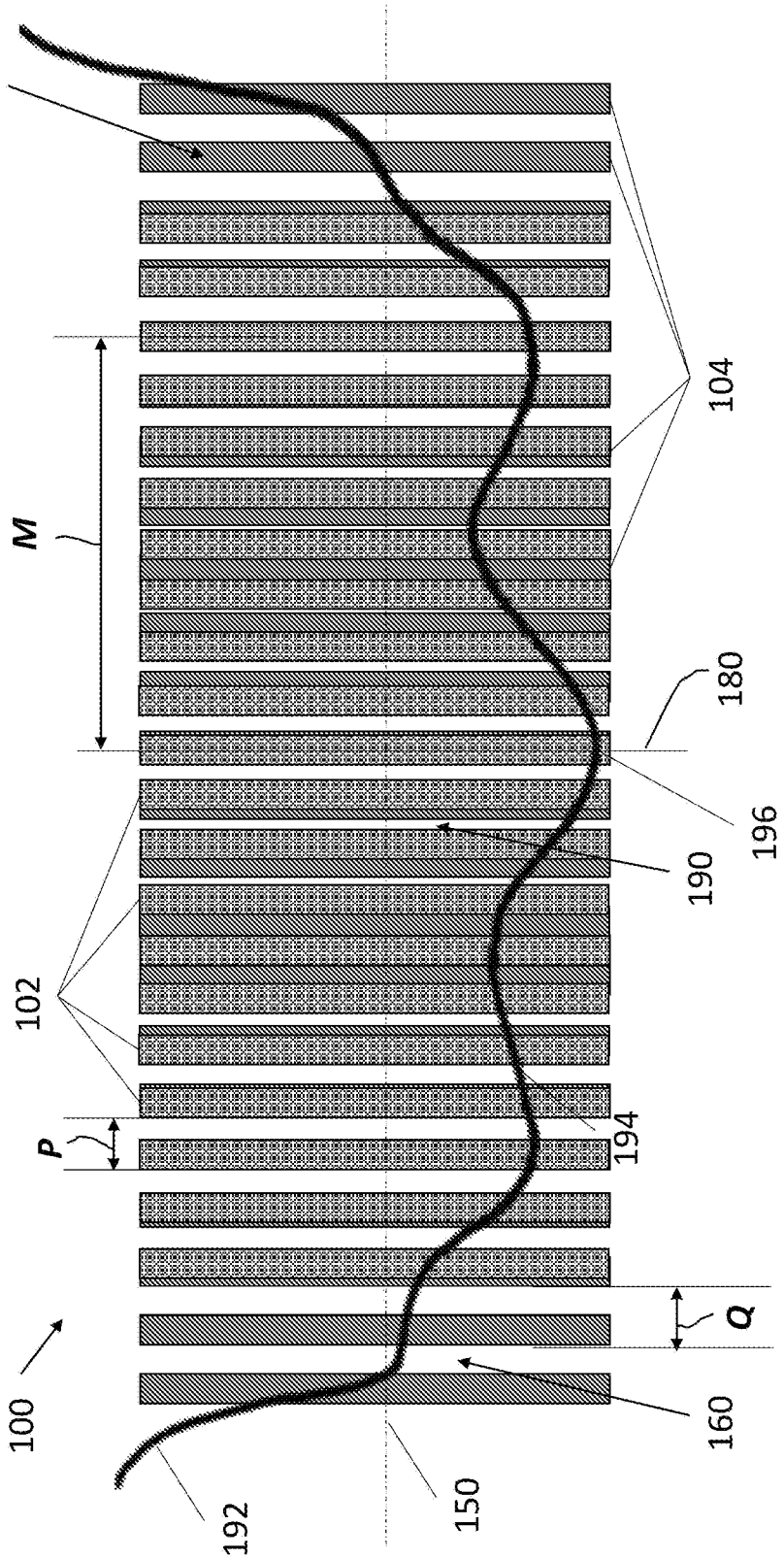

Fig. 1A

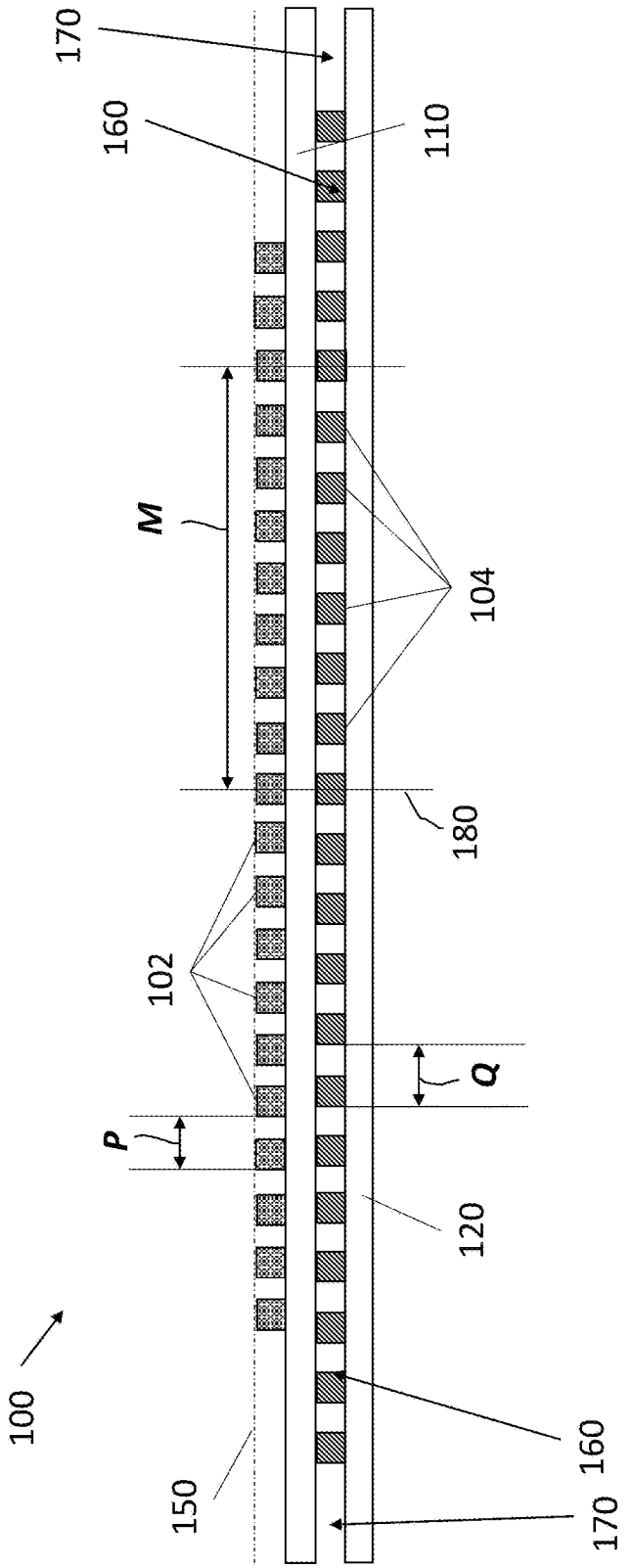

Fig. 1B

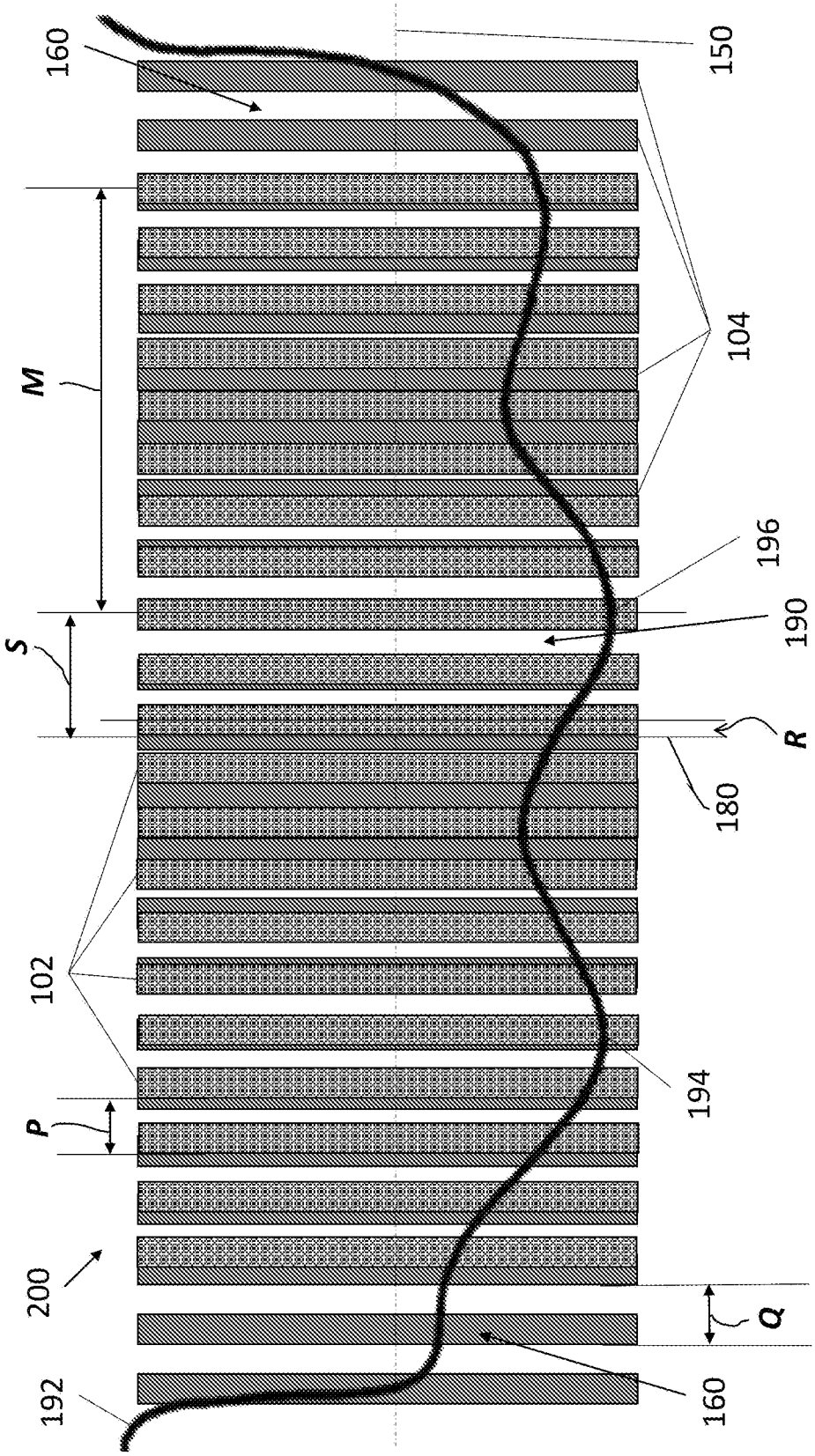

Fig. 2A

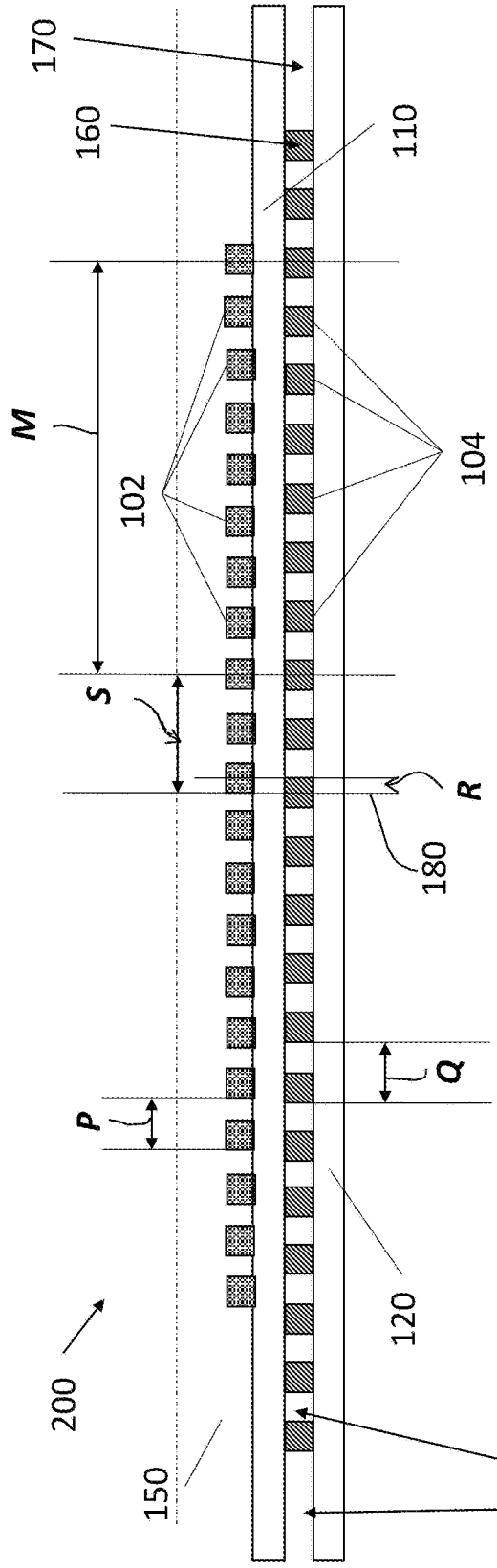

Fig. 2B

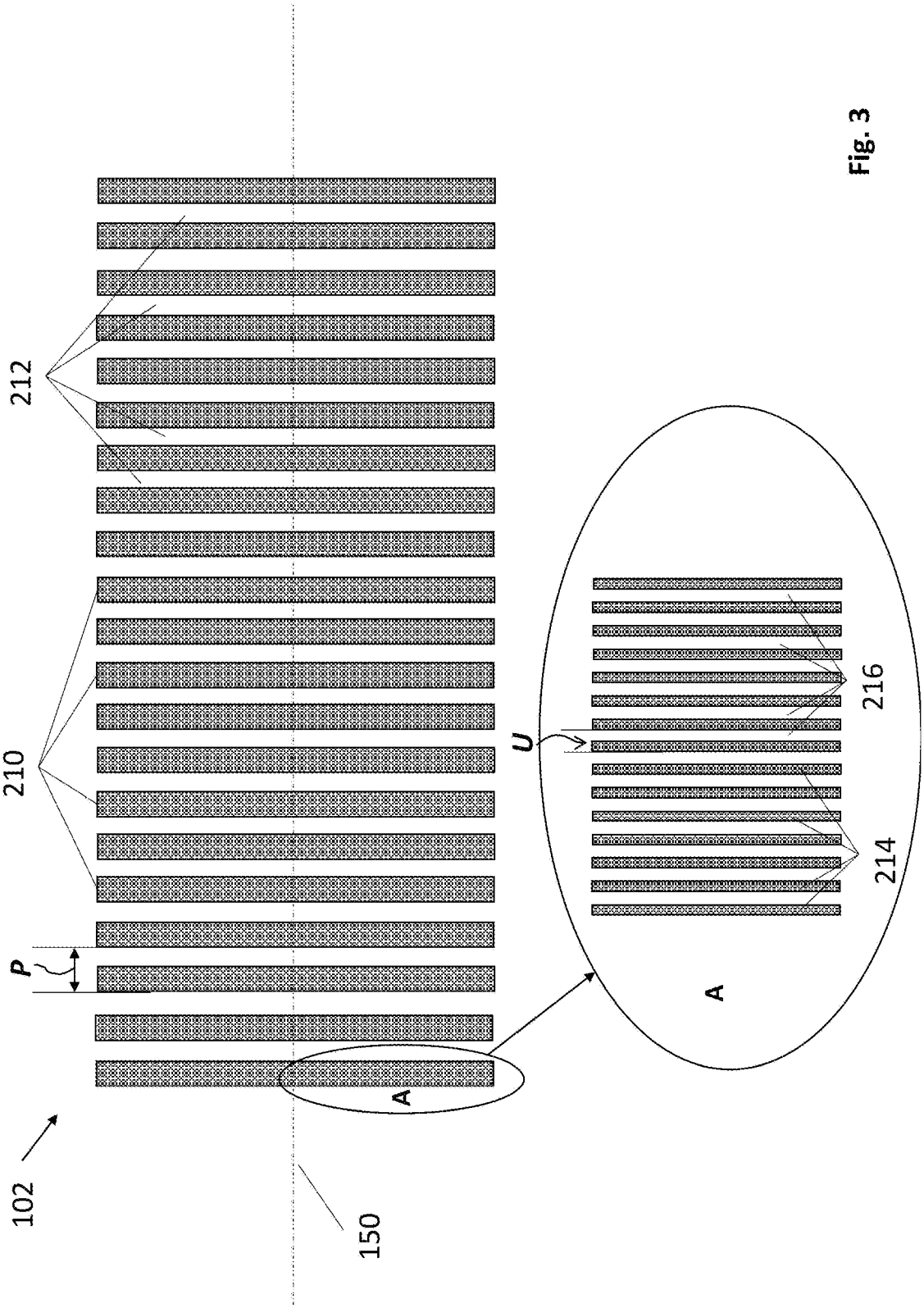

Fig. 3

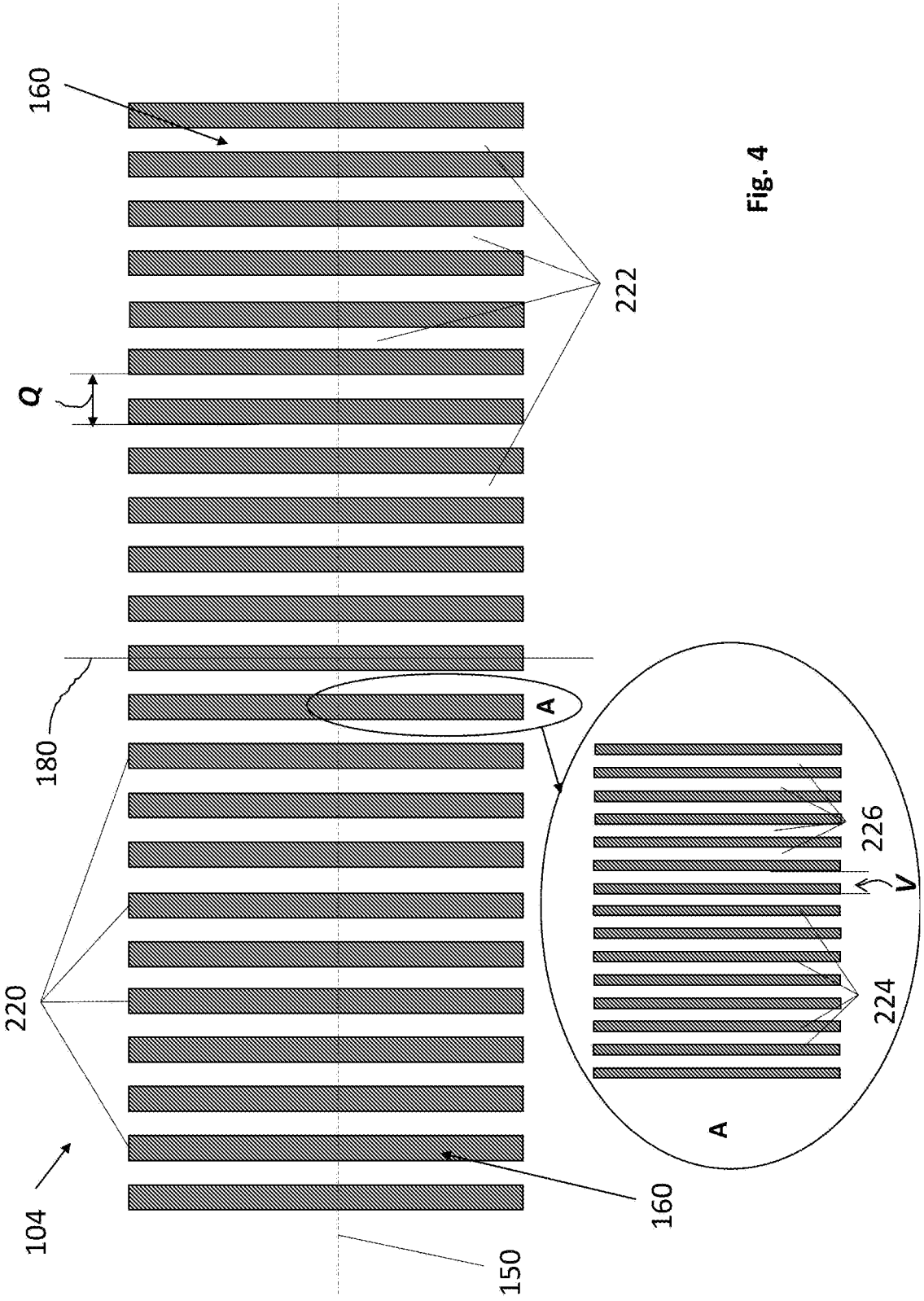

Fig. 4

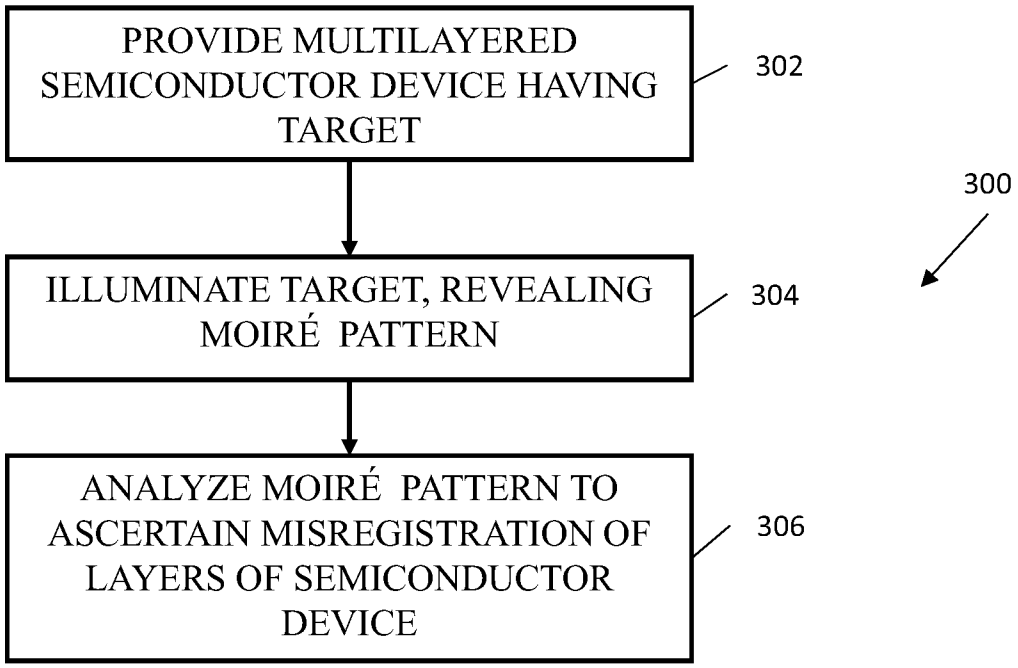
PROVIDE MULTILAYERED SEMICONDUCTOR DEVICE HAVING TARGET
302
300
ILLUMINATE TARGET, REVEALING MOIRÉ PATTERN
304
ANALYZE MOIRÉ PATTERN TO ASCERTAIN MISREGISTRATION OF LAYERS OF SEMICONDUCTOR DEVICE
306

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/026686

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/02(2006.01)i, C23C 14/34(2006.01)i, H01L 21/66(2006.01)i, H01L 21/67(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/02; G01B 11/00; G01B 11/14; G01B 11/26; G06K 9/34; H01L 23/544; H04N 1/40; C23C 14/34; H01L 21/66; H01L 21/67

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: semiconductor, target, picth, moire pattern, misregistration

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7230705 B1 (WEIDONG YANG et al.) 12 June 2007 See column 4, lines 15-19, column 9, lines 15-26, column 13, lines 21-32, column 15, lines 24-31, column 21, lines 6-14, column 23, lines 19-23 and claim 1.	1-4,18-22
A	US 9182219 B1 (KLA-TENCOR CORPORATION) 10 November 2015 See claims 1-3 and figure 7.	1-4,18-22
A	US 7772710 B2 (RICHARD SILVER et al.) 10 August 2010 See claims 1, 11 and figures 4-8C.	1-4,18-22
A	US 2004-0061857 A1 (IBRAHIM ABDULHALIM et al.) 01 April 2004 See claims 1-2, 10 and figures 6-9a.	1-4,18-22
A	US 7826095 B2 (SHEN-GE WANG et al.) 02 November 2010 See claim 1 and figures 1, 10.	1-4,18-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2019 (25.10.2019)	**25 October 2019 (25.10.2019)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
PARK, Hye Lyun
Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/026686

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 13, 17, 30, 34
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 13, 17, 30, 34 are regarded to be unclear because these claims refer to multiple dependent claims which do not comply with PCT Rule 6.4(a).

3. ☒ Claims Nos.: 5-12, 14-16, 23-29, 31-33, 35
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/026686

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7230705 B1	12/06/2007	US 6982793 B1	03/01/2006
US 9182219 B1	10/11/2015	US 9123649 B1	01/09/2015
		US 9255787 B1	09/02/2016
		US 9429856 B1	30/08/2016
US 7772710 B2	10/08/2010	US 2008-0142998 A1	19/06/2008
US 2004-0061857 A1	01/04/2004	EP 1390692 A1	25/02/2004
		EP 1390692 B1	03/06/2015
		JP 2004-533114 A	28/10/2004
		JP 4520696 B2	11/08/2010
		US 10151584 B2	11/12/2018
		US 2003-0002043 A1	02/01/2003
		US 2004-0229471 A1	18/11/2004
		US 2005-0157297 A1	21/07/2005
		US 2005-0208685 A1	22/09/2005
		US 2006-0065625 A1	30/03/2006
		US 2006-0132807 A1	22/06/2006
		US 2006-0262326 A1	23/11/2006
		US 2007-0127025 A1	07/06/2007
		US 2009-0231584 A1	17/09/2009
		US 2010-0073688 A1	25/03/2010
		US 2014-0022563 A1	23/01/2014
		US 2015-0300815 A1	22/10/2015
		US 2016-0084639 A1	24/03/2016
		US 2017-0038198 A1	09/02/2017
		US 2018-0100735 A1	12/04/2018
		US 7656528 B2	02/02/2010
		US 8525994 B2	03/09/2013
		US 8570515 B2	29/10/2013
		US 9103662 B2	11/08/2015
		US 9234745 B2	12/01/2016
		US 9476698 B2	25/10/2016
		US 9835447 B2	05/12/2017
		WO 02-084213 A1	24/10/2002
US 7826095 B2	02/11/2010	EP 1947521 A2	23/07/2008
		EP 1947521 A3	09/09/2015
		EP 1947521 B1	27/06/2018
		JP 2008-178096 A	31/07/2008
		JP 5080286 B2	21/11/2012
		US 2008-0170280 A1	17/07/2008