(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 December 2005 (01.12.2005)

PCT

(10) International Publication Number
WO 2005/112577 A2

(51) International Patent Classification: Not classified

(21) International Application Number: PCT/US2005/016160

(22) International Filing Date: 10 May 2005 (10.05.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/845,984 14 May 2004 (14.05.2004) US

(71) Applicant (*for all designated States except US*): **APPLIED MATERIALS, INC.** [US/US]; 3050 Bowers Ave, Santa Clara, CA 95054 (US).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **SAMOILOV, Arkadaii V.** [US/US]; 1136 S. Mary Avenue, Sunnyvale, CA 96087 (US). **KIM, Yihwan** [KR/US]; 825 Heavenly Place, Milpitas, CA 95035 (US). **SANCHEZ, Errol** [US/US]; 5291 Gilford Court, Dublin, CA 94568 (US). **DALIDA, Nicholas C.** [US/US]; 3459 Deodara Street, Fremont, CA 94538 (US).

(74) Agents: **PATTERSON, B., Todd** et al.; Moser, Patterson & Sheridan, LLP, 3040 Post Oak Blvd., Suite 1500, Houston, TX 77056-6582 (US).

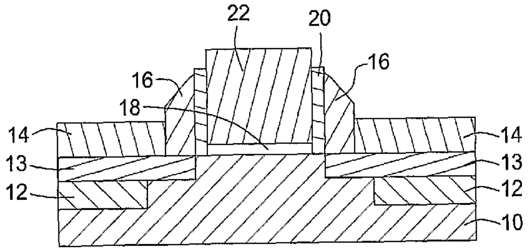
(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHODS TO FABRICATE MOSFET DEVICES USING SELECTIVE DEPOSITION PROCESSES



(57) Abstract: Embodiments of the invention provide processes to deposit silicon-containing materials, such as selectively depositing an epitaxial silicon-germanium material containing a high dopant concentration. In one example, a substrate is exposed to at least two different process gases to deposit one layer on top of another layer. One process gas contains dichlorosilane, a germanium source and an etchant while the next process gas contains silane and an etchant. In other examples, a process gas contains dichlorosilane, methylsilane and hydrogen chloride or silane, methylsilane and hydrogen chloride. In one aspect, a deposited layer has interstitial sites within a crystalline lattice and contains about 3 at% or less of carbon within the interstitial sites and is subsequently annealed to incorporate carbon within substitutional sites of the crystalline lattice. In another aspect, a silicon-germanium stack has first, second and third layers containing germanium concentrations of about 25 at% or less, about 25 at% or more and about 5 at% or less.

WO 2005/112577 A2

METHODS TO FABRICATE MOSFET DEVICES USING SELECTIVE DEPOSITION PROCESSES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention generally relate to the field of semiconductor manufacturing processes and devices, more particular, to methods of depositing silicon-containing materials and films to form semiconductor devices.

Description of the Related Art

[0002] As smaller transistors are manufactured, ultra shallow source/drain junctions are becoming more challenging to produce. According to the International Technology Roadmap for Semiconductors (ITRS), junction depth is required to be less than 30 nm for sub-100 nm CMOS (complementary metal-oxide semiconductor) devices. Recently, selective epitaxy has become a useful deposition process for silicon-germanium materials during formation of elevated source/drain and source/drain extension features. Source/drain extension features are manufactured by etching silicon to make a recessed source/drain feature and subsequently filling the etched surface with a selectively grown silicon-germanium epilayer. Selective epitaxy processes permits near complete dopant activation with *in-situ* doping, therefore removes or at least reduces the need of a post annealing process. Selective epitaxy processes and silicon etching processes may be used to accurately define junction depth. On the other hand, the ultra shallow source/drain junction inevitably results in increased series resistance. Also, junction consumption during silicide formation further increases the series resistance. In order to compensate for junction consumption, an elevated source/drain may be epitaxially and selectively grown on the junction.

[0003] Selective epitaxial deposition provides growth of epilayers on silicon moats with no growth on dielectric areas. Selective epitaxy may be used to deposit silicon or silicon-germanium materials in semiconductor devices, such as within elevated source/drains, source/drain extensions, contact plugs, and base layer deposition of bipolar devices. Generally, a selective epitaxy process involves two competing chemical reactions, deposition reactions and etching reactions. The deposition and etching reactions occur simultaneously with relatively different reaction rates on single crystalline silicon surfaces and on dielectric surfaces. A selective process window results in the deposition of a material on exposed silicon surfaces and not on exposed dielectric surfaces, by adjusting the concentration of an etchant gas (*e.g.,* HCl).

[0004] Although epitaxial deposition processes for depositing silicon-germanium materials are suitable for small dimensions, the processes do not readily form doped silicon-germanium, since the dopants react with hydrogen chloride. The process development of heavily boron doped (*e.g.,* higher than 5×10^{19} cm^{-3}) selective silicon-germanium epitaxy material is a much more complicated task because boron doping makes the process window for selective deposition narrow. Generally, when a deposition gas contains an increase of the boron concentration (*e.g.,* B_2H_6), an increase of the hydrogen chloride concentration is necessary to achieve selectivity due to the increase growth rate of deposited material on dielectric areas. The increased hydrogen chloride concentration reduces boron incorporation into the epilayers presumably because the B-Cl bond is stronger than Ge-Cl and Si-Cl bonds.

[0005] Currently, there are two popular applications for a selective silicon-based epitaxy process in junction formation of silicon-containing MOSFET (metal oxide semiconductor field effect transistor) devices. One application is to deposit elevated source/drain (S/D) films by a selective epitaxy process. Typically, the epitaxial layer is undoped silicon. Another application is to fill recessed junction areas with epitaxial silicon-containing material, usually containing germanium, carbon or a dopant.

[0006] MOSFET devices may contain a PMOS or a NMOS component, whereas the PMOS has a p-type channel, *i.e.,* holes are responsible for conduction in the channel and the NMOS has an n-type channel, *i.e.,* the electrons are responsible for conduction in the channel. For PMOS, the film in the recessed area usually contains silicon-germanium. For NMOS application, the film in the recessed area may contain silicon-carbon. A silicon-germanium material is used for PMOS application for several reasons. A silicon-germanium material incorporates more boron than silicon alone, thus the junction resistivity is lowered. Also, the silicon-germanium/silicide layer interface at the substrate surface has a lower Schottky barrier than the silicon/silicide interface. Further, a silicon-germanium layer grown epitaxially on the top of a silicon layer may have compressive stress inside the film because the lattice constant of silicon-germanium is larger than that of silicon. The compressive stress is transferred in the lateral dimension to create compressive strain in the PMOS channel and to increase mobility of the holes. For NMOS application, a silicon-carbon material may be used in the recessed areas to create tensile stress in the channel, since the lattice constant of silicon-carbon is smaller than that of silicon. The tensile stress is transferred into the channel and increases the electron mobility.

[0007] Therefore, there is a need to have a process for selectively and epitaxially depositing silicon and silicon-containing materials with an enriched dopant concentration. Furthermore, the process should be versatile to form silicon-containing materials with varied elemental concentrations.

SUMMARY OF THE INVENTION

[0008] In one embodiment, a method for forming a silicon-based material on a substrate is provided which includes exposing a substrate to a first process gas containing dichlorosilane, a germanium source, a first etchant and a carrier gas to deposit a first silicon-containing layer thereon and exposing the substrate to a second process gas containing silane and a second etchant to deposit a second silicon-containing layer thereon. In one example, the first process gas is formed by combining dichlorosilane with a flow rate in a range from about 50 standard cubic centimeters per minute (sccm) to about 200 sccm, germane with a flow rate in a range from about 0.5 sccm to about 5 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm and hydrogen with a flow rate in a range from about 10 standard liters per minute (slm) to about 30 slm. In another example, the method provides the second process gas is formed by combining silane with a flow rate in a range from about 50 sccm to about 200 sccm and hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm. The method further provides that the first silicon-containing layer and the second silicon-containing layer may be formed by a selective deposition process. In one example, the first and second silicon-containing layers have a boron concentration within a range from about 5×10^{19} atoms/cm^3 to about 2×10^{20} atoms/cm^3.

[0009] In another embodiment, a method for forming a silicon-based material on a substrate in a process chamber is provided which includes exposing a substrate to a process gas containing dichlorosilane, methylsilane, hydrogen chloride and hydrogen to deposit a silicon-containing layer thereon. In one example, the process gas is formed by combining dichlorosilane with a flow rate in a range from about 20 sccm to about 400 sccm, methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm and the hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

[0010] In another embodiment, a method for forming a silicon-based material on a substrate within a process chamber is provided which includes exposing a substrate to a process gas containing silane, methylsilane, hydrogen chloride, and hydrogen to deposit a silicon-containing layer thereon. In one example, the process gas is formed by combining silane with a flow rate in a range from about 20 sccm to about 400 sccm, methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm and hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

[0011] In another embodiment, a method for forming a silicon-based material on a substrate within a process chamber is provided which includes exposing a substrate to a process gas containing silane, germane, methylsilane, hydrogen chloride and hydrogen to deposit a silicon-containing layer thereon. In one example, the process gas is formed by combining silane with a flow rate in a range from about 50 sccm to about 200 sccm, germane with a flow rate in a range from about 0.5 sccm to about 5 sccm, methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm and hydrogen with a flow rate in a range from about 10 slm to about 30 slm. The silicon-containing layer may be deposited with a composition containing silicon at a concentration of at least about 50 atomic percent (at%), carbon at a concentration of about 2 at% or less and germanium at a concentration in a range from about 15 at% to about 30 at%.

[0012] In another embodiment, a method for forming a silicon-based material on a substrate within a process chamber is provided which includes exposing a substrate to a process gas to deposit a silicon-containing layer thereon such that the first silicon-containing layer has interstitial sites within a crystalline lattice and contains about 3 at% or less of carbon within the interstitial sites. The method further provides annealing the silicon-containing layer to incorporate at least a portion of the carbon within substitutional sites of the crystalline lattice. In one example, the process gas is formed by combining dichlorosilane with a flow rate in a range from about 20 sccm to about 400 sccm, methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm and hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

[0013] In another embodiment, a method for forming a silicon-based material on a substrate is provided which includes depositing a first silicon-containing layer on a substrate, depositing a second silicon-containing layer on the first silicon-containing layer and depositing a third silicon-containing layer on the second silicon-containing layer. In one example, the first silicon-containing layer contains about 25 at% or less of germanium, the second silicon-containing layer contains about 25 at% or more of germanium and the third silicon-containing layer contains about 5 at% or less of germanium. In one example, the first process gas may be formed by combining dichlorosilane with a flow rate in a range from about 50 sccm to about 200 sccm, germane with a flow rate in a range from about 0.5 sccm to about 5 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm, a dopant precursor with a flow rate in a range from about 0.2 sccm to about 3 sccm and hydrogen with a flow rate in a range from about 10 slm to about 30 slm. In another example, the second process gas may be formed by combining dichlorosilane with a flow rate in a range from about 50 sccm to about 400 sccm, germane with a flow rate in a range from about 0.5 sccm to about 20 sccm, hydrogen chloride with a flow rate in a range from about 30 sccm to about 700 sccm, a dopant precursor with a flow rate in a range from about 0.2 sccm to about 6 sccm and hydrogen with a flow rate in a range from about 10 slm to about 30 slm. The third process gas may be formed by combining silane with a flow rate in a range from about 50 sccm to about 200 sccm and hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm. In one example, the first silicon-containing layer has a germanium concentration within a range from about 15 at% to about 25 at%, the second silicon-containing layer has a germanium concentration within a range from about 25 at% to about 35 at% and the third silicon-containing layer has a germanium concentration up to about 5 at%.

[0014] In another embodiment, a method for depositing a silicon-containing material on a substrate is provided which includes depositing a first silicon-containing layer containing a first germanium concentration of about 15 at% or more on the substrate and depositing a second silicon-containing layer containing a second germanium concentration of about 15 at% or less on the first silicon-containing layer. The method further provides exposing the substrate to air to form a native oxide layer, removing the native oxide layer to expose the second silicon-containing layer and depositing a third silicon-containing layer on the second silicon-containing layer.

[0015] In another embodiment, a method for depositing a silicon-containing material on a substrate is provided which includes depositing a first silicon-containing layer containing a first lattice strain epitaxially on the substrate and depositing a second silicon-containing layer containing a second lattice strain epitaxially on the first silicon-containing layer so that the second lattice strain is greater than the first lattice strain. The method further provides that the first and second silicon-containing layers may each contain silicon germanium, silicon carbon, silicon germanium carbon, dopants, derivatives thereof or combinations thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] So that the manner in which the above recited features of the invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0017] Figures 1A-1C show several devices with epitaxially deposited silicon-containing layer; and

[0018] Figures 2A-2F show schematic illustrations of fabrication techniques for a source/drain extension device within a MOSFET.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0019] Embodiments of the invention provide processes to deposit silicon-containing materials during the manufacture of device structures. The deposition processes selectively and epitaxially form silicon-containing materials on crystalline silicon surfaces of a substrate surface containing features. Selective epitaxial growth of the crystalline, silicon surfaces are achieved while the features are left bare due to the presence of an etchant (*e.g.,* HCl). The deposited silicon-containing materials or films may contain silicon, silicon-germanium or silicon-carbon materials. Also, the silicon-containing layers may be highly concentrated by boron, phosphorus or arsenic dopants. In one example, a silicon-containing layer has a boron concentration within a range from about 5×10^{19} atoms/cm^3 to about 2×10^{20} atoms/cm^3.

[0020] In some embodiments, the process utilizes the silicon precursor silane (SiH_4) during the deposition of silicon-containing materials. In other embodiments, the process utilizes the silicon precursor dichlorosilane (Cl_2SiH_2) during the deposition of silicon-containing materials. In another embodiment, a step-wise process using dichlorosilane in one step and silane in a later step is effective for minimizing defects in epitaxial layers while depositing silicon-containing materials for silicon-based devices.

[0021] Herein, "silicon-containing" materials, compounds, films or layers should be construed to include a composition containing at least silicon and may contain germanium, carbon, boron, arsenic and/or phosphorus. Other elements, such as metals, halogens or hydrogen may be incorporated within a silicon-containing material, film or layer, usually as impurities. Silicon-containing materials may be represented by an abbreviation, such as Si for silicon, SiGe for silicon-germanium, SiC for silicon-carbon and SiGeC for silicon-germanium-carbon. The abbreviations do not represent chemical equations with stoichiometrical relationships, nor represent any particular reduction/oxidation state of the silicon-containing materials.

[0022] The deposition processes are extremely useful for depositing silicon-containing layers within MOSFET and bipolar transistors as depicted in Figures 1A-1C. Herein, silicon-containing materials are the deposited layers or films and include silicon, silicon-germanium, silicon-carbon, silicon-germanium-carbon, doped variants thereof or combinations thereof, epitaxially grown during the processes herein. The silicon-containing materials include strained or unstrained layers within the films.

[0023] Figures 1A-1B show a MOSFET device containing epitaxially grown silicon-containing materials deposited on the source/drain features by deposition process described herein. A silicon-containing material grown from the crystal lattice of the underlying layer maintains the lattice structure of the underlying layer. In one embodiment, Figure 1A illustrates the silicon-containing material deposited as a recessed source/drain, while in another embodiment, Figure 1B shows silicon-containing materials deposited as a recessed source/drain and an elevated source/drain (ESD).

[0024] Source/drain layer 12 may be formed by exposing lower layer 10 to an ion implantation process. Generally, lower layer 10 is doped n-type while source/drain layer 12 is doped p-type. Silicon-containing layer 13 is selectively and epitaxially deposited on source/drain layer 12 or directly on lower layer 10 and silicon-containing layer 14 is selectively and epitaxially deposited on silicon-containing layer 13 by the various deposition processes described herein. Gate oxide layer 18 bridges segmented silicon-containing layer 13 and usually contains silicon dioxide, silicon oxynitride or hafnium oxide. Partially encompassing gate oxide layer 18 is spacer 16, which usually contains an isolation material such as a nitride/oxide stack (*e.g.,* $Si_3N_4/SiO_2/Si_3N_4$). Gate layer 22 (*e.g.,* polysilicon) may have protective layer 19, such as silicon dioxide, along the perpendicular sides, as in Figure 1A. Alternately, gate layer 22 may have spacer 16 and off-set layers 20 (*e.g.,* Si_3N_4) disposed on either side.

[0025] In another embodiment, Figure 1C depicts base layer 34 of a bipolar transistor deposited on n-type collector layer 32 disposed on lower layer 30. Base layer 34 contains silicon-containing material epitaxially deposited by the processes described herein. The device further includes isolation layer 33 (*e.g.,* SiO_2 or Si_3N_4), contact layer 36 (*e.g.,* heavily doped poly-Si), off-set layer 38 (*e.g.,* Si_3N_4), and a second isolation layer 40 (*e.g.,* SiO_2 or Si_3N_4).

[0026] In one embodiment, as depicted in Figures 2A-2F, a source/drain extension is formed within a MOSFET wherein the silicon-containing layers are epitaxially and selectively deposited on the surface of the substrate. Figure 2A depicts source/drain layer 132 formed by implanting ions into the surface of substrate 130. The segments of source/drain layer 132 are bridged by gate 136 formed on gate oxide layer 135 and subsequent deposition of off-set layer 134. A portion of the source/drain layer is etched and wet-cleaned, to produce recess 138, as in Figure 2B. A portion of gate 136 may also be etched, or optionally a hardmask may be deposited prior to etching to avoid removal of gate material.

[0027] Figure 2C illustrates silicon-containing layer 140 (*e.g.,* epitaxial or monocrystalline material) selectively deposited on source/drain layer 132 and silicon-containing layer 142 (*e.g.,* polycrystalline or amorphous crystalline material) selectively deposited on gate 136 by deposition process described herein. In one example, a hardmask is disposed over gate 136 before a deposition process, so that gate 136 remains exposed upon removal of the hardmask. In another example, silicon-containing layers 140 and 142 are deposited simultaneously without depositing on off-set layer 134. In one embodiment, silicon-containing layers 140 and 142 are silicon-germanium containing layers with a germanium concentration in a range from about 1 atomic percent (at%) to about 50 at%, preferably about 25 at% or less. Multiple silicon-germanium containing layers containing varying amount of elements may be stacked to form silicon-containing layer 140 with a graded elemental concentration. For example, a first silicon-germanium layer may be deposited with a germanium concentration in a range from about 15 at% to about 25 at% and a second silicon-germanium layer may be deposited with a germanium concentration in a range from about 25 at% to about 35 at%. In another example, a first silicon-germanium layer may be deposited with a germanium concentration in a range from about 15 at% to about 25 at%, a second silicon-germanium layer may be deposited with a germanium concentration in a range from about 25 at% to about 35 at% and a third silicon-containing layer may be deposited with no germanium or with a germanium concentration up to about 5 at%.

[0028] In another embodiment, silicon-containing layers 140 and 142 are silicon-carbon containing layers with a carbon concentration in a range from about 200 ppm to about 5 at%, preferably about 3 at% or less, more preferably from about 1 at% to about 2 at%, for example, about 1.5 at%. In another embodiment, silicon-containing layers 140 and 142 are silicon-germanium-carbon containing layers with a germanium concentration in a range from about 1 at% to about 50 at%, preferably about 25 at% or less and a carbon concentration in a range from about 200 ppm to about 5 at%, preferably about 3 at% or less, more preferably from about 1 at% to about 2 at%, for example, about 1.5 at%.

[0029] Multiple layers containing silicon, silicon-germanium, silicon-carbon or silicon-germanium-carbon may be deposited in varying order to form graded elemental concentrations of silicon-containing layer 140. The silicon-containing layers are generally doped with a dopant (*e.g.*, B, As or P) having a concentration in a range from about 1×10^{19} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3, preferably from about 5×10^{19} atoms/cm^3 to about 2×10^{20} atoms/cm^3. Dopants added in individual layers of silicon-containing material form graded doped layers. For example, silicon-containing layer 140 is formed by depositing a first silicon-germanium containing layer with a dopant concentration (*e.g.*, boron) in a range from about 5×10^{19} atoms/cm^3 to about 1×10^{20} atoms/cm^3 and a second silicon-germanium containing layer with a dopant concentration (*e.g.*, boron) in a range from about 1×10^{20} atoms/cm^3 to about 2×10^{20} atoms/cm^3.

[0030] Carbon incorporated in silicon-carbon containing layers and silicon-germanium-carbon containing layers is generally located in interstitial sites of the crystalline lattice immediately following the deposition of the silicon-containing layer. The interstitial carbon content is about 10 at% or less, preferably less than about 5 at% and more preferably in a range from about 1 at% to about 3 at%, for example, about 2 at%. The silicon-containing layer may be annealed to incorporate at least a portion, if not all of the interstitial carbon into substitutional sites of the crystalline lattice. The annealing process may include a spike anneal, such as rapid thermal process (RTP), laser annealing or thermal annealing with an atmosphere of gas, such as oxygen, nitrogen, hydrogen, argon, helium or combinations thereof. The annealing process is conducted at a temperature in a range from about 800°C to about 1,200°C, preferably from about 1,050°C to about 1,100°C. The annealing process may occur immediately after the silicon-containing layer is deposited or after a variety of other process steps endured by the substrate.

[0031] During the next step, Figure 2D shows spacer 144, generally a nitride spacer (*e.g.,* Si_3N_4) deposited on the off-set layer 134. Spacer 144 is usually deposited within a different process chamber than the process chamber used to deposit silicon-containing layer 140. During the transfer between the two chambers, the substrate may be exposed to ambient conditions, such as atmospheric air at room temperature containing water and oxygen. Once spacer 144 has been deposited or an alternative process (*e.g.,* anneal, deposition or implant) conducted, the substrate may be exposed to ambient conditions a second time prior to depositing silicon-containing layers 146 and 148. In one example, an epitaxial layer (not shown) containing no germanium or a minimal concentration of germanium (*e.g.,* less than about 5 at%) is deposited on top of layer 140 prior to exposing the substrate to ambient conditions. The native oxides that are formed by the ambient conditions are removed easier from epitaxial layers containing minimal germanium concentrations than from an epitaxial layer formed with a germanium concentration greater than about 5 at%.

[0032] Figure 2E depicts elevated layer 148 epitaxially and selectively deposited from silicon-containing material, as described herein. Elevated layer 148 is deposited on layer 140 (*e.g.,* doped SiGe) while polysilicon is deposited on the silicon-containing layer 142 to produce polysilicon layer 146. Depending on the elemental concentrations of silicon-containing layer 142 and polysilicon deposited thereto, the elemental concentrations of polysilicon layer 146 will inheritably contain these elemental concentrations, including graded concentrations when both layers are different.

[0033] In a preferred embodiment, elevated layer 148 is epitaxially deposited silicon containing little or no germanium or carbon. However, in another embodiment, elevated layer 148 contains a low concentration of germanium or carbon. For example, elevated layer 148 may have about 5 at% or less germanium. In another example, elevated layer 148 may have about 2 at% or less carbon. Elevated layer 148 may also be doped with a dopant, such as boron, arsenic or phosphorus.

[0034] In the next step shown in Figure 2F, a metal layer 154 is deposited over the features and the device is exposed to an annealing process. The metal layer 154 may include cobalt, nickel or titanium, among other metals. During the annealing process, polysilicon layer 146 and elevated layer 148 are converted to metal silicide layers, 150 and 152, respectively. For example, cobalt may be deposited as metal layer 154 and is converted to metal silicide layers 150 and 152 containing cobalt silicide during an annealing process.

[0035] The silicon-containing material may be heavily doped with the *in-situ* dopants. Therefore, annealing steps of the prior art may be omitted and the overall throughput is shorter. An increase of carrier mobility along the channel and subsequent drive current is achieved with the optional addition of germanium and/or carbon into the silicon-containing material layer. Selectively grown epilayers of the silicon-containing material above the gate oxide level can compensate junction consumption during the silicidation, which can relieve concerns of high series resistance of ultra shallow junctions. These two applications can be implemented together as well as solely for CMOS device fabrication.

[0036] Silicon-containing materials formed by the deposition processes here may be to deposit silicon-containing films used by Bipolar (*e.g.*, base, emitter, collector, emitter contact), BiCMOS (*e.g.*, base, emitter, collector, emitter contact) and CMOS (*e.g.*, channel, source/drain, source/drain extension, elevated source/drain, substrate, strained silicon, silicon on insulator and contact plug). Other uses of the silicon-containing materials films may include gate, base contact, collector contact, emitter contact or elevated source/drain.

[0037] In one embodiment, a silicon-containing film is epitaxially grown as a silicon film. A substrate (*e.g.*, 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.*, silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.*, H_2 and/or N_2) and an etchant (*e.g.*, HCl). The flow rate of the silicon precursor is in a range from about 5 standard cubic centimeters per minute (sccm) to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 standard liters per minute (slm) to about 30 slm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained with a pressure in a range from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 50 Torr. The substrate is heated at a temperature in a range from about 500°C to about 1,000°C, preferably from about 600°C to about 900°C, more preferably from about 650°C to about 750°C, for example about 720°C. The mixture of reagents is thermally driven to react and epitaxially deposit crystalline silicon. The etchant removes any deposited amorphous silicon or polycrystalline silicon from dielectric features on the surface of the substrate. The process is conducted to form the deposited silicon-containing film with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing film has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing film has a thickness greater than 500 Å, such as about 1,000 Å.

[0038] Etchants are used to provide select areas of a feature on a substrate surface to be free of deposited silicon-containing materials. The etchant removes amorphous silicon or polysilicon growth that forms on the features at a faster rate than the etchant removes crystalline silicon growth from the crystalline surfaces, thus achieving selective epitaxial growth or deposition. Etchants that are useful during deposition processes as described herein include HCl, HF, HBr, Si_2Cl_6, $SiCl_4$, Cl_2SiH_2, CCl_4, Cl_2, derivatives thereof or combinations thereof.

[0039] Other silicon precursors, besides silane and dichlorosilane, which are useful while depositing silicon-containing materials include higher silanes, halogenated silanes and organosilanes. Higher silanes include the compounds with the empirical formula $Si_xH_{(2x+2)}$, such as disilane (Si_2H_6), trisilane (Si_3H_8), and tetrasilane (Si_4H_{10}), as well as others. Halogenated silanes include compounds with the empirical formula $X'_ySi_xH_{(2x+2-y)}$, where X' = F, Cl, Br or I, such as hexachlorodisilane (Si_2Cl_6), tetrachlorosilane ($SiCl_4$), dichlorosilane (Cl_2SiH_2) and trichlorosilane (Cl_3SiH). Organosilanes include compounds with the empirical formula $R_ySi_xH_{(2x+2-y)}$, where R = methyl, ethyl, propyl or butyl, such as methylsilane ($(CH_3)SiH_3$), dimethylsilane ($(CH_3)_2SiH_2$), ethylsilane ($(CH_3CH_2)SiH_3$), methyldisilane ($(CH_3)Si_2H_5$), dimethyldisilane ($(CH_3)_2Si_2H_4$) and hexamethyldisilane ($(CH_3)_6Si_2$). Organosilane compounds have been found to be advantageous silicon sources and carbon sources during embodiments of the present invention to incorporate carbon in to deposited silicon-containing material.

[0040] Carrier gases are used throughout the processes and include hydrogen (H_2), argon (Ar), nitrogen (N_2), helium (He), forming gas (N_2/H_2) or combinations thereof. In one example, hydrogen is used as a carrier gas. In another example nitrogen is used as a carrier gas. In one embodiment, a carrier gas during an epitaxial deposition process is conducted with neither hydrogen nor atomic hydrogen. However, an inert gas is used as a carrier gas, such as nitrogen, argon, helium or combinations thereof. Carrier gases may be combined in various ratios during some embodiments of the process. For example, a carrier gas may include nitrogen or argon to maintain available sites on the silicon-containing material film. The presence of hydrogen on the silicon-containing material surface limits the number of available sites (*i.e.*, passivates) for silicon or silicon-germanium to grow when an abundance of hydrogen is used as a carrier gas. Consequently, a passivated surface limits the growth rate at a given temperature, particularly at lower temperatures (e.g., <650°C). Therefore, a carrier gas of nitrogen and/or argon may be used during a process at lower temperature and reduce the thermal budget without sacrificing growth rate.

[0041] In another embodiment, a silicon-containing film is epitaxially grown as a silicon-germanium film. A substrate (*e.g.*, 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.*, silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.*, H_2 and/or N_2), a germanium source (*e.g.*, GeH_4) and an etchant (*e.g.*, HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 slm to about 30 slm. The flow rate of the germanium source is in a range from about 0.1 sccm to about 10 sccm, preferably from about 0.5 sccm to about 5 sccm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained with a pressure in a range from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon-containing material, namely a silicon germanium film. The etchant removes any deposited amorphous silicon-germanium compounds from dielectric features upon the surface of the substrate.

[0042] The process is conducted to form the deposited silicon-germanium film with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing film has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing film has a thickness greater than 500 Å, such as about 1,000 Å. The germanium concentration may be graded within the silicon-germanium film, preferably graded with a higher germanium concentration in the lower portion of the silicon-germanium film than in the upper portion of the silicon-germanium film. The germanium concentration of the silicon-germanium film is in a range from about 1 at% to about 30 at% of the silicon-germanium material, for example, about 20 at%.

[0043] Other germanium sources or precursors, besides germane, that are useful while depositing silicon-containing materials include higher germanes and organogermanes. Higher germanes include the compounds with the empirical formula $Ge_xH_{(2x+2)}$, such as digermane (Ge_2H_6), trigermane (Ge_3H_8) and tetragermane (Ge_4H_{10}), as well as others. Organogermanes include compounds with the empirical formula $R_yGe_xH_{(2x+2-y)}$, where R = methyl, ethyl, propyl or butyl, such as methylgermane ($(CH_3)GeH_3$), dimethylgermane ($(CH_3)_2GeH_2$), ethylgermane

($(CH_3CH_2)GeH_3$), methyldigermane ($(CH_3)Ge_2H_5$), dimethyldigermane ($(CH_3)_2Ge_2H_4$) and hexamethyldigermane ($(CH_3)_6Ge_2$). Germanes and organogermane compounds have been found to be an advantageous germanium sources and carbon sources during embodiments of the present invention to incorporate germanium and carbon in to the deposited silicon-containing materials, namely silicon-germanium and silicon-germanium-carbon materials. Germanium sources are often mixed with a carrier gas (*e.g.,* H_2) to dilute and therefore better control the germanium doses. For example, a germanium source with a flow rate in a range from about 0.5 sccm to about 5 sccm is equivalent to a flow of about 1% germanium source in a carrier gas with a flow rate in a range from about 50 sccm to about 500 sccm. Throughout the disclosure, the flow rate of germanium source ignores the flow rate of the carrier gas.

[0044] In another embodiment, a silicon-containing film is epitaxially grown as a doped silicon film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.,* silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a dopant (*e.g.,* B_2H_6) and an etchant (*e.g.,* HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 slm to about 30 slm. The flow rate of the dopant precursor is in a range from about 0.01 sccm to about 10 sccm, preferably from about 0.2 sccm to about 2 sccm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained with a pressure in a range from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The mixture of reagents is thermally driven to react and epitaxially deposit doped silicon films. The etchant removes any deposited amorphous silicon or polycrystalline silicon from dielectric features upon the surface of the substrate.

[0045] The process is conducted to form the deposited, doped silicon-containing film with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing film has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing film has a thickness greater than 500 Å, such as about 1,000 Å. The dopant concentration may be graded within the silicon film, preferably graded with a higher dopant concentration in the lower portion of the silicon film than in the upper portion of the silicon film.

[0046] Dopants provide the deposited silicon-containing materials with various conductive characteristics, such as directional electron flow in a controlled and desired pathway required by the electronic device. Films of the silicon-containing materials are doped with particular dopants to achieve the desired conductive characteristic. In one embodiment, the silicon-containing material is doped p-type, such as by using diborane to add boron at a concentration in a range from about 10^{15} atoms/cm^3 to about 10^{21} atoms/cm^3. In one embodiment, the p-type dopant has a concentration of at least 5×10^{19} atoms/cm^3. In another embodiment, the p-type dopant is in a range from about 1×10^{20} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3. In another embodiment, the silicon-containing material is doped n-type, such as with phosphorus and/or arsenic to a concentration in a range from about 10^{15} atoms/cm^3 to about 10^{21} atoms/cm^3.

[0047] Boron-containing dopants or dopant precursors that may be used during the deposition processes described herein include boranes and alkylboranes. Boranes may include borane, diborane, triborane, tetraborane, pentaborane, derivatives thereof, complexes thereof or combinations thereof. Alkylboranes include compounds with the empirical formula $R_xBH_{(3-x)}$, where R = methyl, ethyl, propyl or butyl and x = 0, 1, 2 or 3. Alkylboranes may include trimethylborane ($(CH_3)_3B$), dimethylborane ($(CH_3)_2BH$), triethylborane ($(CH_3CH_2)_3B$), diethylborane ($(CH_3CH_2)_2BH$), derivatives thereof, complexes thereof or combinations thereof. Dopant precursors also include arsine (AsH_3), phosphine (PH_3) and alkylphosphines, such as with the empirical formula $R_xPH_{(3-x)}$, where R = methyl, ethyl, propyl or butyl and x = 1, 2 or 3. Alkylphosphines include trimethylphosphine ($(CH_3)_3P$), dimethylphosphine ($(CH_3)_2PH$), triethylphosphine ($(CH_3CH_2)_3P$) and diethylphosphine ($(CH_3CH_2)_2PH$), derivatives thereof, complexes thereof or combinations thereof. Dopants are often mixed with a carrier gas (*e.g.*, H_2) to dilute and therefore better control the doping doses. For example, a flow rate of dopant in a range from about 0.2 sccm to about 2 sccm is equivalent to a flow of 1% dopant in a carrier gas with a flow rate in a range from about 20 sccm to about 200 sccm. Throughout the disclosure, the flow rate of dopant precursor ignores the flow rate of the carrier gas.

[0048] In another embodiment, a silicon-containing film is epitaxially grown to produce a doped silicon-germanium film. A substrate (*e.g.*, 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.*, silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.*, H_2 and/or N_2), a germanium source (*e.g.*, GeH_4), a dopant (*e.g.*, B_2H_6) and an etchant (*e.g.*, HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 slm to about 30 slm. The flow rate of the germanium source is in a range from about 0.1 sccm to about 10 sccm, preferably from about 0.5 sccm to about 5 sccm. The flow rate of the dopant precursor is in a range from about 0.01 sccm to about 10 sccm, preferably from about 0.2 sccm to about 3 sccm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon-containing material, namely a silicon germanium film. The etchant removes any deposited amorphous silicon-germanium from features upon the surface of the substrate. The process is conducted to form the doped silicon-germanium film with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing film has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing film has a thickness greater than 500 Å, such as about 1,000 Å. The germanium concentration and the dopant concentration may be graded within the doped silicon-germanium film, preferably graded with a higher germanium concentration and/or dopant concentration in the lower portion of the doped silicon-germanium film than in the upper portion of the doped silicon-germanium film. The germanium concentration is in a range from about 1 at% to about 50 at%, preferably from about 15 at% to about 35 at% of the silicon-germanium material. The boron concentration is in a range from about 1×10^{19} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3 of the silicon-germanium material, for example, about 1×10^{20} atoms/cm^3.

[0049] In another embodiment, a silicon-containing film is epitaxially grown as a silicon-carbon film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.,* silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a carbon source (*e.g.,* CH_3SiH_3) and an etchant (*e.g.,* HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 slm to about 30 slm. The flow rate of the carbon source is in a range from about 0.1 sccm to about 15 sccm, preferably from about 0.3 sccm to about 5 sccm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained with a pressure in a range from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon-containing material, namely a silicon carbon film. The etchant removes any deposited amorphous silicon-carbon materials from dielectric features upon the surface of the substrate.

[0050] The process is conducted to form the deposited silicon-carbon film with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing film has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing film has a thickness greater than 500 Å, such as about 1,000 Å. The carbon concentration may be graded within the silicon-carbon film, preferably graded with a higher carbon concentration in the lower portion of the silicon-carbon film than in the upper portion of the silicon-carbon film. The carbon concentration of the silicon-carbon film is in a range from about 200 ppm to about 5 at%, preferably from about 1 at% to about 3 at%, for example 1.5 at%.

[0051] Carbon sources useful for depositing silicon-containing materials containing carbon include organosilanes, alkyls, alkenes and alkynes of ethyl, propyl and butyl. Such carbon sources include methylsilane (CH_3SiH_3), dimethylsilane ($(CH_3)_2SiH_2$), ethylsilane ($CH_3CH_2SiH_3$), methane (CH_4), ethylene (C_2H_4), ethyne (C_2H_2), propane (C_3H_8), propene (C_3H_6), butyne (C_4H_6), as well as others. Carbon sources are often mixed with a carrier gas (*e.g.,* H_2) to dilute and therefore better control the carbon doses. For example, a carbon source with a flow rate in a range from about 0.3 sccm to about 5 sccm is equivalent to a flow of 1% carbon source in a carrier gas with a flow rate in a range from about 30 sccm to about 500 sccm. Throughout the disclosure, the flow rate of carbon source ignores the flow rate of the carrier gas.

[0052] In another embodiment, a silicon-containing film is epitaxially grown to produce a doped silicon-carbon film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.,* silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a carbon source (*e.g.,* CH_3SiH_3), a dopant (*e.g.,* B_2H_6) and an etchant (*e.g.,* HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 slm to about 30 slm. The flow rate of the carbon source is in a range from about 0.1 sccm to about 15 sccm, preferably from about 0.3 sccm to about 5 sccm. The flow rate of the dopant precursor is in a range from about 0.01 sccm to about 10 sccm, preferably from about 0.2 sccm to about 3 sccm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon-containing material, namely a doped silicon carbon film. The etchant removes any deposited amorphous silicon-carbon from features upon the surface of the substrate.

[0053] The process is conducted to form the doped silicon-carbon film with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing film has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing film has a thickness greater than 500 Å, such as about 1,000 Å. The carbon concentration and/or the dopant concentration may be graded within the doped silicon-carbon film, preferably graded with a higher carbon concentration and/or dopant concentration in the lower portion of the doped silicon-carbon film than in the upper portion of the doped silicon-carbon film. The carbon concentration of the doped silicon-carbon film is in a range from about 200 ppm to about 5 at%, preferably from about 1 at% to about 3 at%, for example 1.5 at%. The boron concentration is in a range from about 1×10^{19} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3 of the silicon-germanium material, for example, about 1×10^{20} atoms/cm^3.

[0054] In another embodiment of the invention, a silicon-containing film is epitaxially grown as a silicon-germanium-carbon film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.,* silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4), a carbon source (*e.g.,* CH_3SiH_3) and an etchant (*e.g.,* HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is from about 10 slm to about 30 slm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm, preferably from about 0.5 sccm to about 5 sccm. The flow rate of the carbon source is from about 0.1 sccm to about 50 sccm, preferably from about 0.3 sccm to about 5 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 500°C to about 700°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon-containing material, namely a silicon germanium carbon film. The etchant removes any deposited amorphous or polycrystalline silicon-germanium-carbon compounds from dielectric features upon the surface of the substrate.

[0055] The process is conducted to form the deposited silicon-germanium-carbon compound with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing material has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing material has a thickness greater than 500 Å, such as about 1,000 Å. The germanium concentration and/or the carbon concentration may be graded within the silicon-germanium-carbon film, preferably graded with a higher germanium concentration and/or carbon concentration in the lower portion of the silicon-germanium-carbon film than in the upper portion of the silicon-germanium-carbon film. The germanium is in a range from about 1 at% to about 50 at%, preferably from about 15 at% to about 35 at% of the silicon-germanium-carbon compound. The carbon concentration is in a range from about

200 ppm to about 5 at%, preferably from about 1 at% to about 3 at% of the silicon-germanium-carbon material.

[0056] In another embodiment of the invention, a silicon-containing material film is epitaxially grown as a doped silicon-germanium-carbon film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.,* silane or dichlorosilane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4), a carbon source (*e.g.,* CH_3SiH_3), a dopant (*e.g.,* B_2H_6) and an etchant (*e.g.,* HCl). The flow rate of the silicon precursor is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is from about 10 slm to about 30 slm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm, preferably from about 0.5 sccm to about 5 sccm. The flow rate of the carbon source is from about 0.1 sccm to about 50 sccm, preferably from about 0.3 sccm to about 5 sccm. The flow rate of the dopant precursor is from about 0.01 sccm to about 10 sccm, preferably from about 0.2 sccm to about 3 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably from about 1 Torr to about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 500°C to about 700°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon-containing material, namely a doped silicon germanium carbon film. The etchant removes any deposited amorphous or polycrystalline silicon-germanium-carbon materials from dielectric features upon the surface of the substrate.

[0057] The process is conducted to form a doped silicon-germanium-carbon material with a thickness in a range from about 10 Å to about 3,000 Å, for example, from about 40 Å to about 100 Å. In another example, the deposited silicon-containing material has a thickness in a range from about 200 Å to about 600 Å. In one embodiment, the silicon-containing material has a thickness greater than 500 Å, such as about 1,000 Å. The germanium concentration, the carbon concentration and/or the dopant concentration may be graded within the doped silicon-germanium-carbon film, preferably graded with a higher germanium concentration, carbon concentration and/or dopant concentration in the lower portion of the doped silicon-germanium-carbon film than in the upper portion of the doped silicon-germanium-carbon film. The germanium concentration is in a range from about 1 at% to about 50 at%, preferably from about 15 at% to about 35 at% of the doped silicon-germanium-carbon material. The carbon concentration is in a range from about 0.1 at% to about 5 at%, preferably from about 1 at% to about 3 at% of the doped silicon-germanium-carbon material. The boron concentration is in a range from about 1×10^{19} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3 of the silicon-germanium material, for example, about 1×10^{20} atoms/cm^3.

[0058] In another embodiment, a second silicon-containing film is epitaxially grown by using dichlorosilane, subsequently to depositing any of the silicon-containing materials aforementioned in the above disclosure. A substrate (*e.g.,* 300 mm OD) containing any of the above described silicon containing compounds is placed into the process chamber. During the deposition process, a silicon precursor (*e.g.,* Cl_2SiH_2) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4) and an etchant (*e.g.,* HCl). The flow rate of the dichlorosilane is in a range from about 5 sccm to about 500 sccm, preferably from about 50 sccm to about 200 sccm. The flow rate of the carrier gas is in a range from about 10 slm to about 30 slm. The flow rate of the germanium source is in a range from about 0.1 sccm to about 10 sccm, preferably from about 0.5 sccm to about 5 sccm. The flow rate of the etchant is in a range from about 5 sccm to about 1,000 sccm, preferably from about 30 sccm to about 500 sccm. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 200 Torr, preferably less than about 5 Torr, for example, about 3 Torr. The substrate is heated to a temperature in a range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a second silicon-containing material, namely a silicon germanium film. The etchant removes any deposited amorphous or polycrystalline silicon-germanium materials from any dielectric features upon the surface of the substrate. The process is conducted to form the deposited silicon-germanium material with a thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 10 Å/min and about 100 Å/min, preferably at about 50 Å/min. The germanium concentration is in a range from about 1 at% to about 30 at% of the silicon-germanium material, preferably at about 20 at%. In one example, a deposition process uses silane to deposit a silicon-germanium film. In other examples, silane is substituted with dichlorosilane to any of the previously described embodiments or examples to deposit a second silicon-containing film. In another example, a third silicon-containing layer is deposited using any of the silane based process described herein.

[0059] Therefore, in one embodiment, a silicon-containing laminate film may be deposited in sequential layers of silicon-containing material by altering the silicon precursor between silane and dichlorosilane. In one example, a laminate film of about 2,000 Å is formed by depositing four silicon-containing layers (each of about 500 Å), such that the first and third layers are deposited using dichlorosilane and the second and fourth layers are deposited using silane. In another aspect of a laminate film, the first and third layers are deposited using silane and the second and fourth layers are deposited using dichlorosilane. The thickness of each layer is independent from each other; therefore, a laminate film may have various thicknesses of the silicon-containing layers.

[0060] In one embodiment, dichlorosilane is used to deposit the silicon-containing layer when the previous layer contains surface islands (*e.g.,* contamination or irregularity to film). A process incorporating dichlorosilane may be less sensitive to the surface islands while depositing the silicon-containing material layer over the previous layer. Silicon-containing materials formed during processes that use dichlorosilane as the silicon precursor have a higher or faster horizontal or lateral growth rate relative to silicon-containing materials formed during processes that use silane. In one example, the surface island is covered by a silicon-containing material having a conformal, smooth and consistent surface formed by a deposition process containing dichlorosilane. Subsequently, dichlorosilane is replaced with silane and deposition process is continued to form the silicon-containing layer.

[0061] In another embodiment, the substrate surface may be exposed to ambient conditions, such oxygen or water from the air, between process steps. The ambient exposure is generally endured while shuffling substrates between multiple process chambers during the fabrication of devices. A first silicon-containing layer is deposited on the substrate surface, the substrate is exposed to ambient conditions, and subsequently, a second silicon-containing layer is deposited on the substrate surface. In one aspect, a cap layer is deposited on the first silicon-containing layer before the ambient exposure. The cap layer may be a dielectric material, such as silicon. For example, a silicon-germanium layer is deposited on the substrate surface, a silicon-cap layer is deposited on the silicon-germanium layer, the substrate is exposed to ambient conditions, and subsequently a second-silicon containing layer is deposited on the silicon-cap layer, such as a silicon layer or a silicon-carbon layer.

[0062] Embodiments of the invention provide processes to deposit silicon-containing materials on many substrates and surfaces. Substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon (*e.g.,* Si<100> and Si<111>), silicon oxide, silicon germanium, doped or undoped wafers and patterned or non-patterned wafers. Substrates have a variety of geometries (*e.g.,* round, square and rectangular) and sizes (*e.g.,* 200 mm OD, 300 mm OD). Surfaces or substrates may include wafers, films, layers and materials with dielectric, conductive and barrier properties and include polysilicon, silicon on insulators (SOI), strained and unstrained lattices. Pretreatment processes of surfaces may include a polishing process, an etching process, a reduction process, an oxidation process, a hydroxylation process, an annealing process and a baking process. In one embodiment, wafers are dipped into a 1% HF solution, dried and heated within a hydrogen atmosphere at 800°C.

[0063] In one embodiment, silicon-containing materials include a germanium concentration within a range from about 0 at% to about 95 at%. In another embodiment, a germanium concentration is within a range from about 1 at% to about 30 at%, preferably from about 15 at% to about 30 at%, for example, about 20 at%. Silicon-containing compounds also include a carbon concentration within a range from about 0 at% to about 5 at%. In other aspects, a carbon concentration is within a range from about 200 ppm to about 3 at%, preferably about 1.5 at%.

[0064] The silicon-containing material films of germanium and/or carbon are produced by various processes of the invention and can have consistent, sporadic or graded elemental concentrations. Graded silicon germanium films are disclosed in commonly assigned United States Patent No. 6,770,134 and United States Patent Publication No. 20020174827, which are incorporated herein by reference in their entirety for the purpose of describing methods of depositing graded silicon-containing material or films. In one embodiment, a silicon source and a germanium source (*e.g.,* GeH_4) are used to deposit silicon germanium containing films. In this embodiment, the ratio of silicon source and germanium source can be varied in order to provide control of the elemental concentrations, such as silicon and germanium, while growing graded films. In another embodiment, a silicon source and a carbon source (*e.g.,* CH_3SiH_3) are used to deposit silicon carbon containing films. The ratio of silicon source and carbon source can be varied in order to provide control of the elemental concentration while growing homogenous or graded films. In another embodiment, a silicon source, a germanium source (*e.g.,* GeH_4) and a carbon source (*e.g.,* CH_3SiH_3) are used to deposit silicon germanium carbon containing films. The ratios of silicon, germanium and carbon sources are independently varied in order to provide control of the elemental concentration while growing homogenous or graded films.

[0065] MOSFET devices formed by processes described herein may contain a PMOS component or a NMOS component. The PMOS component, with a p-type channel, has holes that are responsible for channel conduction, while the NMOS component, with a n-type channel, has electrons that are responsible channel conduction. Therefore, for example, a silicon-containing material such as silicon-germanium may be deposited in a recessed area to form a PMOS component. In another example, a silicon-containing film such as silicon-carbon may be deposited in a recessed area to form a NMOS component. Silicon-germanium is used for PMOS application for several reasons. A silicon-germanium material incorporates more boron than silicon alone, thus the junction resistivity may be lowered. Also, the silicon-germanium/silicide layer interface at the substrate surface has a lower Schottky barrier than the silicon/silicide interface.

[0066] Further, a silicon-germanium layer deposited epitaxially on top of a silicon layer has compressive stress inside the film because the lattice constant of silicon-germanium is larger than that of silicon. The compressive stress is transferred in the lateral dimension to create compressive strain in the PMOS channel and to increase mobility of the holes. For NMOS application, silicon-carbon can be used in the recessed areas to create tensile stress in the channel, since the lattice constant of silicon-carbon is smaller than that of silicon. The tensile stress is transferred into the channel and increases the electron mobility. Therefore, in one embodiment, a first silicon-containing layer is formed with a first lattice strain value and a second silicon-containing layer is formed with a second lattice strain value. For example, a silicon-carbon layer with a thickness in a range from about 50 Å to about 200 Å is deposited on a substrate surface and sequentially, a silicon-germanium layer with a thickness in a range from about 150 Å to about 1,000 Å is deposited on the silicon-carbon layer. The silicon-carbon layer may be epitaxially grown and has less strain than the silicon-germanium layer epitaxially grown on the silicon-carbon layer.

[0067] In processes of the invention, silicon-containing material films are grown by chemical vapor deposition (CVD) processes, wherein CVD processes include atomic layer deposition (ALD) processes and/or atomic layer epitaxy (ALE) processes. Chemical vapor deposition includes the use of many techniques, such as plasma-assisted CVD (PA-CVD), atomic layer CVD (ALCVD), organometallic or metalorganic CVD (OMCVD or MOCVD), laser-assisted CVD (LA-CVD), ultraviolet CVD (UV-CVD), hot-wire (HWCVD), reduced-pressure CVD (RP-CVD), ultra-high vacuum CVD (UHV-CVD) and others. In one embodiment, the preferred process of the present invention is to use thermal CVD to epitaxially grow or deposit the silicon-containing material, whereas the silicon-containing material includes silicon (Si), silicon-germanium (SiGe), silicon-carbon (SiC), silicon-germanium-carbon (SiGeC), doped variants thereof or combinations thereof.

[0068] The processes of the invention can be carried out in equipment known in the art of ALE, CVD and ALD. The apparatus brings the sources into contact with a heated substrate on which the silicon-containing material films are grown. The processes can operate at a range of pressures from about 0.1 Torr to about 200 Torr, preferably from about 0.5 Torr to about 50 Torr, and more preferably from about 1 Torr to about 10 Torr. Hardware that can be used to deposit silicon-containing films includes the Epi Centura® system and the Poly Gen® system available from Applied Materials, Inc., located in Santa Clara, California. An ALD apparatus useful during processes for depositing silicon-containing materials herein is described in commonly assigned United States Patent Publication No. 20030079686, filed on December 21, 2001, entitled "Gas Delivery Apparatus and Methods for ALD," and is incorporated herein by reference in entirety for the purpose of describing the apparatus. Other apparatuses include batch, high-temperature furnaces, as known in the art.

Examples

[0069] Example 1: SiGe/Si stack: A substrate, Si<100>, (*e.g.,* 300 mm OD) was employed to investigate selective, monocrystalline film growth by CVD. A dielectric feature existed on the surface of the wafer. The wafer was prepared by subjecting to a 1% HF dip for 45 seconds. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Dichlorosilane (100 sccm) and germane (1% GeH_4 in H_2, 280 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (190 sccm) and diborane (1% in H_2, 150 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for about 5 minutes to form a 500 Å silicon-germanium film with a germanium concentration of about 20 at% and the boron concentration of about 1.0×10^{20} cm^{-3}. The substrate was removed from the process chamber and exposed to the ambient air. The substrate was loaded into a second deposition chamber (Epi Centura® chamber) and heated to 800°C. The substrate was exposed to a process gas containing silane (100 sccm) and hydrogen chloride (250 sccm) for about 10 minutes to selectively deposit a silicon film on the silicon-germanium film.

[0070] Example 2: Graded-SiGe/Si stack: A substrate, Si<100>, (*e.g.*, 300 mm OD) was employed to investigate selective, monocrystalline film growth by CVD. A dielectric feature existed on the surface of the wafer. The wafer was prepared by subjecting to a 1% HF dip for 45 seconds. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A first silicon-germanium film was deposited by directing a hydrogen carrier gas towards the substrate and the source compounds were added to the carrier flow. Dichlorosilane (100 sccm) and germane (1% GeH_4 in H_2, 190 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (160 sccm) and diborane (1% in H_2, 150 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for 2 minutes to form a 100 Å silicon-germanium film with a germanium concentration of 15 at% and the boron concentration of about 5.0×10^{19} cm^{-3}. A second silicon-germanium film was deposited to the first silicon-germanium film to form a graded-silicon-germanium film. Dichlorosilane (100 sccm) and germane (1% GeH_4 in H_2, 350 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (250 sccm) and diborane (1% in H_2, 125 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for about 5 minutes to form a 500 Å silicon-germanium film with a germanium concentration of about 30 at% and the boron concentration of about 1.8×10^{20} cm^{-3}. The substrate was removed from the process chamber and exposed to the ambient air. The substrate was loaded into a second deposition chamber (Epi Centura® chamber) and heated to

800°C. The substrate was exposed to a process gas containing silane (100 sccm) and hydrogen chloride (250 sccm) for about 10 minutes to selectively deposit a silicon film on the silicon-germanium film.

[0071] Example 3: SiC/Si stack: A substrate, Si<100>, (*e.g.,* 300 mm OD) was employed to investigate selective, monocrystalline film growth by CVD. A dielectric feature existed on the surface of the wafer. The wafer was prepared by subjecting to a 1% HF dip for 45 seconds. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Dichlorosilane (100 sccm) and methylsilane (1% CH_3SiH_3 in H_2, 100 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (160 sccm) and diborane (1% in H_2, 150 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for about 5 minutes to form a 500 Å silicon-carbon film with a carbon concentration of about 1.25 at% and the boron concentration of about 1.0×10^{20} cm^{-3}. The substrate was removed from the process chamber and exposed to the ambient air. The substrate was loaded into a second deposition chamber (Epi Centura® chamber) and heated to 800°C. The substrate was exposed to a process gas containing silane (100 sccm) and hydrogen chloride (250 sccm) for about 10 minutes to selectively deposit a silicon film on the silicon-carbon film.

[0072] Example 4: Graded-SiC/Si stack: A substrate, Si<100>, (*e.g.,* 300 mm OD) was employed to investigate selective, monocrystalline film growth by CVD. A dielectric feature existed on the surface of the wafer. The wafer was prepared by subjecting to a 1% HF dip for 45 seconds. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A first silicon-carbon film was deposited by directing a hydrogen carrier gas towards the substrate and the source compounds were added to the carrier flow. Dichlorosilane (100 sccm) and methylsilane (1%

CH_3SiH_3 in H_2, 80 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (160 sccm) and diborane (1% in H_2, 100 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for about 2 minutes to form a 100 Å silicon-germanium film with a carbon concentration of 1.25 at% and the boron concentration of about 5×10^{19} cm^{-3}. A second silicon-carbon film was deposited to the first silicon-carbon film to form a graded silicon-carbon film. Dichlorosilane (100 sccm) and methylsilane (1% CH_3SiH_3 in H_2, 350 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (250 sccm) and diborane (1% in H_2, 150 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for 5 minutes to form a 500 Å silicon-carbon film with a carbon concentration of 1.75 at% and the boron concentration of about 1.8×10^{20} cm^{-3}. The substrate was removed from the process chamber and exposed to the ambient air. The substrate was loaded into a second deposition chamber (Epi Centura® chamber) and heated to 800°C. The substrate was exposed to a process gas containing silane (100 sccm) and hydrogen chloride (250 sccm) for about 10 minutes to selectively deposit a silicon film on the silicon-carbon film.

[0073] Example 5: SiGeC/Si stack: A substrate, Si<100>, (*e.g.,* 300 mm OD) was employed to investigate selective, monocrystalline film growth by CVD. A dielectric feature existed on the surface of the wafer. The wafer was prepared by subjecting to a 1% HF dip for 45 seconds. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Dichlorosilane (100 sccm), germane (1% GeH_4 in H_2, 190 sccm) and methylsilane (1% CH_3SiH_3 in H_2, 100 sccm) were added to the chamber at 3 Torr and 725°C. Also, hydrogen chloride (220 sccm) and diborane (1% in H_2, 150 sccm) were delivered to the chamber. The substrate was maintained at 725°C. Deposition was conducted for about 5 minutes to form a 500 Å silicon-germanium-carbon film with a germanium concentration of about 20 at% a carbon concentration of about 1.5 at% and the boron concentration of about 1.0×10^{20} cm^{-3}. The substrate was removed from the process chamber and exposed to the ambient air. The substrate was loaded into a second deposition chamber (Epi Centura® chamber) and heated to 800°C. The substrate was exposed to a process gas containing silane (100 sccm) and hydrogen chloride (250 sccm) for about 10 minutes to selectively deposit a silicon film on the silicon-germanium-carbon film.

[0074] While the foregoing is directed to embodiments of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. A method for forming a silicon-based material on a substrate, comprising:

exposing a substrate to a first process gas comprising dichlorosilane, a germanium source, a first etchant and a carrier gas to deposit a first silicon-containing layer thereon; and

exposing the substrate to a second process gas comprising silane and a second etchant to deposit a second silicon-containing layer thereon.

2. The method of claim 1, wherein the first process gas is formed by combining:

the dichlorosilane with a flow rate in a range from about 50 sccm to about 200 sccm;

germane with a flow rate in a range from about 0.5 sccm to about 5 sccm;

hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm; and

hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

3. The method of claim 2, wherein the first silicon-containing layer and the second silicon-containing layer are deposited in a process chamber maintained at a pressure within a range from about 1 Torr to about 10 Torr.

4. The method of claim 2, wherein the first silicon-containing layer is selectively deposited on the substrate.

5. The method of claim 4, wherein the second silicon-containing layer is selectively deposited on the first silicon-containing layer.

6. The method of claim 5, wherein the first silicon-containing layer is a recessed layer and the second silicon-containing layer is an elevated layer within a source/drain feature.

7. The method of claim 2, wherein the first silicon-containing layer comprises a graded germanium concentration.

8. The method of claim 2, wherein the first and second process gases each comprise a dopant precursor independently selected from the group consisting of diborane, arsine, phosphine and derivatives thereof.

9. The method of claim 8, wherein the first and second silicon-containing layers have a boron concentration at a range from about 5×10^{19} atoms/cm^3 to about 2×10^{20} atoms/cm^3.

10. The method of claim 8, wherein the first and second silicon-containing layers independently comprise a graded dopant concentration.

11. The method of claim 1, wherein the second process gas is formed by combining:

the silane with a flow rate in a range from about 50 sccm to about 200 sccm; and

hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm.

12. The method of claim 11, wherein the second process gas comprises a second germanium source.

13. The method of claim 12, wherein a germanium concentration of the second silicon-containing layer is larger than the germanium concentration of the first silicon-containing layer.

14. The method of claim 8, wherein a dopant concentration of the second silicon-containing layer is larger than a dopant concentration of the first silicon-containing layer.

15. A method for forming a silicon-based material on a substrate within a process chamber, comprising:

exposing a substrate to a process gas comprising dichlorosilane, methylsilane, hydrogen chloride and hydrogen to deposit a silicon-containing layer thereon.

16. The method of claim 15, wherein the process gas is formed by combining:

the dichlorosilane with a flow rate in a range from about 20 sccm to about 400 sccm;

the methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm;

the hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm; and

the hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

17. The method of claim 16, wherein the process chamber is maintained at a pressure within a range from about 1 Torr to about 10 Torr.

18. The method of claim 17, wherein the silicon-containing layer is selectively deposited on the substrate.

19. The method of claim 18, wherein the silicon-containing layer comprises a graded carbon concentration.

20. The method of claim 16, wherein the process gas further comprises a dopant precursor with a flow rate in a range from about 0.2 sccm to about 3 sccm.

21. The method of claim 20, wherein the dopant precursor is selected from the group consisting of diborane, arsine, phosphine and derivatives thereof.

22. The method of claim 21, wherein the silicon-containing layer comprises a graded dopant concentration.

23. A method for forming a silicon-based material on a substrate within a process chamber, comprising:

exposing a substrate to a process gas comprising silane, methylsilane, hydrogen chloride and hydrogen to deposit a silicon-containing layer thereon.

24. The method of claim 23, wherein the process gas is formed by combining:

the silane with a flow rate in a range from about 20 sccm to about 400 sccm;

the methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm;

the hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm; and

the hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

25. The method of claim 24, wherein the process chamber is maintained at a temperature within a range from about 650°C to about 750°C.

26. The method of claim 25, wherein the process chamber is maintained at a pressure within a range from about 1 Torr to about 10 Torr.

27. The method of claim 24, wherein the first silicon-containing layer comprises a graded carbon concentration.

28. The method of claim 24, wherein the process gas further comprises a dopant precursor with a flow rate in a range from about 0.2 sccm to about 10 sccm.

29. The method of claim 28, wherein the dopant precursor is selected from the group consisting of diborane, arsine, phosphine and derivatives thereof.

30. The method of claim 29, wherein the silicon-containing layer comprises a graded dopant concentration.

31. The method of claim 27, wherein the silicon-containing layer is selectively deposited on the substrate.

32. A method for forming a silicon-based material on a substrate within a process chamber, comprising:

exposing a substrate to a process gas comprising silane, germane, methylsilane, hydrogen chloride and hydrogen to deposit a silicon-containing layer thereon.

33. The method of claim of claim 32, wherein the process gas is formed by combining:

the silane with a flow rate in a range from about 50 sccm to about 200 sccm;

the germane with a flow rate in a range from about 0.5 sccm to about 5 sccm;

the methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm;

the hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm; and

the hydrogen with a flow in a range from about 10 slm to about 30 slm.

34. The method of claim of claim 33, wherein the silicon-containing layer is deposited with a composition comprising:

silicon at a concentration of about 50 at% or more;
carbon at a concentration of about 2 at% or less; and
germanium at a concentration in a range from about 15 at% to about 30 at%.

35. The method of claim 34, wherein the process chamber is maintained at a temperature within a range from about 550°C to about 750°C.

36. The method of claim 35, wherein the process chamber is maintained at a pressure within a range from about 1 Torr to about 10 Torr.

37. The method of claim 34, wherein the silicon-containing layer comprises a graded germanium concentration.

38. The method of claim 34, wherein the silicon-containing layer comprises a graded carbon concentration.

39. The method of claim 34, wherein the process gas further comprises a dopant precursor with a flow rate in a range from about 0.2 sccm to about 3 sccm.

40. The method of claim 39, wherein the dopant precursor is selected from the group consisting of diborane, arsine, phosphine and derivatives thereof.

41. The method of claim 33, wherein the silicon-containing layer is selectively deposited on the substrate.

42. The method of claim 41, wherein an additional silicon-containing layer is selectively deposited on the silicon-containing layer.

43. A method for forming a silicon-based material on a substrate within a process chamber, comprising:

exposing a substrate to a process gas to deposit a silicon-containing layer thereon, wherein the silicon-containing layer has interstitial sites within a crystalline lattice and contains about 3 at% or less of carbon within the interstitial sites; and

annealing the silicon-containing layer to incorporate at least a portion of the carbon within substitutional sites of the crystalline lattice.

44. The method of claim 43, wherein the process gas is formed by combining:

dichlorosilane with a flow rate in a range from about 20 sccm to about 400 sccm;

methylsilane with a flow rate in a range from about 0.3 sccm to about 5 sccm;

hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm; and

hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

45. The method of claim 44, wherein the process chamber is maintained at a temperature within a range from about 750°C to about 850°C.

46. The method of claim 45, wherein the process chamber is maintained at a pressure within a range from about 1 Torr to about 10 Torr.

47. The method of claim 44, wherein the silicon-containing layer comprises a graded carbon concentration.

48. The method of claim 47, wherein the silicon-containing layer is selectively deposited on the substrate.

49. A method for forming a silicon-based material on a substrate, comprising:

depositing a first silicon-containing layer on a substrate;

depositing a second silicon-containing layer on the first silicon-containing layer; and depositing a third silicon-containing layer on the second silicon-containing layer, wherein:

the first silicon-containing layer comprises about 25 at% or less of germanium;

the second silicon-containing layer comprises about 25 at% or more of germanium; and

the third silicon-containing layer comprises about 5 at% or less of germanium.

50. The method of claim 49, further comprising:

the first silicon-containing layer has a germanium concentration within a range from about 15 at% to about 25 at%;

the second silicon-containing layer has a germanium concentration within a range from about 25 at% to about 35 at%; and

the third silicon-containing layer has a germanium concentration up to about 5 at%.

51. The method of claim 49, wherein the first silicon-containing layer is selectively deposited on the substrate.

52. The method of claim 51, wherein the second silicon-containing layer is selectively deposited on the first silicon-containing layer.

53. The method of claim 52, wherein the third silicon-containing layer is selectively deposited on the second silicon-containing layer.

54. The method of claim 53, wherein the first, second or third silicon-containing layers are deposited in a process chamber maintained at a pressure within a range from about 1 Torr to about 10 Torr.

55. The method of claim 49, wherein the first silicon-containing layer has a germanium concentration within a range from about 15 at% to about 25 at%.

56. The method of claim 55, wherein the first silicon-containing layer has a thickness within a range from about 40 Å to about 100 Å.

57. The method of claim 56, wherein the first silicon-containing layer has a boron concentration within a range from about 5×10^{19} atoms/cm^3 to about 1×10^{20} atoms/cm^3.

58. The method of claim 49, wherein the second silicon-containing layer has a germanium concentration within a range from about 25 at% to about 35 at%.

59. The method of claim 58, wherein the second silicon-containing layer has a thickness within a range from about 200 Å to about 1,000 Å.

60. The method of claim 59, wherein the second silicon-containing layer has a boron concentration within a range from about 1×10^{20} atoms/cm^3 to about 2×10^{20} atoms/cm^3.

61. The method of claim 58, wherein the third silicon-containing layer is free of germanium.

62. The method of claim 58, wherein the third silicon-containing layer has a germanium concentration of about 5 at% or less.

63. The method of claim 49, wherein depositing the first silicon-containing layer comprises exposing the substrate to a first process gas formed by combining:

dichlorosilane with a flow rate in a range from about 50 sccm to about 200 sccm;

germane with a flow rate in a range from about 0.5 sccm to about 5 sccm;

hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm;

a dopant precursor with a flow rate in a range from about 0.2 sccm to about 3 sccm; and

hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

64. The method of claim 49, wherein depositing the second silicon-containing layer comprises exposing the substrate to a second process gas formed by combining:

dichlorosilane with a flow rate in a range from about 50 sccm to about 400 sccm;

germane with a flow rate in a range from about 0.5 sccm to about 20 sccm;

hydrogen chloride with a flow rate in a range from about 30 sccm to about 700 sccm;

a dopant precursor with a flow rate in a range from about 0.2 sccm to about 6 sccm; and

hydrogen with a flow rate in a range from about 10 slm to about 30 slm.

65. The method of claim 49, wherein depositing the third silicon-containing layer comprises exposing the substrate to a third process gas is formed by combining:

silane with a flow rate in a range from about 50 sccm to about 200 sccm; and

hydrogen chloride with a flow rate in a range from about 30 sccm to about 500 sccm.

66. A method for depositing a silicon-containing material on a substrate, comprising:

depositing a first silicon-containing layer comprising a first germanium concentration of about 15 at% or more on the substrate;

depositing a second silicon-containing layer comprising a second germanium concentration of about 15 at% or less on the first silicon-containing layer;

exposing the substrate to air to form a native oxide layer thereon;

removing the native oxide layer to expose the second silicon-containing layer; and

depositing a third silicon-containing layer on the second silicon-containing layer.

67. The method of claim 66, wherein the first and second silicon-containing layers are independently deposited by a selective deposition process.

68. The method of claim 67, wherein a MOSFET spacer formation is deposited after the second silicon-containing layer and before the third silicon-containing layer.

69. A method for depositing a silicon-containing material on a substrate, comprising:

depositing a first silicon-containing layer containing a first lattice strain epitaxially on the substrate; and

depositing a second silicon-containing layer containing a second lattice strain epitaxially on the first silicon-containing layer, wherein the second lattice strain is greater than the first lattice strain.

70. The method of claim 69, wherein the first and second silicon-containing layers each independently comprise a material selected from the group consisting of silicon germanium, silicon carbon, silicon germanium carbon, dopants, derivatives thereof and combinations thereof.

71. The method of claim 70, wherein the first silicon-containing layer has a first thickness in a range from about 50 Å to about 200 Å and the second silicon-

containing layer has a second thickness in a range from about 150 Å to about 1,000 Å.

72. The method of claim 69, wherein the first and second silicon-containing layers are independently deposited by a selective deposition process.

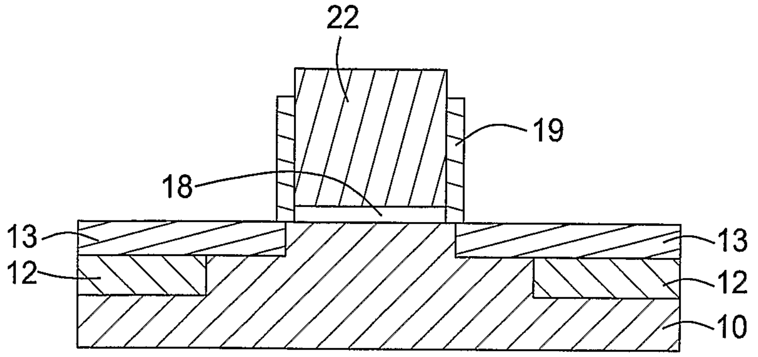


FIG. 1A

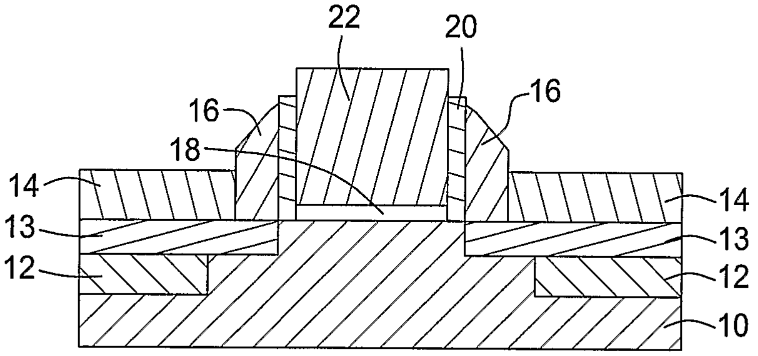


FIG. 1B

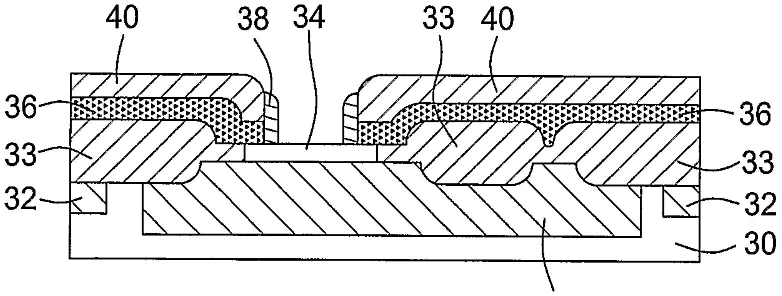


FIG. 1C

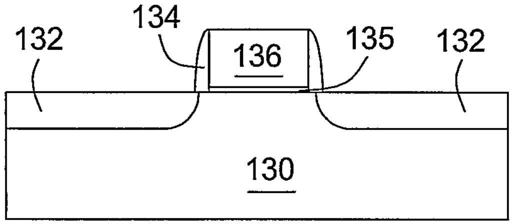


FIG. 2A

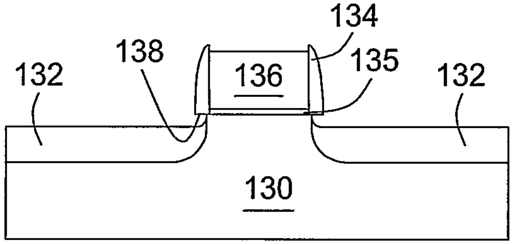


FIG. 2B

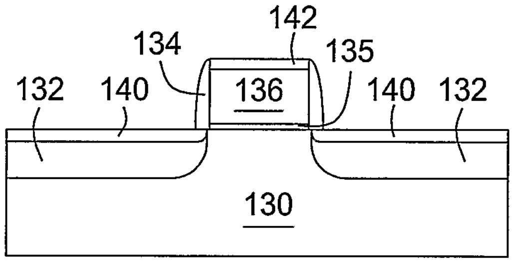


FIG. 2C

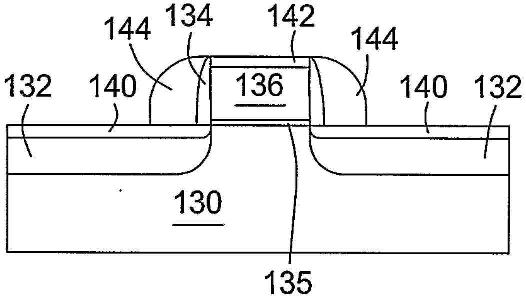


FIG. 2D

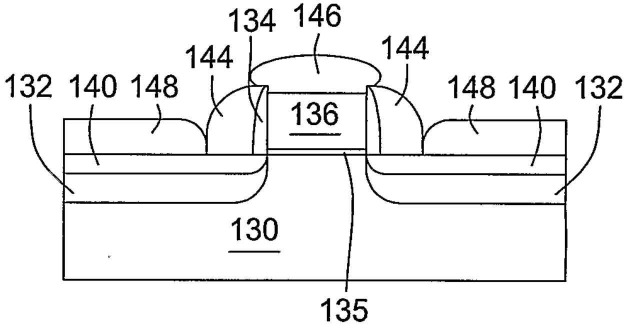


FIG. 2E

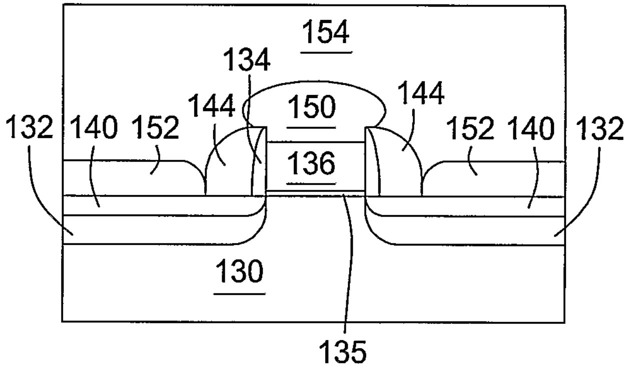


FIG. 2F