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(54) Title: ULTRA WIDEBAND TRANSCEIVER ARCHITECTURE AND METHOD

(57) Abstract: In the technology known today, UWB transceiver power consumption is not efficient and too high. We have solved this problem. In our patent we have presented our innovationist UWB transceiver circuit, which could be used for preamble based OFDM or pilot based OFDM reception. In IEEE P802.15-03/268r3 it is reported that UWB OFDM receiver power consumption at 480Mbits/sec, when implemented using traditional digital method, is 323mwatts for 130nm, and 236mwatts for 90nm. We have found that implementation of the same receiver using our new innovationist OFDM receiver, working at 480Mhz, consumes about 40mwatts. It is clear, in terms of power consumptions, that our OFDM receiver implementation is 8 times lower than the lowest power consumption known today by OFDM receiver circuit.

Ultra Wideband transceiver architecture and method

The theme of our patent is an ultra low power; ultra wide band transceiver.

A new and innovationist ultra wide band transceiver ("our UWB transceiver"), is described in this patent application.

Our UWB transceiver is based on an OFDM modulation, we first describe the OFDM receiver and continue with the UWB OFDM transmitter.

OFDM receiver circuit is usually related to a communication field, where it is used to receive and decode a transmitted data.

OFDM receiver circuit gets at its input OFDM modulated signals, and performs all necessary tasks, in order to decode the received data.

OFDM signal comprised of multiple orthogonal carrier (103a-105a), in which each one carries different data symbol. The summation of all carriers symbols comprises the data.

To perform the receiving operation, an OFDM receiver must first perform detection, synchronization, parameter and channel estimation, then, a Fast Fourier Transform (FFT) is applied, and then, equalization is performed, and the last stage, is the de-interleaving and the error correction.

All tasks above require complicated computational operations, such as additions, multiplications. Therefore, if implemented in a digital way, as it is with the current known technology, a significant high power is consumed by the receiver.

Our OFDM receiver is built and designed to work with discrete time analog signals, based on extremely low power additions, multiplications operations, and therefore achieves significant power reduction, compared to it's digital counter implementation.

Technical Field of the invention

Our UWB transceiver receiver circuit, relates to the field of communication using discrete time analog signal processing, where discrete analog signals are used instead of their counter digital samples.

Our UWB transceiver receiver circuit could be used in transceiver implementation and applications such as: WiMax, Mobile TV (DVBH- TDMB), , etc.

The result of using our UWB transceiver circuit is significant power reduction.

Background Art

Today's most known communication standards use the OFDM modulation scheme, to send and receive information over the communication channel. OFDM method is well understood and suitable for many applications, wired and wireless. ADSL for example, uses an OFDM to transmit internet information to the end user. OFDM, is also used for many Mobile TV standards, such as DVBH, T-DMB. Also, OFDM is penetrating to almost all standards for wireless application, such as WiMax, WiFi , home network, Ultra Wide Band, etc.

In Figure 1a, OFDM signal (100a), for one OFDM symbol, is described. It is comprised of two parts - the cyclic prefix (101a), and the OFDM cycles (102a).
As shown, the OFDM signal, is a summation of many sinusoidal waveforms, each one carries, in this example, one bit. The first sinusoidal carries +1(103a). The second carries -1 when it is 180 degrees inverted (104a). The third, also carries +1(105a).

In figure 1b , Another method for OFDM signal is described, in which the OFDM symbol, is comprised of zero prefix (101b) and OFDM cycles (102b). As before the OFDM signal of figure 1b, carries the same information bits.
The above signal, shown in Figures 1a and 1b, is transmitted through communication channels like wired, wireless, or optical. And therefore the signal is distorted where each of the sinusoidal waveforms, gets it own phase shift and amplitude.
It is therefore, the purpose of the OFDM receiver to mitigate all impairments and to decode the transmitted data stream correctly.
OFDM receivers, in today's known technology, are implemented in a Digital Signal Processing (DSP) method.

In figure 2, general DSP system is depicted, in which the analog signal source (200-201), is first filtered by anti-aliasing filter (202), the signal is sampled and hold (203), and passed to the Analog to Digital converter (ADC) (204). The ADC quantize the analog signal S(n) (204), and passes the stream of digitized samples Sq(n) (206) into

the digital processing unit (207), which could be implemented by Instruction Set Architecture (ISA) DSP, or, by Application Specific Integrated Circuit (ASIC) DSP. The ISA DSP gives flexibility but charges high power, on the other hand, ASIC DSP gives lower power but no flexibility.
In general, in mobile application, ASIC DSP is used, but still, although designed for low power, ASIC DSP power is too high and shortening battery life.
We will now go into more details with respect to receiver implementation.

In figure 3, DSP implementation of a receiver is shown. The first stage is a tuner (301) connected to antenna (300). The tuner translates the high frequency signal to some base band signal, and performs some pre-processing filtering.
The complex signal (I&Q)(302) is then, "sampled & hold" (S/H) (303-304). The output from S/H is digitized by ADC's (306-307) and sent to the base band receiver (308), for decoding the received signal data.
The base band receiver needs to perform many computational operations, such as detection, synchronization, parameter estimation etc, to reliably decode the received data.

In figure 4, an OFDM receiver, based on DSP method, is described. Similar to figure 3, the first stages in the chain are, the antenna (400), tuner (401) for converting the Radio Frequency (RF) signal to base band, S/H units (402-403), and ADC's (404-405). The base band processing is described in more details, to show the complexity involved with OFDM reception (see US 7075949 B1).
The first block, OFDM symbol synchronization (410), is responsible of detecting the OFDM packet and finding the starting point, in time, of the OFDM symbol at the end of the cyclic/zero prefix (101a, 101b). The synch block sends a mark to a memory buffer (411), which stores the OFDM symbol (100a, 100b), the OFDM symbol is then processed by the Fast Fourier Transform (FFT) (413), which extracts the amplitudes values from the different OFDM carriers. The FFT is a complex operation that involves many additions/multiplications memory and control operations.
Equation (1) shows the number of real multiplications per one FFT block. Equation (2) shows the number of real addition per one FFT block :

Eq(1) Number of Multiplications $= 2 \bullet N \bullet \log_2(N)$

Eq(2) Number of Additions $= 2 \bullet N \bullet \log_2(N)$

For large N , and short time OFDM symbols, according the above equations, implies too many operation per second, and therefore too high power, resulted shortening buttery life, which is not suitable for mobile devices.

Carrier frequency correction (407, 409) and timing correction (406,408) are operated in parallel which involves too many mathematical operations per second, and hence power consumption is increased.

The next block in the receive chain, is the equalizer (EQU)(420), which responsible on the amplitude and phase correction, of the OFDM carriers. Equalization, as well, requires many multiplications/addition per second.

Equalizer output is further corrected for residual phase (422), if required (depended on the standard).

The OFDM corrected phase carriers, are then processed by the de-mapping (423), for converting the carriers symbol data into bits, and also processed by de-interleaving (424) and error correction (425).

In high rate communication, the above requires too many mathematical operations per second and hence power consumption is increased.

In parallel to the receive chain, which process the samples sequentially, parameter estimation blocks perform, carrier frequency/sampling timing (412), phase, channel and noise estimation (415-417), and equalization coefficients calculation (416-418) .

To understand the complexity involved with above implementation, we will now demonstrate UWB example working at 480Mbits/sec, which requires:

- Tuner
- 2 ADC's 5-6 bits resolution, operated at 1024Mhz, are required – each consumes about 40mwttas
- Input timing correction (406) – requires 7 real multiplications per sample, or 7.168GMAC's/sec
- Carrier correction 4 MAC's/sample at 512Mhz, or 2.2GMAC`s/sec
- FFT about 5.73GMAC`s/sec
- Equalization about 1.6GMAC`s/sec

- Error correction (Viterbi) about 92GADD's/sec (branch metric & state metric for k=7 Viterbi decoder)

According to **IEEE P802.15-03/268r3**, the UWB component list at 480Gbits/sec, is summed up to 323mwatts for 130nm process and 236mwatts for 90nm process.
The reason for that is inherently due to the high power involved with digital implementation of the signal processing blocks, timing correction, frequency correction, FFT, equalization, Viterbi, and due to the high sample rate. Therefore, the above method, is not suitable for mobile devices.
Also, in some cases, (i.e. 802.15.3c), an even higher rate UWB (3Gbits/sec) communication standard, it is even impractical for implementation, due to the higher power (about 1.5watts with current known technology)
It is therefore, the purpose of this invention to describe a new and extremely low power consumption OFDM receiver circuit.

Detailed description of our Invention

In this section, we will cover the principals of our UWB transceiver circuit we start with the description of our innovationist OFDM receiver circuit ("our OFDM receiver")
Our OFDM receiver circuit works in the discrete time analog signal processing, in which, rather than working on digitized samples, work is done on analog samples.
By doing that:

- The need for ADC is eliminated.
- The amount of gates is reduced and hence power.
- The signal voltage swing is reduced by 10 and therefore the power by 100.

Figure 5, shows a possible implementation of the invention. The identical parts to the prior art are the antenna (500), tuner (501) and the S/H units (502,503).
However, we see a huge difference compared to the prior art shown in **figure 4**.

Our OFDM receiver, processes the analog samples at the output of the S/H units in an analog way, by representing the input samples at the output of the S/H units (502-503), using some physical parameter, such as current or voltage.
All processing blocks, are implemented using analog circuit implementation of the required function.

Our signal chain, shown in **figure 5**, is innovationist. And in relation to the chain, shown in **figure 4**, these changes are demonstrated:

- Work is done on analog samples – no ADC's are required.
- Sampling timing correction, in **figure 4**, is done by using digital re-sampling, here it is done by generating sampling clock (504) which is connected to the S/H units.

Other signal chain elements are, in terms of functionally, the same. The input buffer that collects the samples, which represents, at least, one OFDM symbol, is stored in a dual buffer **analog memory** (509), while one buffer is connected to the input samples stream, the other feeds the Fast Fourier Transform (FFT) (510), which is also implemented using the discrete time analog signal processing. FFT output is then passed to the EQU (519), phase correction (520) and de-mapping (521).
All the above are implemented using analog multipliers and addition circuits, in our other patent applications which ***"Right of Priority"*** is requested in this applicition.
The de-mapping (521) output, is then passed to the de-interleaver (522) and to the Forward Error Correction block(FEC) (523). The de-interlever is implemented using analog memory in case of soft outputs, at the de-mapper (521), or, digitally for hard decision case.
In parallel to the above signal chain, there are some blocks responsible of parameter estimation and EQU coefficients calculation.
Usually the parameter estimation process, is based on the FFT output pilot data (511), but in some standards (DVBH, T-DMB), some of the parameters are estimated using the time domain signal (511a).
We will now cover the method of implementing each of the algorithms, shown in **figure 5**.

In figure 6, we see a functional block diagram of eight points FFT algorithm (we used eight points for simplicity). The input (601) is fed into three stages of butterflies (603-605), as the FFT compute the frequency content of the input (601), and the FFT output is presented (606).
As shown, one butterfly (602) , includes one complex multiplication and two additions.

Figure 7, shows an example of implementation extremely low power multiplier and addition circuits, in which currents are used to represent the samples values.
Although, a current mode multiplier and addition circuits, are shown in **figure 7**, and voltage mode circuit could be used as well.

Figure 7a, represents the multiplication symbols with inputs x & y (716, 717) and multiplication output Z (718).

Figure 7b, describes one possible implementation of the multiplier, where one input (butterfly input) is differential current (714,715) , and the second (twiddle factors) are the VREF pins (702).
Multiplication output is differential current (712,713).
The multiplier shown in this figure is implemented using Floating Gate Metal Oxide Semi-conductor (FG-MOS) for offset compensation, and hence, higher multiplier accuracy.
This multiplier is fully described in our **"Current Mode Micro Power Multiplier with floating gate offset cancellation"** - Our patent application No. 187075, which ***"Right of Priority"*** is requested in this applicition.
The summation circuit, in cases of currents, is simply implemented using current junction as shown in **figure 7d**, where negative currents are connected to the negative node of differential current representation, and positive currents to the positive node.

Figure 7c, represents the addition symbol with inputs x & y (720, 721) and the addition output z (722).
In general, when analog processing is used, significant power reduction is achieved.
In **IEEE 802.15-03/343r**, it is reported that 128 points FFT for UWB, consumes about 50mwatts. Using the multiplication mentioned in figure 7b, the power of the

128 points FFT is reduced to 1mwatts, 50 times better, when, still, it is functioning with the same accuracy.

Figure 8, describes our OFDM receiver, where all blocks responsible for parameter estimation - such as sampling timing deviation, carrier offset deviation, channel estimation, and residual phase estimation - operate using discrete time analog signal processing, in one parameter block estimation (813).
The parameter estimation block, operates with addition, subtraction, multiplication and division for the estimation process, as was described above. These operations could be implemented using similar analog circuits.
But for greater flexibility the parameter estimation block of **figure 8** (813), is replaced by a digital signal processor.

In figure 9, we see our OFDM receiver circuit, in which the parameter estimation block (913) is implemented using the traditional signal processing method.
The input is taken form the time domain samples (910) or frequency domain samples (912).
The inputs (910,912) are first converted to their digitized samples, by the analog to digital converter (914), and last, processed by ISA DSP or ASIC DSP, to reflect the value of required parameters.
The motivation of using the receiver of **figure 9** , is gaining some degree of flexibility, to support many modes or communication standards.
In some cases, parameter estimation process is done in low frequency, hence, power is not high when done digitally, therefore, for this case the receiver of **figure 9** will be suitable.
Next we show a description of our innovationist OFDM transmitter circuit.

Figure 3a, describes our invention, which presents the same analog signals to the transmit antenna (312a). Our transmitter is divided into three parts.
The first, is the bit processing, built of data bit source (300a-301a), bit processing (302a) which performs the forward error encoding interleaving, the pilot insertion (303) and the mapping module (304).

The second, is the signal processing block, built of the DAC array (306a-307a), analog IFFT (308a), Cyclic/Zero prefix add (309a) and analog pulse shaping filter (310a).

We emphasis that the DAC array, works on the OFDM symbol rate, and therefore decreases the power consumption. Moreover, when the DAC array interfaces an analog IFFT block based on current mode processing.

Brief Description of the figures

Figure 1: describes OFDM symbol structure.
Figure 2: describes general digital signal processing system block diagram.
Figure 3: describes receiver implementation block diagram based on digital signal processing method.
Figure 3a: describes OFDM transmitter implementation block.
Figure 4: describes OFDM receiver implementation using digital signal processing.
Figure 5: describes ultra low power, discrete time analog signal processing based,.OFDM receiver.
Figure 6: describes eight points Fast Fourier Transform (FFT) flow/block diagram.
Figure 7: describes Addition and multiplication symbols with low power circuit implementation.
Figure 8: describes ultra low power OFDM receiver – with analog processing for parameters estimations/calculations.
Figure 9: describes ultra low power OFDM receiver – with Digital siganl Processing (DSP) for parameters estimations/calculations.

Claims

1. Our OFDM receiver circuit comprised of:
    a. Analog OFDM signal source.
    b. "Sample and hold" unit.
    c. Base band processor, based on discrete time analog signal processing.
2. Also, our OFDM receiver circuit comprised of :
    a. Tuner for pre-processing the RF signal.
    b. "Sample and hold" units for the I & Q.
    c. Base band processing unit for decoding the received data.
3. Our OFDM receiver circuits as in claims 1 & 2, in which the base band processing unit is comprised of:
    a. A synchronization circuit – for the detection and synchronization of the OFDM symbol.
    b. Sampling time correction clock, connected to the "sample and hold" units.
    c. Carrier deviation correction unit.
    d. A memory element to store the input data.
    e. A transform element that transform the input.
    f. Equalization unit.
    g. Phase correction.
    h. De-mapping unit.
    i. One or more De-interleaving.
    j. Forward error correction unit.
    k. Parameter estimation block.
4. Our OFDM receiver of claim 3, in which the signal chain blocks (a-k) are operating in the discrete time analog signal processing domain.
5. Our OFDM receiver of claim 4, in which, the multiplier used for the analog processing is
    a. Extremely low power, based on current mode processing.
    b. Operating in the sub-threshold of transistor region of operation.
    c. Based on FG-MOS, to allow compensation for process variations.

6. Our OFDM receiver of claim 3, in which the parameter estimation block is implemented using discrete time analog signal processing.
7. Our OFDM receiver of claim 6, in which, the parameter estimation block is implemented using:
    a. Extremely low power multiplier, division, addition and subtraction circuits, based on current mode processing.
    b. Signal processing blocks, operating in the sub-threshold region of transistor operation.
    c. FG-MOS transistors, to allow compensation for process variations.
8. Our OFDM receiver of claim 3, in which the parameter estimation block is implemented using Digital Signal Processing.
9. Our OFDM receiver of claim 8, in which the Digital Signal Processing comprised of:
    a. An analog to digital converter
    b. A digital signal processor based on ASIC DSP or ISA DSP methods.

Figures

Figure 1: OFDM Symbol

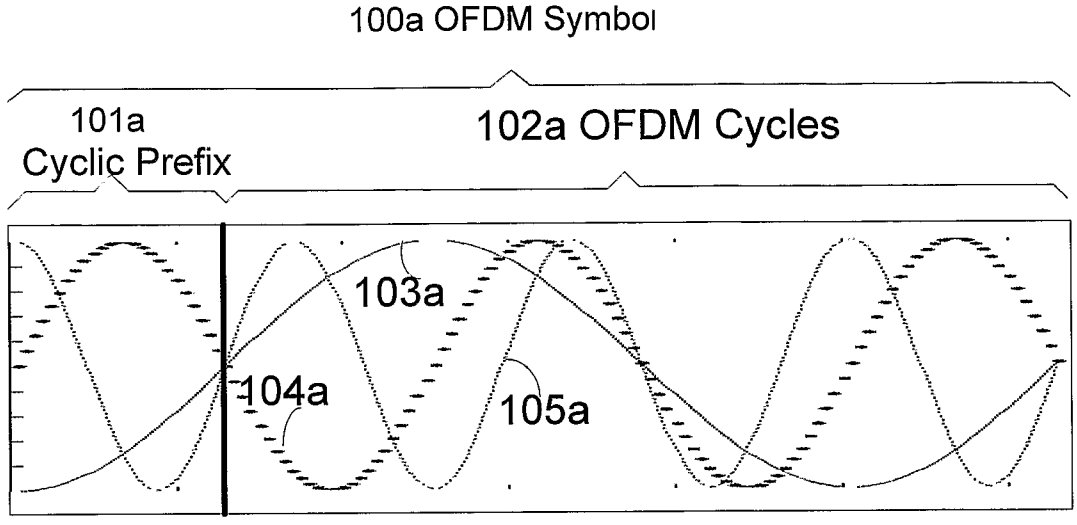

Figure 1a :OFDM Symbol with Cyclic prefix

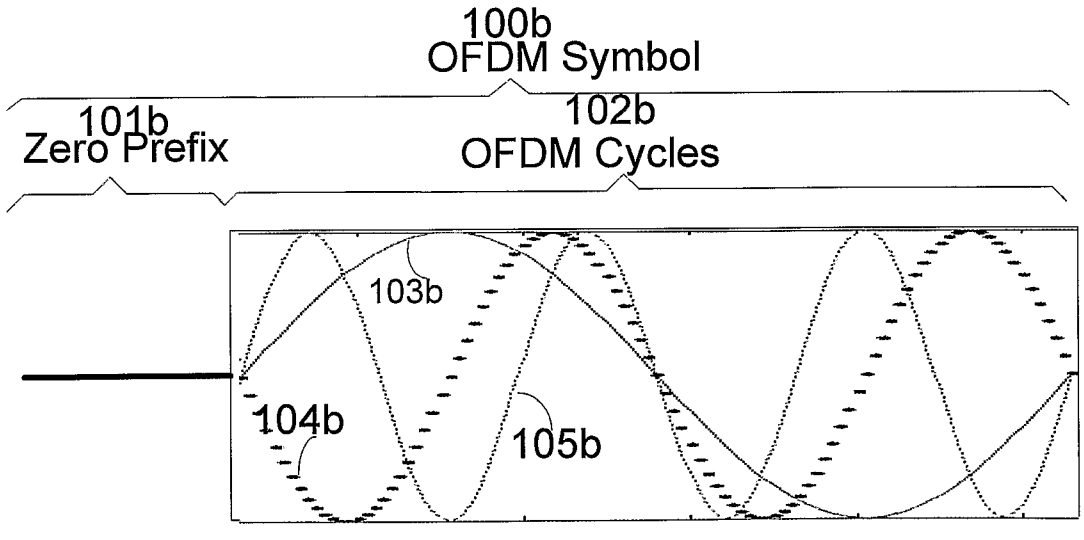

Figure 1b :OFDM Symbol with Zero prefix

Figure 2: Traditional Digital Signal Processing (DSP) system

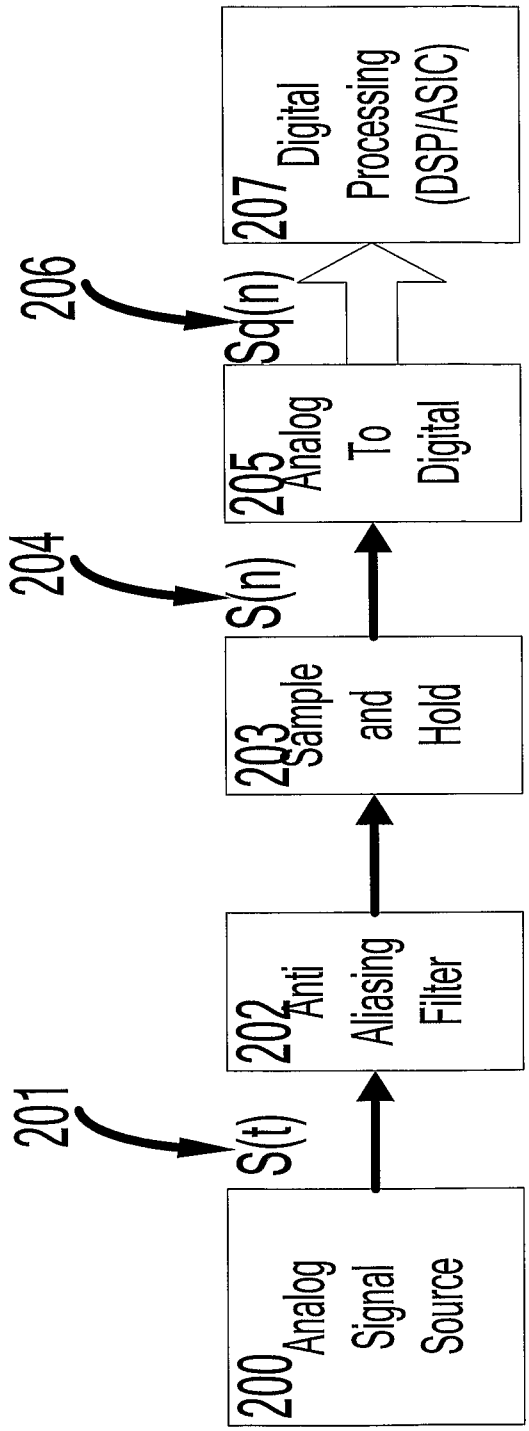

Figure 3: Digital Signal Processing based, receiver implementation high level block diagram

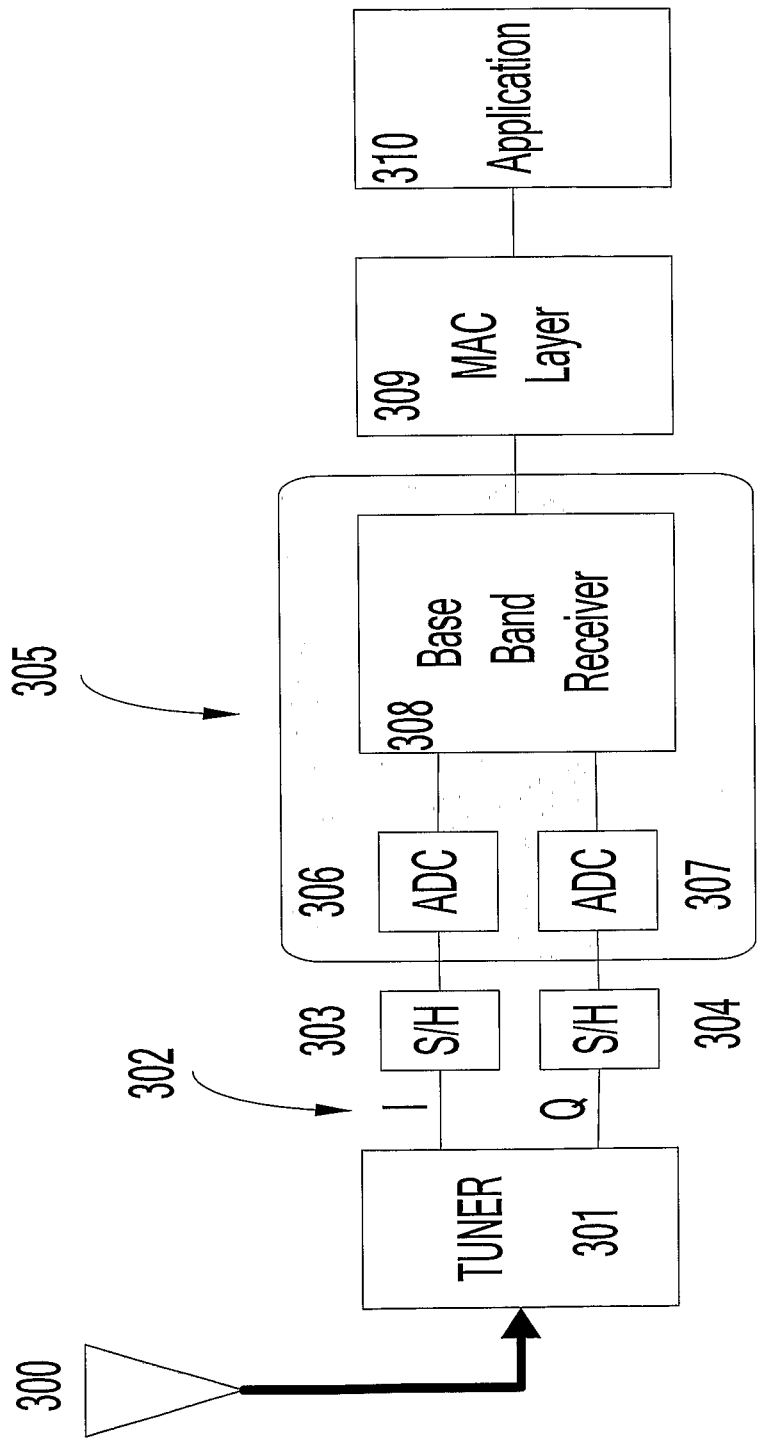

Figure 3a: New, low power, implementation of OFDM transmitter

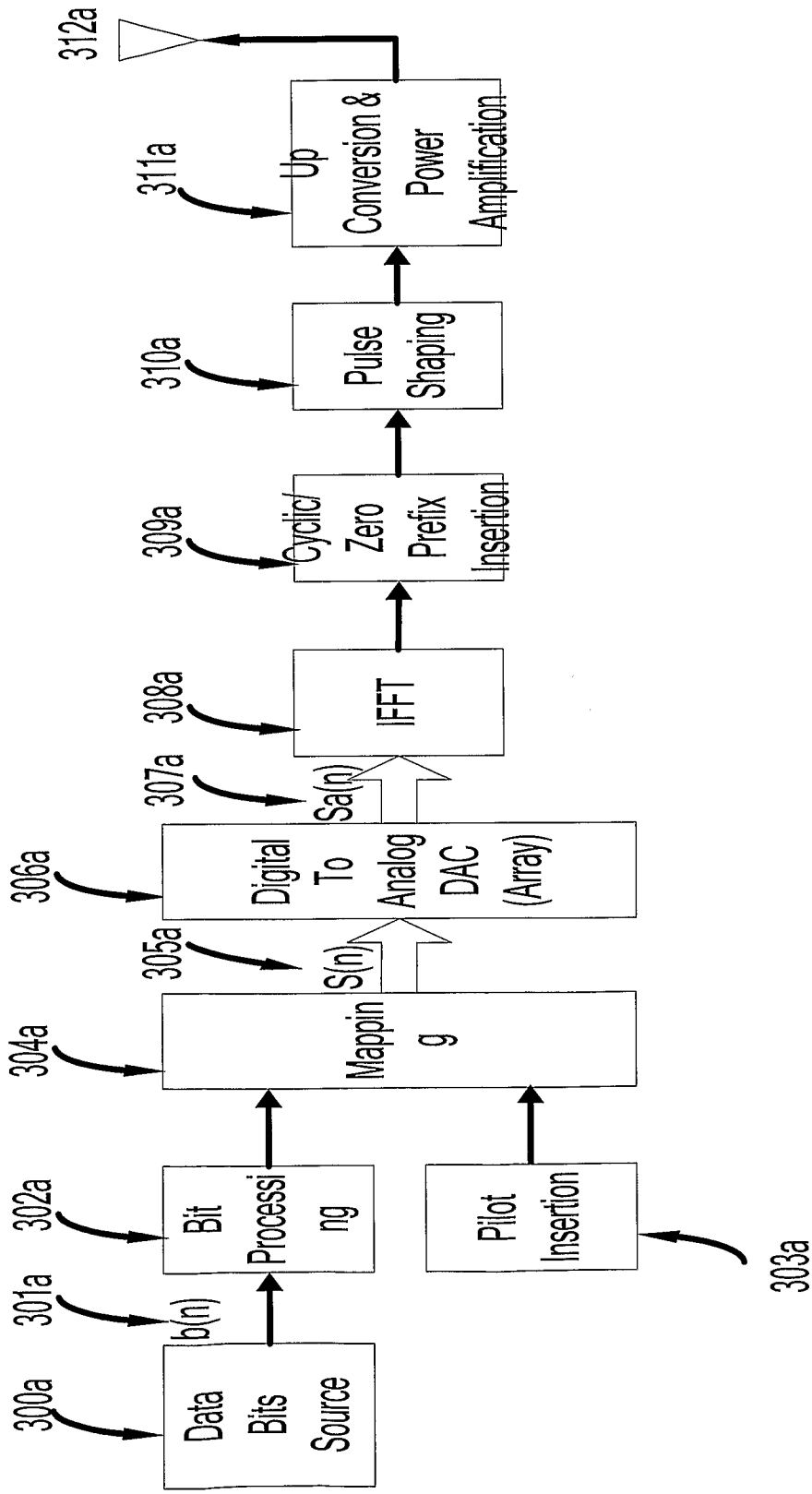

Figure 4: Digital Signal Processing (DSP) based OFDM receiver (prior art)

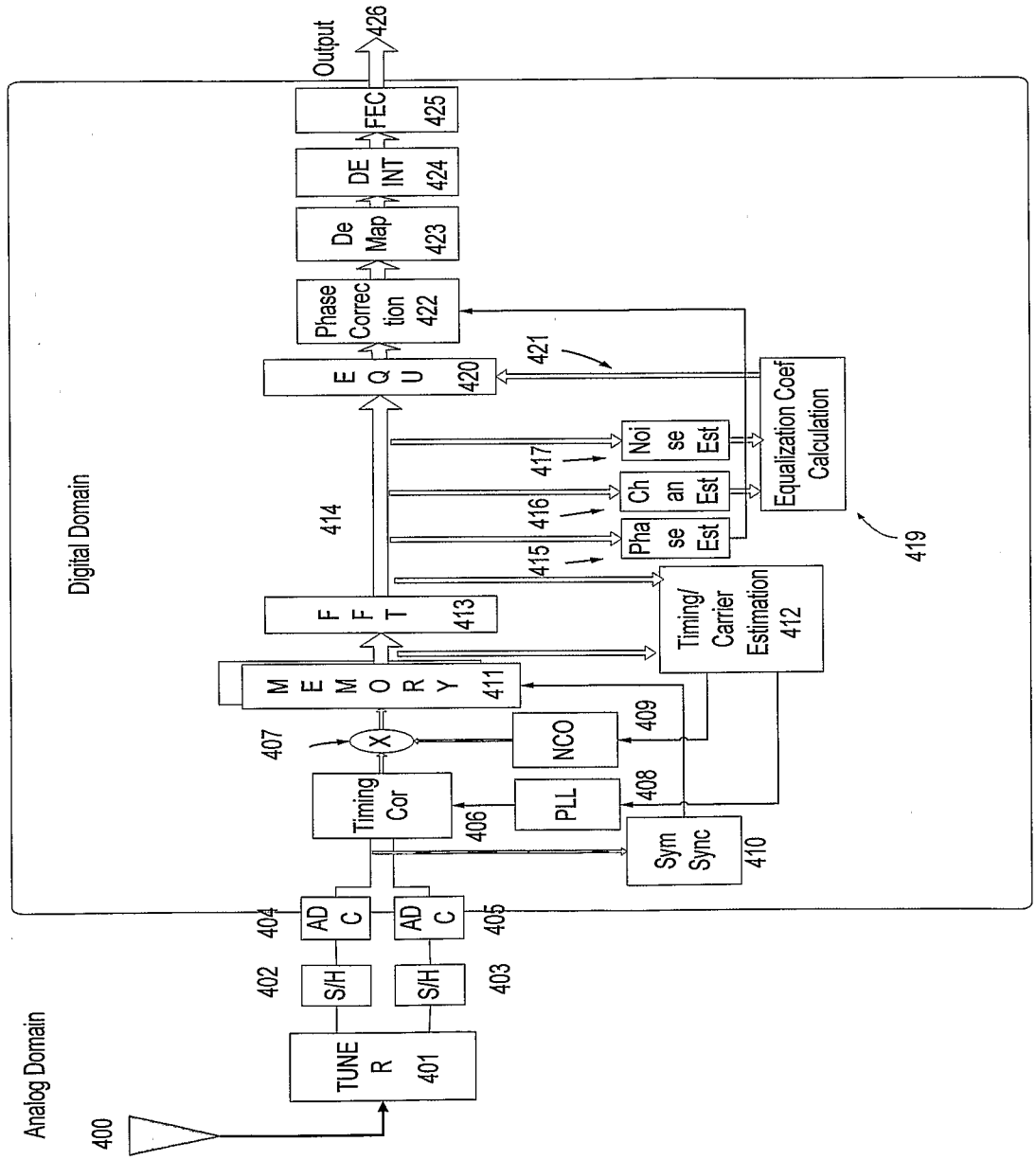

Figure 5: Ultra low power, discrete time analog signal processing based, OFDM receiver

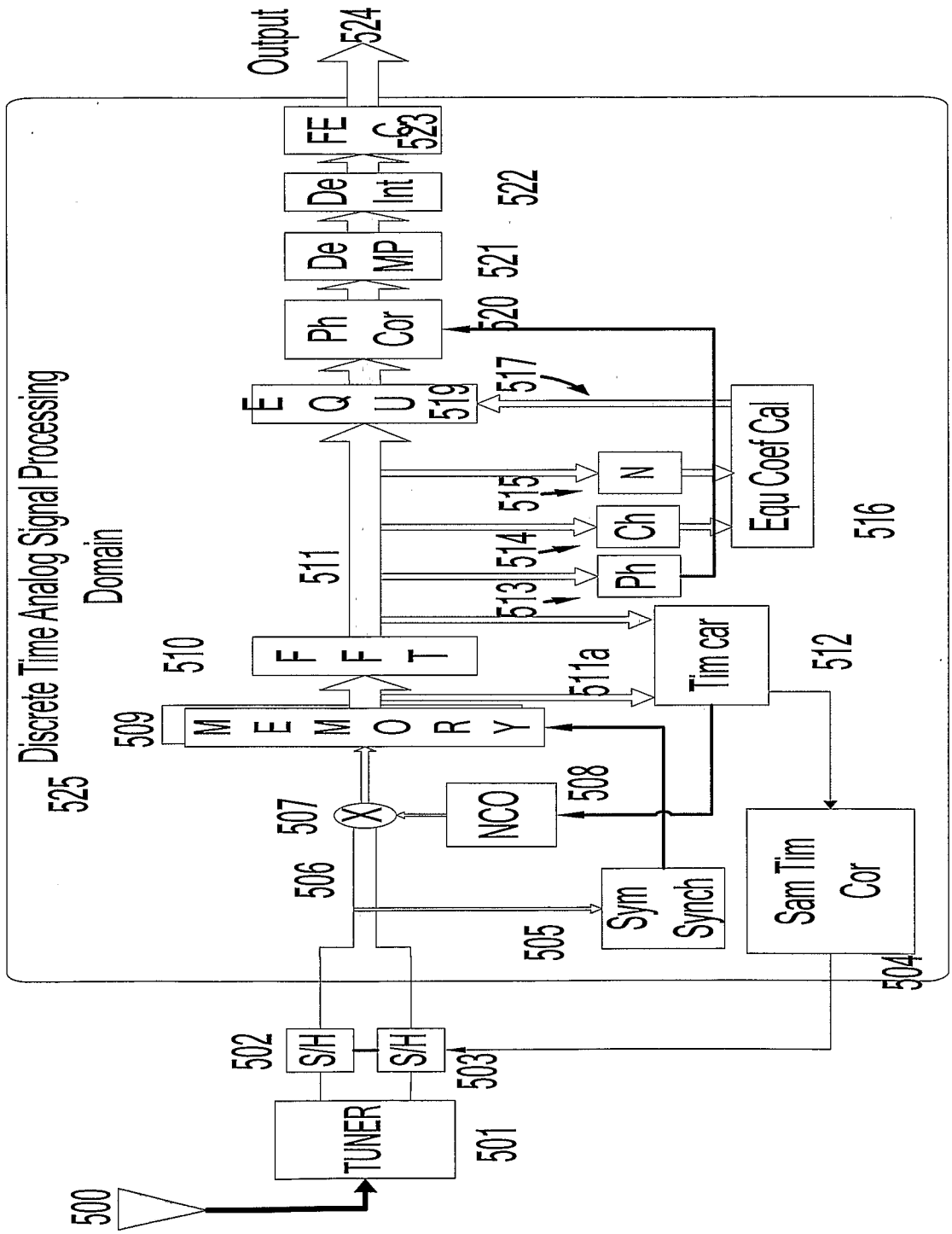

Figure 6: Eight points Fast Fourier Transform (FFT) flow/block diagram

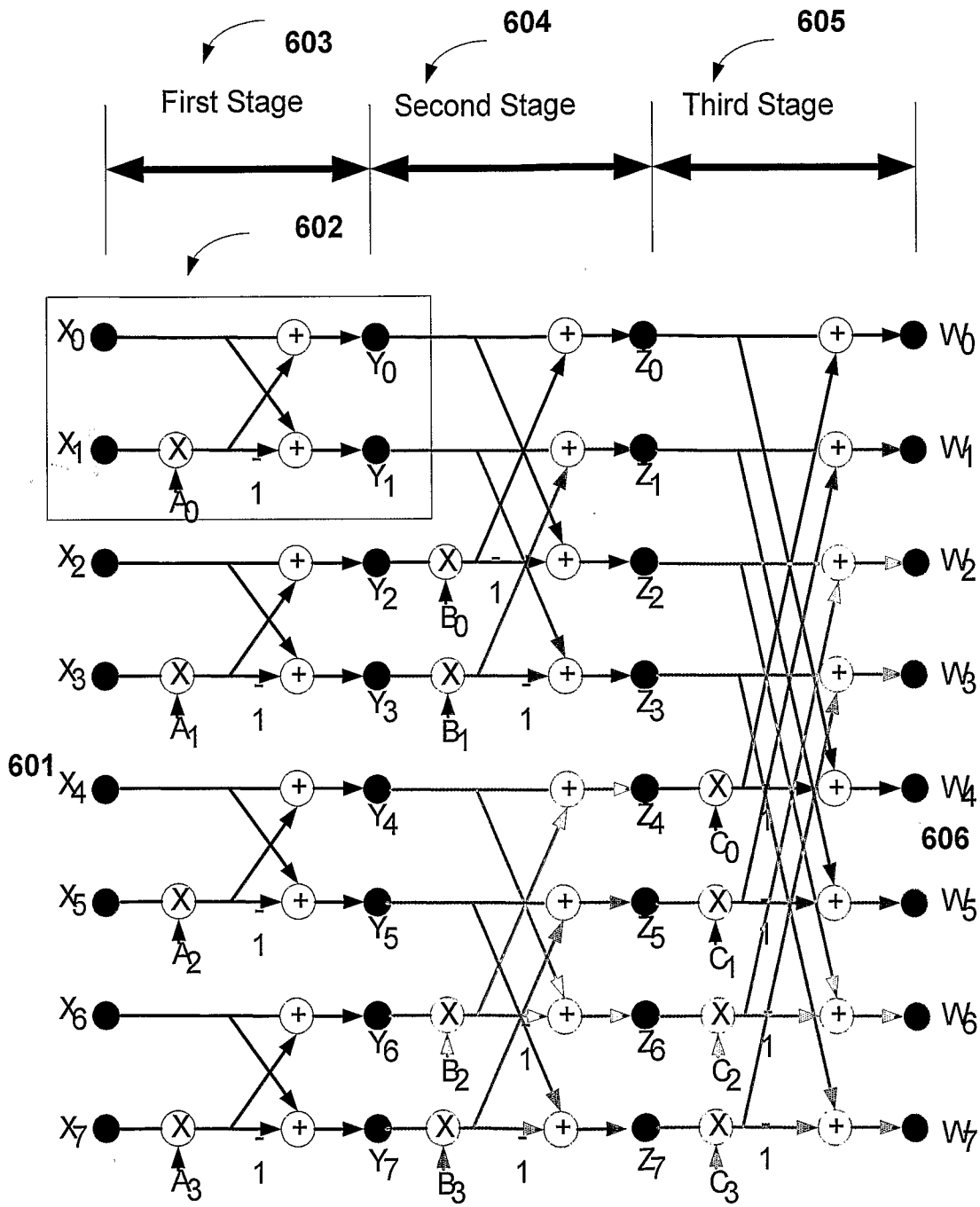

Figure 7: Addition and multiplication symbols with low power circuit implementation

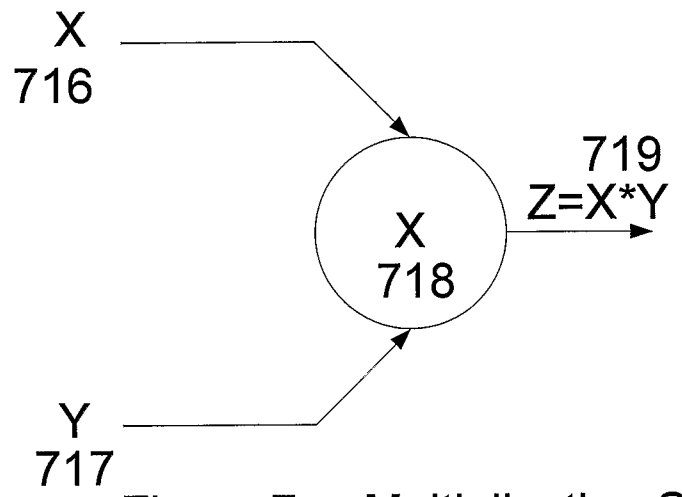

Figure 7a : Multiplication Symbol

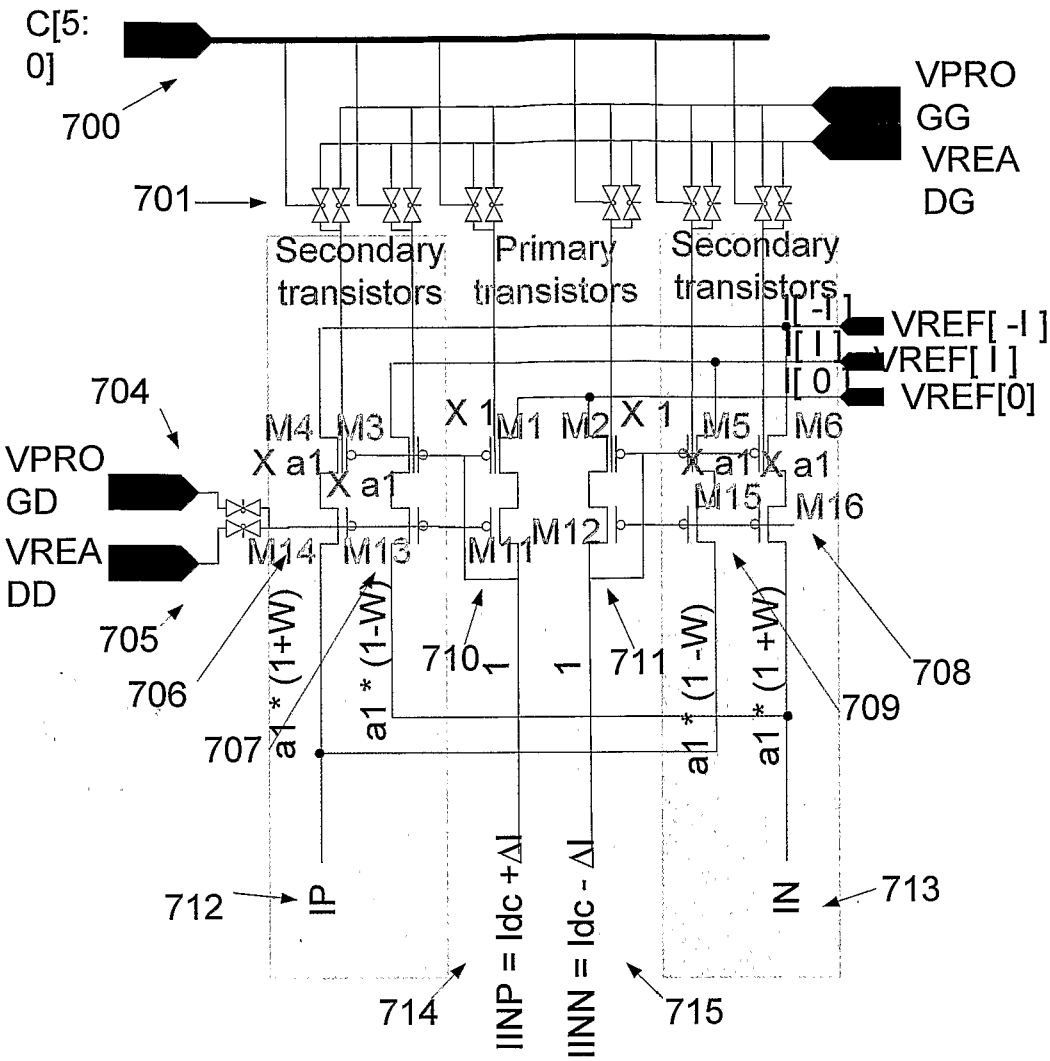

Figure 7b : Multiplication Circuit

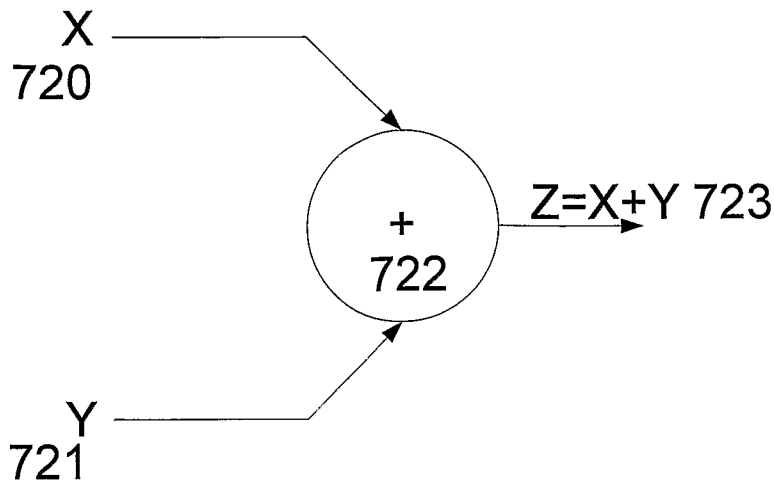

Figure 7c : Addition Symbol

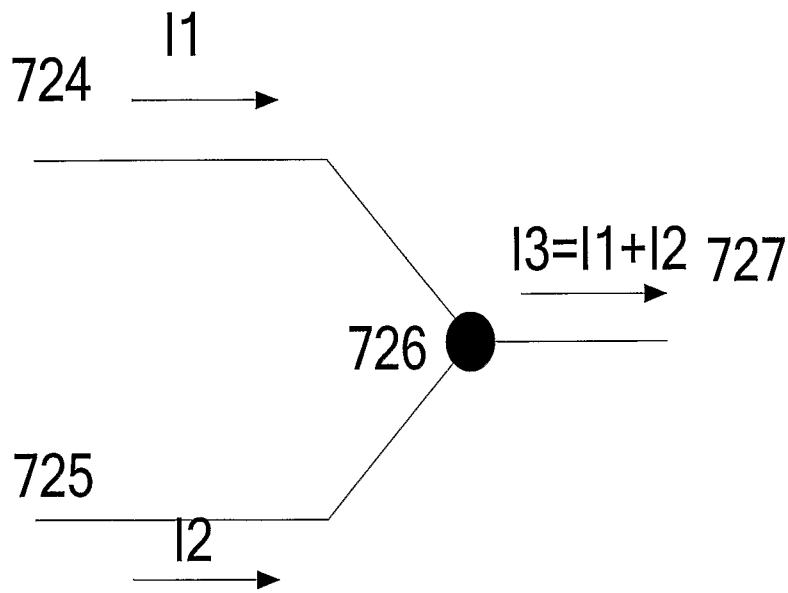

Figure 7d : Addition Circuit

Figure 8 : Ultra Low power OFDM receiver – with analog processing for parameters estimations/calculations

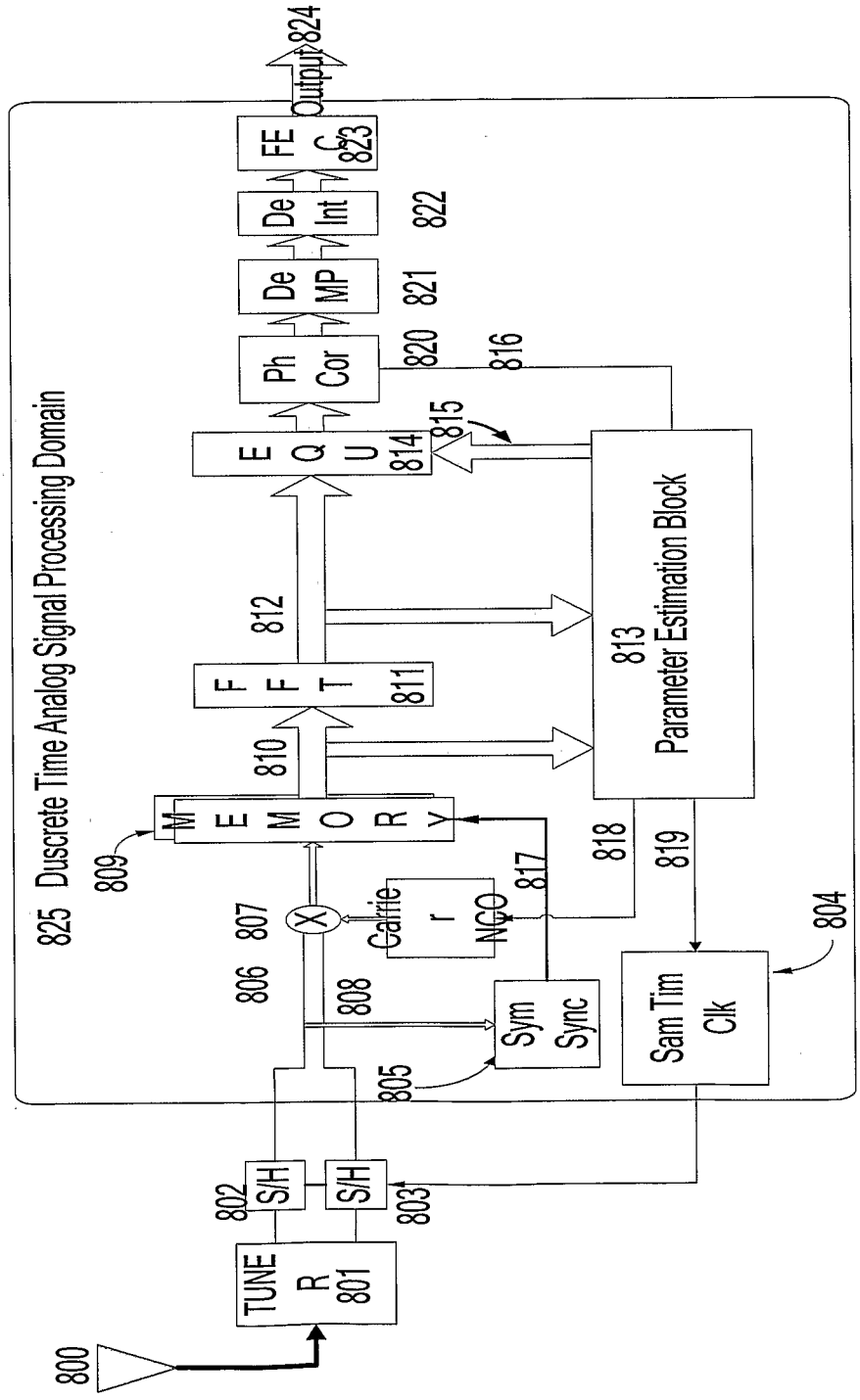

Figure 9 : Ultra Low power OFDM receiver – with Digital siganl Processing (DSP) for parameters estimations/calculations