



(51) International Patent Classification:
H01L 21/20 (2006.01)

(21) International Application Number:

PCT/GB2017/053246

(22) International Filing Date:

27 October 2017 (27.10.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

1618253.7

28 October 2016 (28.10.2016)

GB

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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,

OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: COATED WAFER

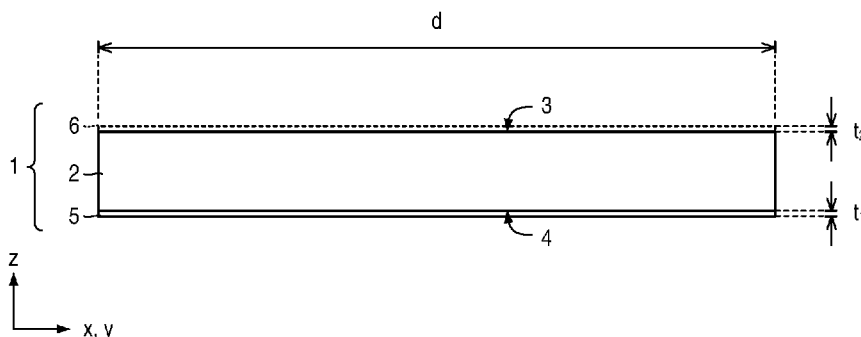


Fig. 1

(57) Abstract: A coated wafer is disclosed. The coated wafer comprises a wafer, such as a silicon or silicon-on-insulator wafer, having a principal surface and a reverse surface comprising a material or respective materials having a cubic crystal structure, such as a diamond or zinc blend crystal structure, and a melting temperature equal to or greater than 1,250°C. The coated wafer further comprises a layer of 3C-SiC having a thickness of at least 1 nm disposed on the reverse surface or on a dielectric layer supported by the reverse surface.



Coated wafer

Field of the Invention

The present invention relates to a coated wafer, particularly, but not exclusively, a
5 coated silicon wafer or a coated silicon-on-insulator wafer.

Background

Silicon carbide is wide-bandgap compound semiconductor material which is well suited
to being used in high-power and high-frequency electronic devices on account of having
10 high values of thermal conductivity, breakdown field and saturation velocity.

Silicon carbide exists in several different crystal forms (or “polytypes”) depending on
the sequence in which bi-layers of silicon and carbon stack. Of these polytypes, 3C-
silicon carbide (3C-SiC), 4H-silicon carbide (4H-SiC) and 6H-silicon carbide (6H-SiC)
15 are most commonly used in electronic devices.

4H- and 6H-SiC substrates are commercially available and high-quality homoepitaxial
layers of 4H- and 6H-SiC can be grown on these types of substrates. However, 4H- and
6H-SiC substrates are much more expensive to produce than silicon substrates and are
20 much smaller.

Although 3C-SiC substrates are not available, heteroepitaxial 3C-SiC can be grown on
silicon. This allows larger, cheaper silicon wafers to be used. Currently, however, hot-
wall chemical vapour deposition (CVD) reactors are used to grow 3C-SiC epitaxial
25 layers on silicon. High-temperature cold-wall CVD reactors have purportedly been
used to grow 3C-SiC epitaxial layers on silicon, although it is unclear how temperatures
exceeding 1,300°C can be achieved in such reactors without damaging the reactor or
component lying inside the reactor.

Moreover, most, if not all, of the research into 3C-SiC/Si heteroepitaxy tends to be
conducted on small substrates, such as 50 mm-diameter wafers or 10 mm dies. This
can give a misleading impression of whether or not a given heteroepitaxial process has
been successful and suitable for production since it is easier to achieve a uniform
temperature across a small substrate. Thus, small heterostructures may not reveal
35 problems regarding lack of uniformity across the wafer, voiding, and wafer bow.

- For example, R. Anzalone *et al.*: “Heteroepitaxy of 3C-SiC on different on-axis oriented silicon substrates”, Journal of Applied Physics, volume 105, page 084910 (2009) describes growing epitaxial films on 2-inch silicon wafers in a hot-wall, low-pressure chemical vapour (LPCVD) reactor using trichlorosilane (SiHCl_3) as a silicon supply, ethylene (C_2H_4) as a carbon supply and hydrogen (H_2) as a carrier gas at a growth temperature of 1350 °C. A hot-wall CVD reactor tends to have a low throughput and requires regular, costly maintenance.
- Wei-Yu Chen *et al.*: “Crystal Quality of 3C-SiC Influenced by the Diffusion Step in the Modified Four-Step Method”, Journal of The Electrochemical Society, volume 157, pages H377-H380 (2010) describes growing epitaxial films on 1 cm × cm substrate in a horizontal, cold-wall-type LPCVD system using silane (SiH_4) as a silicon supply, propane (C_3H_8) as a carbon supply and hydrogen (H_2) as a carrier gas at a growth temperature of 1420 °C. Although a cold-wall reactor is used, a complex 3- or 4-step deposition process is used, employing temperatures which are close to melting point of silicon. However, it is unclear if the process is repeatable, can be achieved without damaging the chamber and components inside the chamber, and can be used to produce high volumes of large-diameter wafers.
- Y. Gao *et al.*: “Low-temperature chemical-vapor deposition of 3C-SiC films on Si(100) using SiH_4 - C_2H_4 - HCl - H_2 ”, Journal of Crystal Growth, volume 191, pages 439 to 445 (1998) describes deposition of 3C-SiC films on silicon using HCl to suppress pure silicon nucleation. The paper, however, omits several details, such as wafer offcut and size, and does not mention whether the substrate suffers from warp or bow after deposition. Furthermore, the SiC films appear to be very rough. From micrographs shown in the paper, RMS surface roughness values of SiC films appear to be several hundreds of nanometres. Moreover, although using a higher concentration of HCl appears to improve crystal quality, it reduces growth rate and if HCl is omitted, then the SiC films are polycrystalline.

Summary

According to a first aspect of the present invention there is provided a coated wafer comprising a wafer having a principal surface (that is, the surface which will be processed to form semiconductor devices) and a reverse surface comprising a material
5 or respective materials having a cubic crystal structure and a melting temperature equal to or greater than 1,250 °C and a layer of 3C-SiC having a thickness of at least 1 nm disposed on the reverse surface or on a dielectric layer supported by (for example, disposed on) the reverse surface.

10 Thus, the 3C-SiC layer need not be necessarily used to form part of a device, but can be used solely or at least in part as a protective layer which can be processed using CMOS and other semiconductor fab processing techniques, i.e. industrial-scale processes.

During or after processing of the wafer, the protective 3C-SiC layer may be removed,
15 although it need not necessarily be removed since it can serve as a heat management layer due to the fact that 3C-SiC has a greater thermal conductivity than, for example, silicon or silicon dioxide.

The cubic crystal structure may be a diamond crystal structure. For example, silicon
20 and silicon-germanium have a diamond cubic crystal structure. The cubic crystal structure may be a zinc blende crystal structure. For example, gallium arsenide and other III-V semiconductors have a zinc blende crystal structure.

The 3C-SiC layer may be monocrystalline, for example, if the 3C-SiC layer is grown on
25 silicon or other suitable material.

The principal and reverse surfaces may comprise the same material.

The wafer may comprise a multilayer wafer, such as, for example, silicon-on-insulator,
30 silicon-on-sapphire, gallium nitride on silicon, silicon-germanium-on-silicon and the like.

Preferably, all of the materials in the wafer have a melting temperature equal to or greater than 1,250 °C.

35

The wafer may be a silicon or silicon-on-insulator wafer. Thus, the principal surface may be a principle silicon surface and the reverse surface may be a reverse silicon surface.

- 5 The wafer may be a gallium nitride wafer or a gallium nitride on silicon wafer.

The wafer may be a sapphire wafer or silicon on sapphire wafer.

- 10 The dielectric layer may be a layer of silicon dioxide (SiO_2), silicon nitride (Si_3N_4) or other dielectric material having melting temperature equal to or greater than $1,250^\circ\text{C}$. If the 3C-SiC layer is disposed on a dielectric layer, then the 3C-SiC layer is not monocrystalline (that is, it may be polycrystalline and/or amorphous).

- 15 The layer of 3C-SiC on the reverse surface preferably has a thickness no more than 300 nm. The layer of 3C-SiC on the reverse surface coats preferably at least 60%, more preferably at least 80% and still more preferably all of the reverse surface.

- 20 The coated wafer may further comprise a layer of 3C-SiC on the principal surface having a thickness of at least 1 nm. The layer of 3C-SiC on the principal surface preferably has a thickness no more than 300 nm. The layer of 3C-SiC on the principal surface is preferably monocrystalline.

- 25 The layer of 3C-SiC on the principal surface may coat at least 60%, more preferably at least 80% and still more preferably all of the principal surface.

The coated wafer may further comprise at least one window in the layer of 3C-SiC on the principal which exposes at least a portion of the principal surface.

- 30 The principal surface may be substantially flat, i.e. without features resulting from processing. The principal surface may be substantially unprocessed. Thus, the wafer may be provided in a blank form ready for CMOS or other semiconductor processing.

- 35 The coated wafer may further comprise at least one layer of silicon or dielectric material on the principal surface and/or one etched step in the principal surface. Thus, the wafer may be provided in part-processed form. The principal surface may have been subjected to at least one deposition, etching or implantation processing step.

The coated wafer may have a diameter of at least 100 mm, at least 200 mm or at least 450 mm.

- 5 According to a second aspect of the present invention there is provided a coated wafer comprising a wafer having a principal surface and a reverse surface comprising a material or respective materials having a cubic crystal structure and a melting temperature equal to or greater than 1,250 °C and a layer of 3C-SiC having a thickness of at least 1 nm on the reverse surface or on a dielectric layer supported by the reverse
10 surface.

According to a third aspect of the present invention there is provide a set of coated wafers according to the first or second aspect of the invention.

- 15 According to a fourth aspect of the present invention there is provided package comprising a wafer carrier, such as a cassette, and one or more coated wafers according to the first or second aspect of the invention removably housed in the wafer carrier.

- According to a fifth aspect of the present invention there is provided a method of
20 fabricating a coated wafer. The method comprises providing a wafer having a principal surface and a reverse surface comprising a material having a cubic crystal structure, such as a diamond or zinc blend crystal structure, and a melting temperature equal to or greater than 1,250 °C and providing a layer of 3C-SiC having a thickness of at least 1 nm on the reverse surface or on a dielectric layer supported by (for example, disposed
25 on) the reverse surface. The layer preferably has a thickness no more than 300 nm. Providing the 3C-SiC layer comprises forming the 3C-SiC layer by growing epitaxial 3C-SiC on the reverse surface. The method comprises providing the wafer, such as a silicon or silicon-on-insulator wafer, in a cold-wall chemical vapour deposition reactor. The method comprises heating the wafer to a temperature equal to or greater than 700
30 °C and equal to or less than 1200 °C and introducing a gas mixture into the reactor, while the substrate is at the temperature, so as to deposit an epitaxial layer of 3C-SiC on the reverse silicon surface of the wafer. The gas mixture comprises a silicon source precursor, a carbon source precursor and a carrier gas.

The method may further comprise providing a layer of monocrystalline 3C-SiC layer having a thickness of at least 1 nm on the principal surface of the wafer. The layer preferably has a thickness no more than 300 nm.

- 5 The 3C-SiC growth rate may be at least 1 $\mu\text{m}/\text{h}$. The growth rate may be at least 10 $\mu\text{m}/\text{h}$. The growth rate may be up to 20 $\mu\text{m}/\text{h}$ or more. However, lower growth rates can be used, for example, to grow thin layers (e.g. < 100 nm) of 3C-SiC.

10 The carbon source precursor may be an organosilicon compound. The carbon source precursor may be a methyl-containing silane. Preferably, the carbon source precursor is trimethylsilane ($\text{C}_3\text{H}_{10}\text{Si}$).

The silicon source precursor and carbon source precursor are preferably different, i.e. a single precursor serving as both silicon and carbon sources is not used.

15

The carbon source precursor may have a flow rate of at least 1 sccm or at least 10 sccm.

The silicon source precursor may be a silane, or a chlorine-containing silane.

20 Preferably, the silicon source precursor is dichlorosilane (SiH_2Cl_2). The silicon source precursor may be trichlorosilane. The silicon source precursor may comprise first and second precursor components. For example, the silicon source precursor may comprise a mixture of gases, such as silane or disilane and hydrogen chloride (HCl).

The silicon source precursor may have a flow rate of at least 1 sccm or at least 10 sccm.

25

The carrier gas is preferably hydrogen (H_2).

The carrier gas may have a flow rate of at least 1 sccm or at least 10 sccm.

30 The ratio of the flow rate of the carbon source precursor and the silicon source precursor may be less than 3 and greater than 0.33. The ratio of the flow rate of the carbon source precursor and the silicon source precursor may be less than 2 and greater than 0.5. The flow rates of the carbon source precursor and the silicon source precursor may be the same or substantially the same (e.g. ratio of the flow rate of the
35 carbon source precursor and the silicon source precursor is less than 1.2 and greater than 0.8).

The gas mixture preferably consists of a silicon source precursor, a carbon source precursor and a carrier gas or a silicon source precursor, a carbon source precursor, a carrier gas and a dopant source precursor.

5

The gas mixture preferably excludes (i.e. does not include or consist of) hydrogen chloride (HCl) gas.

10 The temperature may be equal to or greater than 900 °C, equal to or greater than 900 °C, or equal to or greater than 1000 °C. The temperature is preferably equal to or greater than 1100 °C.

15 Pressure in the reactor during deposition may be equal to or greater than 66.7 Pa (0.5 Torr) and equal to or less than 26.7 kPa (200 Torr) or equal to or less than 80 kPa (600 Torr), i.e. sub-atmospheric chemical vapour deposition. Pressure in the reactor during deposition is equal to or greater than 13.3 kPa (100 Torr) and equal to or less than 13.3 kPa (760 Torr).

20 The principal surface and/or reverse surface may have an (001) surface orientation. The principal surface and/or reverse surface may have a (110) orientation. The principal surface and/or reverse surface may have a (111) orientation. An epilayer of 3C-SiC having (111) orientation (i.e. grown on (111) Si) can be used as a substrate for gallium nitride (GaN) overgrowth.

25 Preferably, the principal surface and/or reverse surface is/are flat, i.e. unpatterned. The principal surface and/or reverse surface may be on-axis. The principal surface and/or reverse surface may be off-axis.

30 For a wafer having a diameter of at least 100 mm, there is substantially no wafer bow. The principal surface and/or reverse surface may have an RMS surface roughness, measured by AFM, equal to or less than 20 nm and preferably equal to or less than 10 nm.

35 The wafer may have a diameter which is at least 100 mm, at least 200 mm or at least 450 mm or more. The wafer is preferably a single-crystal wafer. The silicon-on-insulator (SOI) wafer may be a silicon-on-sapphire (SoS) wafer or other, similar type of

substrates.

Brief Description of the Drawings

Certain embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a coated silicon wafer;

5 Figure 2 shows a coated silicon-on-insulator wafer; and

Figure 3 shows a wafer carrier housing coated wafers.

Detailed Description of Certain Embodiments

Referring to Figure 1, a first coated wafer 1 is shown.

10

The coated wafer 1 comprises a monocrystalline silicon substrate 2 having first and second faces 3, 4 (herein referred to as “upper” and “lower” faces or surfaces respectively or “principal” and “reverse” faces or surfaces respectively).

15 A first layer 5 of monocrystalline 3C-SiC (hereinafter simply referred to as the first 3C-SiC layer) having a thickness of at least 1 nm is disposed on the reverse silicon surface 4. The first 3C-SiC layer 5 can have a thickness of at least 5 nm or at least 10 nm. The first 3C-SiC layer 5 can have a thickness of no more than 300 nm or no more than 100 nm.

20

Optionally, a second layer 6 of monocrystalline 3C-SiC (hereinafter simply referred to as the second 3C-SiC layer) having a thickness of at least 1 nm may be disposed on the principal silicon surface 3. The second 3C-SiC layer 6 can have a thickness of at least 5 nm or at least 10 nm. The second 3C-SiC layer 6 can have a thickness of no more than

25 300 nm or no more than 100 nm.

Referring to Figure 2, a second coated wafer 1' is shown.

30 The second coated wafer 1' is the same as the first coated wafer 1 (Figure 1) except that a silicon-on-insulator wafer 2' is used instead of a silicon wafer 2. The silicon-on-insulator wafer 2' includes a silicon handle 7, a buried oxide layer 8 and a silicon cap 9. The silicon-on-insulator wafer 2' has silicon principal and reverse surfaces 10, 11.

35 As will be now be explained in more detail, the 3C-SiC layer(s) 5, 6 is/are grown by a low-temperature (i.e. below 1200 °C) deposition process in a cold-wall chemical vapour deposition (CVD) reactor of a type normally used in silicon processing.

Growing 3C-SiC on Si

For the coated wafers 1, 1', herein described, crystalline 3C-SiC can be grown on silicon at a temperature below 1200 °C using a cold-wall, reduced-pressure, sub-atmospheric-
5 pressure or atmospheric press CVD reactor of a type normally used in silicon processing. An example of a suitable reactor system is the ASM Epsilon 2000 RP-CVD system.

Deposition is carried out using a gas mixture consisting of a silicon source precursor, a
10 carbon source precursor, an optional dopant precursor and a carrier gas. A single silicon/carbon precursor is not used. Hydrogen chloride is not included in the gas mixture.

The silicon source precursor takes the form of dichlorosilane (which may be referred to
15 as "DCS") having a chemical formula SiH_2Cl_2 and the silicon source precursor takes the form of trimethylsilane (which may be referred to as "TMS") having a chemical formula $\text{C}_3\text{H}_{10}\text{Si}$. An n-type dopant precursor may take the form of arsine (AsH_3) or phosphine (PH_3) and a p-type dopant precursor may take the form diborane (B_2H_6). Hydrogen gas is used as a carrier gas.

20 Using these or other similar precursors, crystalline 3C-SiC epilayers can be grown on blank (i.e. unpatterned) silicon substrates, such as on-axis (001)-orientated silicon wafers, at a deposition temperature, T_{EPI} , at or below 1,200 °C and growth rates above 10 $\mu\text{m}/\text{h}$ can be achieved. If required, lower growth rates can be used.

25 Examples of other silicon source precursors include other silanes, such as silane (SiH_4) or chlorine-containing silanes, such as trichlorosilane (SiHCl_3). Examples of other carbon source precursors include methyl-containing silanes, such as methylsilane (CH_3Si) or penta-methylene methyl silane ($\text{C}_6\text{H}_{14}\text{Si}$).

30 The on-axis (001)-orientated silicon wafer is cleaned and its native surface oxide (not shown) is removed using a hydrofluoric (HF) acid dip. The wafer is loaded into the reactor (not shown) at a standby temperature, T_{SB} , via the load lock at atmospheric pressure. The standby temperature, T_{SB} , is 900 °C. However, the standby temperature,
35 T_{SB} , can take a value between room temperature and 1,200 °C.

Carrier gas, in this case hydrogen, is introduced into the reactor at a flow rate of 10 slm at a pressure 13.3 kPa (100 Torr). The heaters are switched on and are controlled so that the temperature of the wafer reaches and is maintained at a set-point temperature, which in this case is 1,190 °C.

5

A mixture of dichlorosilane, trimethylsilane and hydrogen is introduced into the reactor (not shown) having flow rates of 10 sccm, 10 sccm and 10,000 sccm respectively, while temperature is maintained at 1,190 °C and pressure is maintained at 13.3 kPa (100 Torr). Thus, the partial pressures of the dichlorosilane and trimethylsilane are 13.3 Pa, 13.3 Pa respectively. The growth rate for this gas mixture and gas flow rates, and at this temperature and pressure is about 20 µm/h.

10

The gas mixture continues to flow until the desired thickness of 3C-SiC is grown. Once the desired thickness has been reached, the flow of dichlorosilane and trimethylsilane is stopped, but the carrier gas continues to flow. The heaters are switched off and the 3C-SiC/Si wafer is allowed to cool. This can take about 5 to 10 minutes. Once the wafer has cooled, carrier gas flow is stopped and the reactor purged. The 3C-SiC/Si wafer is then removed from the reactor.

15

The process can be modified by forming *in-situ* a thin seed layer (not shown) prior to epitaxy. The seed layer (not shown) comprises a layer of silicon-carbon ($\text{Si}_{1-x}\text{C}_x$ where x is about 0.01) having a thickness of up to 10 nm.

20

After loading the wafer into the reactor at a standby temperature, T_{SB} , via the load lock at atmospheric pressure, the wafer is cooled to about 600 °C. A short deposition cycle (e.g. lasting a few minutes) using the same precursors, same flow rates and same pressure is carried out. Due to the lower temperature, however, the process does not result in epitaxy.

25

Without wishing to be bound by theory, the seed layer (not shown) is thought to help prevent the formation of voids at the surface of the silicon during epitaxy.

30

No wafer bow can be observed in a 3C-SiC/Si heterostructure 1 comprising a 3C-SiC epilayer grown on a 100 mm-diameter (100) orientation, on-axis single-crystal silicon wafer at 1,190 °C using dichlorosilane and trimethylsilane using the process

35

hereinbefore described. Furthermore, the 3C-SiC/Si heterostructure has an RMS surface roughness of (10 ± 1) nm as measured using an atomic force microscope.

Referring also to Figure 3, the coated wafers 1, 1' can be transported to or from a fab (not shown) or within the fab (not shown) using a wafer carrier 10 having a cassette 11 for holding a set of one or more coated wafers 1, 1'.

Modifications

It will be appreciated that various modifications may be made to the embodiments hereinbefore described. Such modifications may involve equivalent and other features which are already known in wafer processing and in heteroepitaxy which may be used instead of or in addition to features already described herein. Features of one embodiment may be replaced or supplemented by features of another embodiment.

For example, the wafer need not be a silicon or silicon-on-insulator wafer, but may be another suitable type of wafer comprising cubic crystal structure material(s), for example, wafers such as a GaN wafer or a GaN on silicon wafer, or sapphire wafer.

Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel features or any novel combination of features disclosed herein either explicitly or implicitly or any generalization thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

Claims

1. A coated wafer comprising:
a wafer having a principal surface and a reverse surface comprising a material or
5 respective materials having a cubic crystal structure and a melting temperature equal to
or greater than 1,250 °C; and
a layer of 3C-SiC having a thickness of at least 1 nm disposed on the reverse
surface or on a dielectric layer supported by the reverse surface.
- 10 2. A coated wafer according to claim 1, wherein the cubic crystal structure is a
diamond crystal structure or a zinc blend crystal structure.
3. A coated wafer according to claim 1 or 2, wherein the wafer is a silicon or silicon-
on-insulator wafer.
- 15 4. A coated wafer according to claim 1 or 2, wherein the wafer is a gallium nitride
wafer.
5. A coated wafer according to claim 1 or 2, wherein the wafer is a sapphire wafer.
- 20 6. A coated wafer according to any preceding claim, wherein the layer of
monocrystalline 3C-SiC on the reverse surface has a thickness no more than 300 nm.
7. A coated wafer according to any preceding claim, wherein the layer of
25 monocrystalline 3C-SiC on the reverse surface coats at least 60% of the reverse surface.
8. A coated wafer according to claim 7, wherein the layer of monocrystalline 3C-SiC
on the reverse surface coats at least 80% of the reverse surface.
- 30 9. A coated wafer according to claim 8, wherein the layer of monocrystalline 3C-SiC
on the reverse surface coats all of the reverse surface.
10. A coated wafer according to any preceding claim, further comprising:
a layer of monocrystalline 3C-SiC on the principal surface having a thickness of at
35 least 1 nm.

11. A coated wafer according to claim 10, wherein the layer of monocrystalline 3C-SiC on the principal surface has a thickness no more than 300 nm.
12. A coated wafer according to claim 10 or 11, wherein the layer of monocrystalline
5 3C-SiC on the principal surface coats at least 60% of the principal surface.
13. A coated wafer according to claim 12, wherein the layer of monocrystalline 3C-SiC on the principal surface coats at least 80% of the principal surface.
- 10 14. A coated wafer according to claim 13, wherein the layer of monocrystalline 3C-SiC on the principal surface coats all of the principal surface.
15. A coated wafer according to any one of claims 10 to 14, further comprising at least one window in the layer of monocrystalline 3C-SiC on the principal surface which
15 exposes at least a portion of the principal surface.
16. A coated wafer according to any one of claims 1 to 15, wherein the principal surface is substantially flat.
- 20 17. A coated wafer according to any one of claims 1 to 16, wherein the principal surface is substantially unprocessed.
18. A coated wafer according to any one of claims 1 to 15, further comprising at least one layer of semiconductor material or dielectric material on the principal surface
25 and/or one etched step in the principal surface.
19. A coated wafer according to any one of claims 1 to 15 or 18, wherein the principal surface has been subjected to at least one deposition, etching or implantation processing step.
30
20. A coated wafer according to any preceding claim, wherein the coated wafer has a diameter of at least 100 mm.
21. A coated wafer according to any preceding claim, wherein the coated wafer has a
35 diameter of at least 200 mm.

22. A coated wafer according to any preceding claim, wherein the coated wafer has a diameter of at least 450 mm.

23. A set of coated wafers according to any preceding claim.

5

24. A method of semiconductor processing comprising:
receiving a coated wafer according to any one of claims 1 to 22; and
performing a plurality of processing steps on the coated wafer so as to form
semiconductor devices.

10

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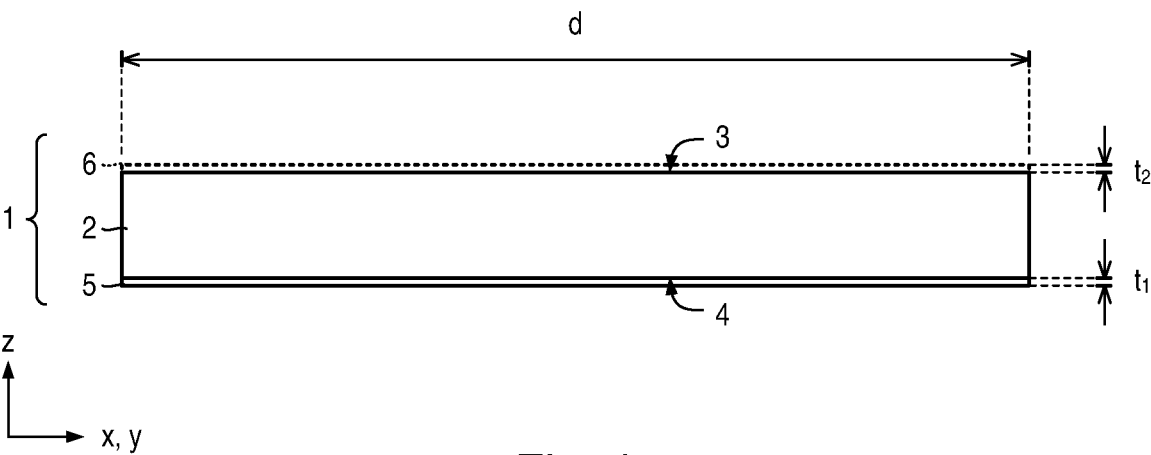


Fig. 1

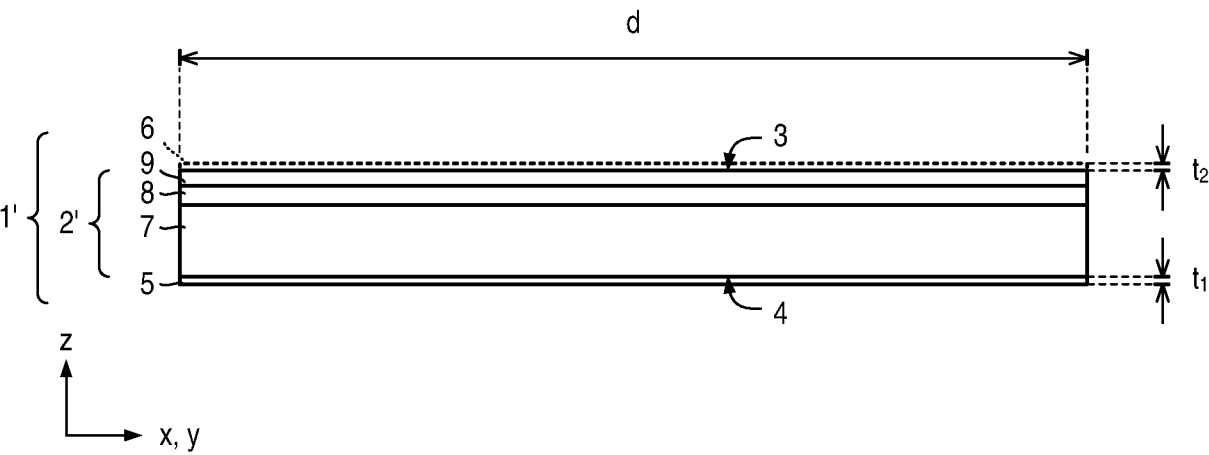


Fig. 2

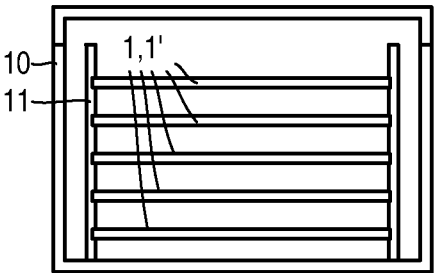


Fig. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2017/053246

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GAO Y ET AL: "Low-temperature chemical-vapor deposition of 3C-SiC films on Si(100) using SiH ⁴ -C ² H ⁴ -HCl-H ² ", JOURNAL OF CRYSTAL GROWTH, ELSEVIER, AMSTERDAM, NL, vol. 191, no. 3, 15 July 1998 (1998-07-15), pages 439-445, XP004148441, ISSN: 0022-0248, DOI: 10.1016/S0022-0248(98)00212-7 cited in the application 2. Experimental procedure; table 3	1-9,16, 17,20-24
X	US 2016/247967 A1 (WARD PETER [GB]) 25 August 2016 (2016-08-25) paragraphs [0054] - [0063]; figure 1	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

16 January 2018

Date of mailing of the international search report

23/01/2018

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2017/053246

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016247967	A1	25-08-2016	NONE
