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[54] **DRIVE CIRCUITRY FOR DISPLAY TUBES**
8 Claims, 3 Drawing Figs.

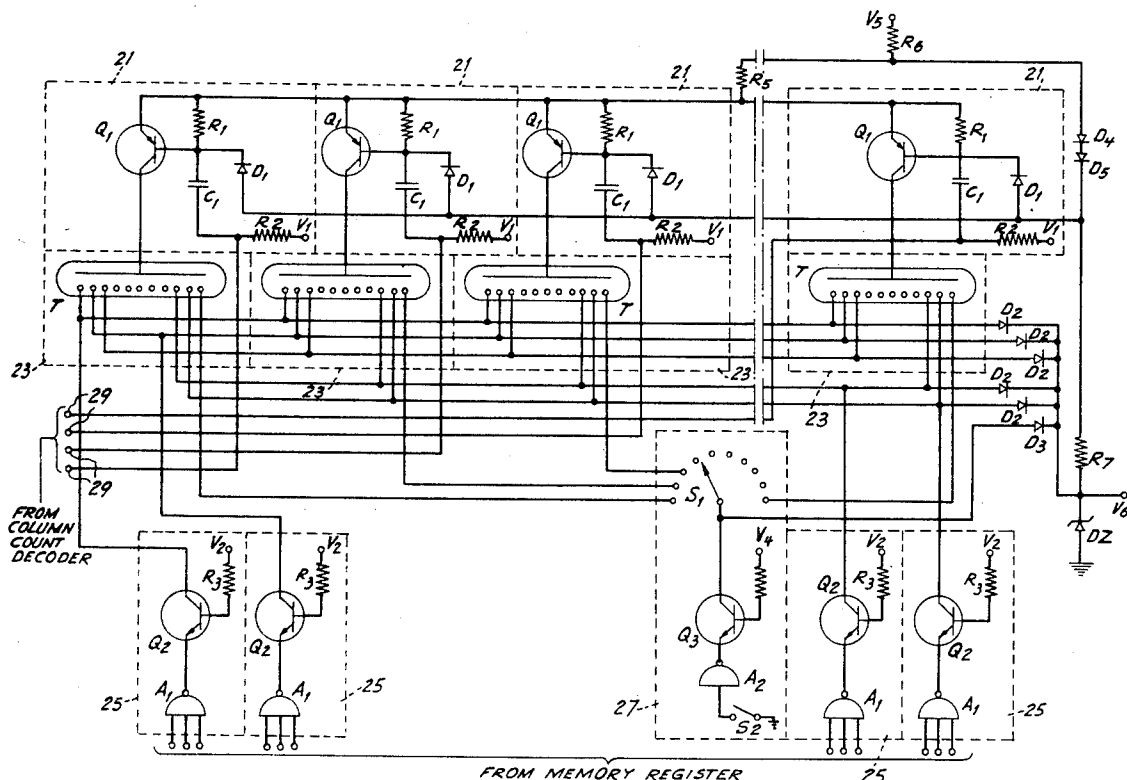
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336; 315/84.6; 307/223

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ABSTRACT: Apparatus for limiting the current, applied to the anodes of a data display system of the type comprising data display tubes having a single anode and a plurality of cathodes, to a constant level when the display tubes are energized as described. The emitter-collector terminals of a current control transistor are connected between an anode voltage source and the anodes of each of the display tubes. The base terminals of the transistors are connected to a voltage limiting zener diode which is biased by the anode voltage source. The zener diode limits the voltage which can be applied to the base of each transistor thereby limiting the current that can flow through each transistor. The base terminals of the transistors are also connected to a control system which controls when a particular anode transistor is to conduct current.



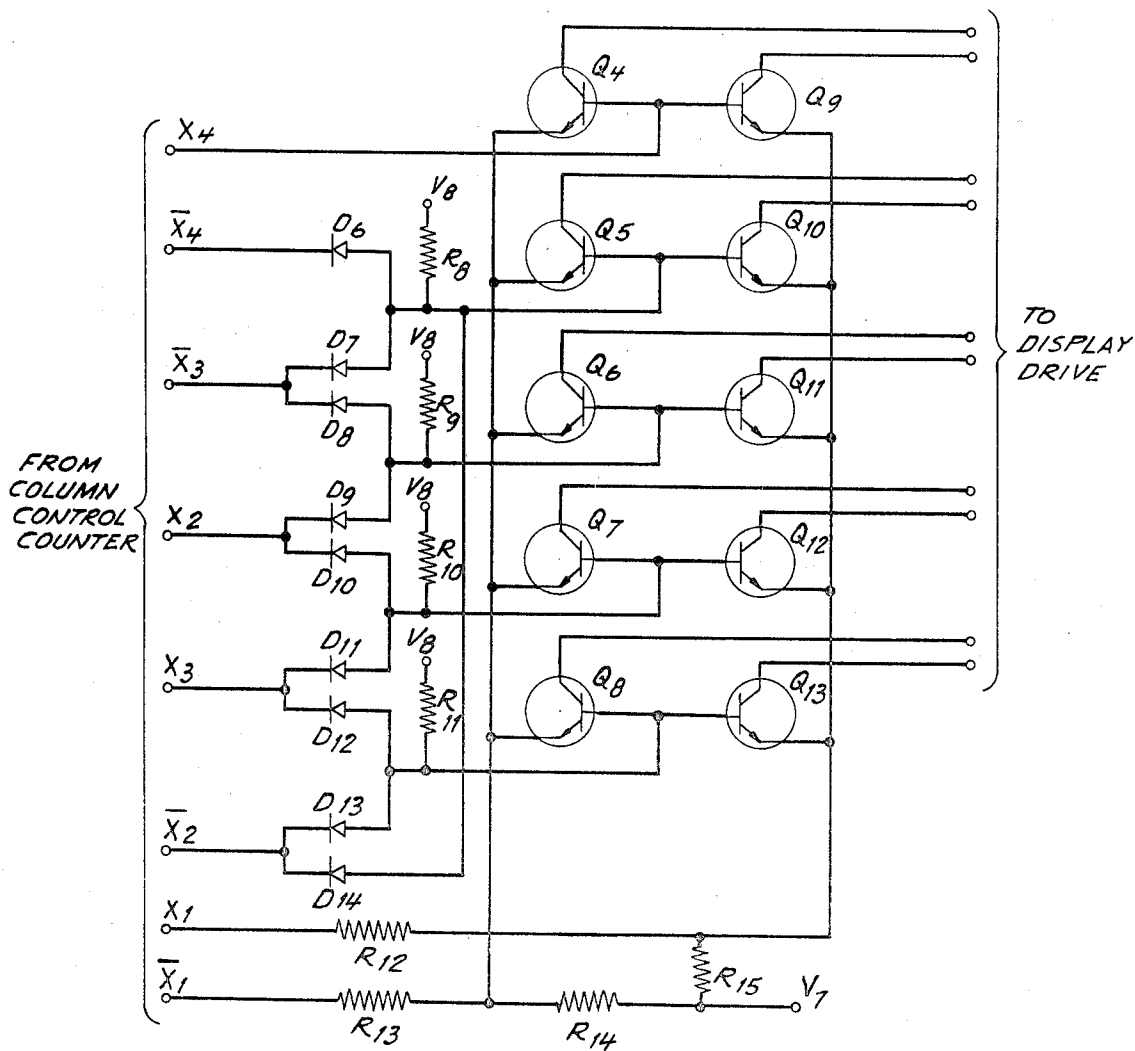
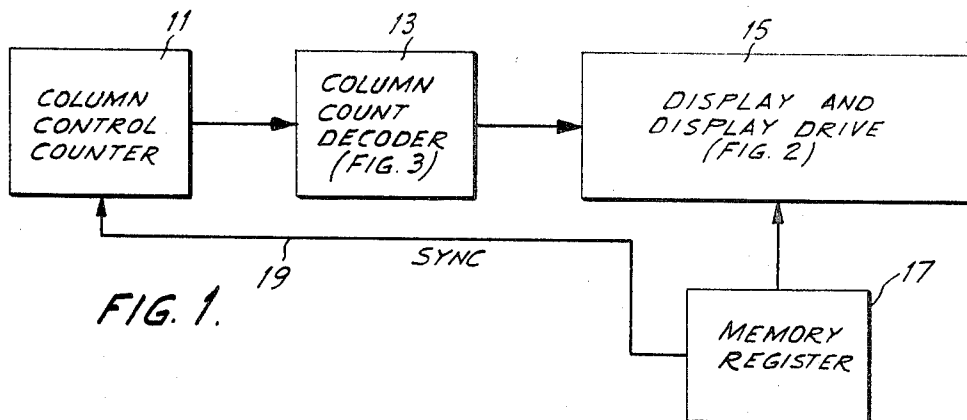
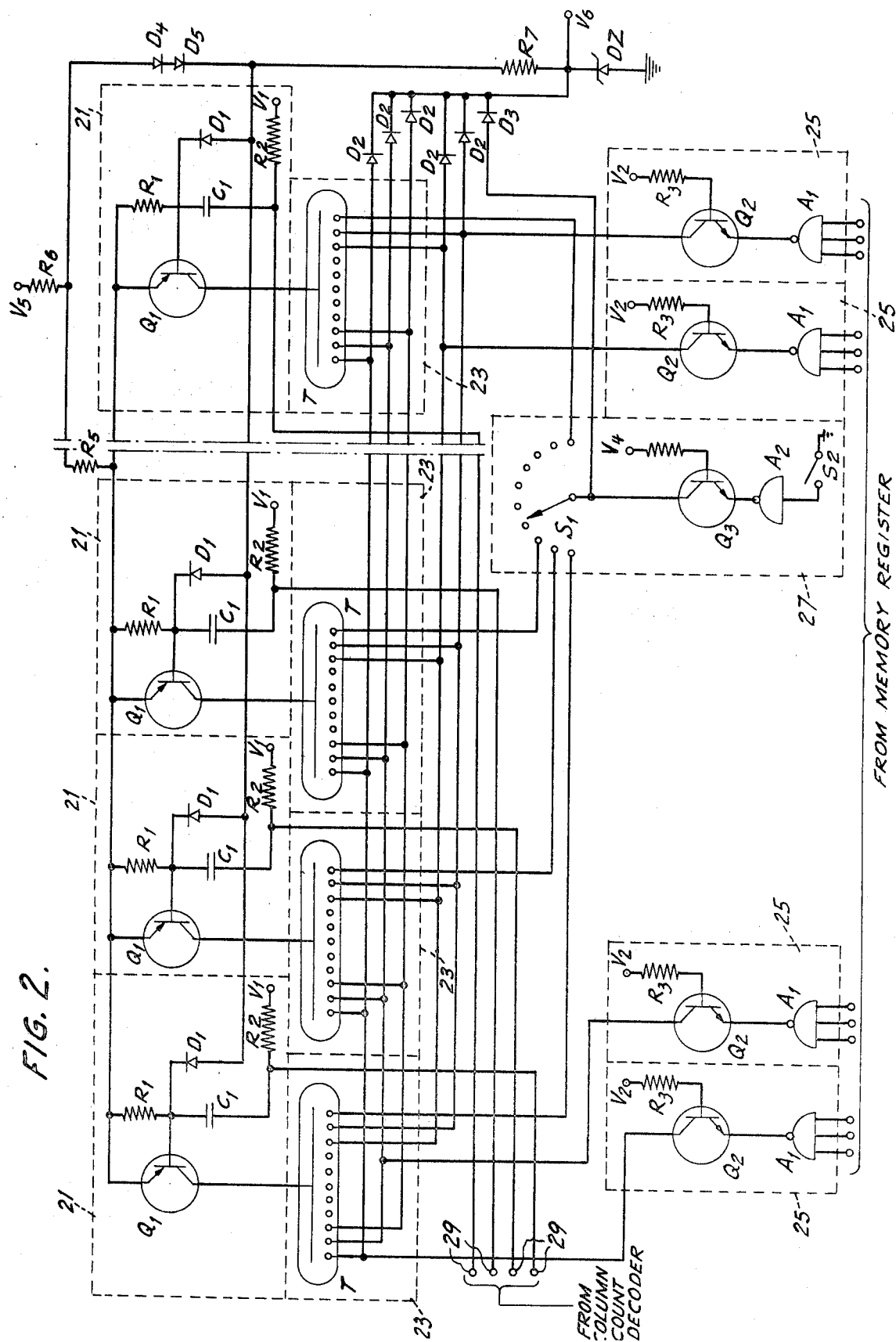


FIG. 3.

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DRIVE CIRCUITRY FOR DISPLAY TUBES

BACKGROUND OF THE INVENTION

Systems for displaying data "readout" from computer registers or other data sources are well known. The data source is connected by drive circuitry to an indicia display tube such as a Nixie (registered TM of the Burroughs Corporation) tube. The drive circuitry energizes the appropriate cathode of the display tube so that the desired indicia is displayed. Normally, a plurality of display tubes are provided, and the drive circuit drives all of the tubes so that a composition indicia display is presented for viewing.

Prior art drive circuits have taken several forms, generally, the anodes of the display tubes have been directly connected to a source of potential. The plural electrodes of the tubes have been connected by control circuits to the data source. When a data signal occurs, one of the control circuits is energized and causes an indicia display on the face of the tube connected to that control circuit. If desired, each tube of a plurality of tubes can be controlled so as to display indicia in a sequential order until a composite data indicia display is presented for viewing.

The major disadvantage of prior art drive circuits is their requirement that the anode voltage be high and stable. That is, for successful operation the anodes must be connected to a stable source of high voltage. If the voltage of the source is not sufficiently well regulated, excessive anode currents occur and reduce the life of the tube. Alternatively, if low currents occur, the light intensity of the display tubes is reduced to an undesirable low level. Because the anode voltage must be high and well regulated, a sophisticated regulating circuit connecting the anode bias source (if the source is unregulated) to the anode is required. Alternatively, a sophisticated regulating circuit may be included in the bias source per se.

In addition to the foregoing disadvantage, prior art drive circuits have further disadvantages. Specifically, the high voltage anode bias or drive circuit and, high voltage components are generally more expensive than lower voltage components. In addition, because many prior art drive circuits include DC rather than AC coupling, the display tubes of prior art systems can turn "on" and draw excessive current. The excessive current may damage either the display tubes or their drive circuitry if there is a fault in the system preceding the drive circuitry.

Therefore, it is an object of this invention to provide a new and improved drive circuit for an indicia display system.

It is also an object of this invention to provide a constant current anode circuit for use in display tube drive circuitry that operates from an unregulated voltage source.

It is another object of this invention to provide a new and improved drive circuit suitable for driving a plurality of display tubes from an unregulated anode voltage supply.

SUMMARY OF THE INVENTION

In accordance with a principal of this invention an electronic drive circuit for an indicia display tube system is provided. Each tube includes a plurality of cathodes for controlling the displaying of a plurality of indicia and a single anode. A plurality of cathode control means are connected to the cathodes of the tube in a predetermined manner, and an anode control means is connected to the anode of the tube. The plurality of cathode control means are connected to a source of data, such as the memory register of a computer so that data information signals control the indicia display of the tubes. The anode control means is connected to a decoder, and the decoder is connected to a counter. The decoder decodes the output from the counter and energizes the anode of the display tube when a particular code is generated by the counter. Hence, the data source provides a data signal that determines what indicia is to be displayed and the decoder determines when the tube will display that indicia.

In accordance with another principal of the invention, the anode control means applies a constant current to the anode of the tube. That is, the current driving the anode is constant regardless of voltage fluctuations. Hence, the life of the tube is not reduced because of the occurrence of overcurrent conditions, nor is the intensity of the display reduced because of undercurrent conditions. These conditions cannot occur because the anode current is constant even though the source voltage changes.

In accordance with still another principle of the invention, the anode control means comprises a relatively low voltage transistor connected between the source of potential and the anode of the display tube so as to apply constant current to the tube when the transistor is triggered "on". The base of the transistor is connected through an AC coupling network to the output of the decoder.

It will be appreciated by those skilled in the art and others that the invention is a rather uncomplicated circuit for driving a display tube system. The output from a data source determines which element of the display tube indicia elements is to be ignited. The output from the decoder determines when the tube is to display the indicia. Alternatively, the output of the decoder could determine which tube of a plurality of tubes is to display the indicia. In addition to controlling the display, the invention provides an anode control means that applies a constant current to the anodes of the tubes to prevent either an overcurrent or an undercurrent condition. An overcurrent condition reduces the life of a tube while an undercurrent condition reduces the intensity of the indicia displayed by a tube. Moreover, the source voltage can be lower in potential than prior art source voltages and, it can fluctuate. A lower source voltage allows the use of lower voltage components in the anode control circuit. And, lower voltage components are more economical than higher voltage components. Finally, because AC coupling is provided, the display tubes will "drop out" if there is a failure in the decoder circuit or the circuits preceding the decoder. Hence, the invention generally provides improved circuit for driving a display tube system that is uncomplicated and economical.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing objects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

FIG. 1 is a block diagram illustrating the use of the invention in a display system;

FIG. 2 is a partial schematic diagram illustrating the display drive circuit of the invention; and

FIG. 3 is a schematic diagram illustrating a decoder suitable for use in the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now to the drawings wherein like reference numerals designate like parts throughout the several views, FIG. 1 is a block diagram illustrating a display system using the invention. The system illustrated in FIG. 1 comprises a column control counter 11, a column count decoder 13, a display and display drive 15, and a recirculating memory register 17. The output from the column control counter 11 is connected to the input of the column count decoder 13, and the output from the column count decoder is connected to one input of the display and display drive 15. The sync line 19 is connected between the column control counter 11 and the memory register 17.

The column control counter 11 generates a parallel control signal on a plurality of lines. Preferably, this signal is an excess-3 binary signal, hence, it is a 4-bit code signal. The column count decoder 13 decodes the control signal from the column control counter and generates a single control signal. The single control signal is related to the particular parallel

code signal submitted by the column control counter and is applied to the display drive 15. This signal, as hereinafter described, controls which tube of a plurality of display tubes displays a particular indicia. For purposes of description, all indicia are numerical indicia ranging from 0 to 9. Hence, numerical signals are displayed on the display tubes.

The memory register 17 generates a signal that determines which indicia of a plurality of indicia will be displayed on the tube selected by the column count decoder signal. The memory register may be the memory register of a computer, or any other similar data storage source. The sync line 19 merely provides a sync signal between the column control counter and the memory register so that the tube selection signal from the column count decoder is in synchronism with the indicia selection signal from the memory register. Generally speaking, signals representing a multidigit number recirculate in the memory register. At each recirculation a different display tube is activated. Therefore, to display all the tubes there must be as many circulations as the number of tubes. The digits are displayed repeatedly, but because of the frequency of display, they appear to the eye to be constantly displayed.

FIG. 2 illustrates the display drive circuit of the invention and is suitable for use in the system illustrated in FIG. 1. For purposes of clarity, FIG. 2 is only a partial schematic diagram. That is, FIG. 2 only illustrates four display tube circuits 23, four anode control circuits 21, four cathode control circuits 25, and a single decimal point control circuit 27. However, the drive circuit illustrated in FIG. 2 can be expanded to control as many display tubes as desired. In accordance with the column count decoder illustrated in FIG. 3 and hereinafter described, a 10-tube system is contemplated by the embodiment of the invention herein described. But, as stated above, only four of the 10 tubes are illustrated in FIG. 2; the remainder of the tubes and their control circuits are identical to those illustrated.

Each anode control circuit 21 comprises: a PNP transistor designated Q_1 ; first and second resistors designated R_1 and R_2 ; a capacitor designated C_1 ; and, a diode designated D_1 . R_1 is connected between the emitter and the base of Q_1 . The base of Q_1 is also connected to one side of C_1 and to the cathode of D_1 . The other side of C_1 is connected through R_2 to a bias source designated V_1 . The junction between C_1 and R_2 is connected to an input terminal 29, said input terminal being connected to one of the outputs of the column count decoder as hereinafter described.

Each display tube circuit 23 comprises a display tube (such as a Nixie tube) designated T having its anode connected to the collector of Q_1 .

Each cathode control circuit 25 comprises: a NPN transistor designated Q_2 ; a resistor designated R_3 ; and, a three input NAND gate designated A_1 . The three inputs of A_1 are connected to the signal outputs of the memory register 17 illustrated in FIG. 1. The output of A_1 is connected to the emitter of Q_2 . The base of Q_2 is connected through R_3 through a bias source designated V_2 . The collector of Q_2 is connected to the same numerical cathode terminal of all of the display tubes. Hence, when Q_2 of any one of the cathode control circuits is energized, it applies power to a common numerical cathode of each of the display tubes. As is well known in the art, each cathode controls the energization of one of the numerical indicia elements contained in the tube.

The decimal point control circuit 27 illustrated in FIG. 2 comprises: a NPN transistor designated Q_3 ; a resistor designated R_4 ; a rotary switch designated S_1 ; a simple switch designated S_2 ; and, a single input NAND gate designated A_2 . Preferably, S_1 is a rotatable switch having a common terminal connected to a wiper arm and a plurality of separate or individual terminals adapted to be selectively contacted by the wiper arm. S_2 is a simple open and close, single pole switch.

The input of A_2 is connected through S_2 to ground. The base of Q_3 is connected through R_4 to a suitable bias source designated V_4 . The emitter of Q_3 is connected to the output of

A_2 . The collector Q_3 is connected to the common terminal of S_1 . The individual terminals of S_1 are connected to the decimal point indicia cathodes of the display tubes. Hence, when S_1 is switched to a particular position, it will ignite the decimal point indicia of the tube connected to that switch position if S_2 is open.

The circuit illustrated in FIG. 2 also comprises three additional resistors designated R_5 , R_6 , and R_7 ; a plurality of tube diodes designated D_2 ; a decimal point diode designated D_3 ; a pair of source diodes designated D_4 and D_5 ; and a Zener diode designated DZ . One end of R_5 is connected to the Q_1 emitters, and the other end of R_5 is connected through R_6 to a bias source designated V_5 . The junction between R_5 and R_6 is connected through D_4 , D_5 , R_7 and DZ connected in that order in series to ground. The anodes of D_4 and D_5 are nearest V_5 and the anode of DZ is connected to ground. The junction between D_5 and R_7 is connected to the anodes of the diodes D_1 . The anodes of the diodes D_2 are separately connected to the collectors of the transistors Q_2 of the cathode control circuits. The anode of D_3 is connected to the collector Q_3 . The cathodes of the diodes D_2 and D_3 are connected together and to the junction between R_7 and DZ . The junction between R_7 and DZ is also connected to a voltage terminal designated V_6 .

With the transistor configuration illustrated in FIG. 2, it will be appreciated by those skilled in the art and others that all voltage sources are positive and that the potential at voltage terminal V_6 is positive. The main voltage source is V_5 ; that is, V_5 is the largest voltage source and other voltage sources necessary to operate the circuit, can be derived from V_5 . For example, the voltage at terminal V_6 is derived from the voltage V_5 . The value of V_6 is determined by the value of DZ and, preferably, the V_6 voltage is equal to the voltage requirements of V_1 , and is connected thereto. The voltage requirements of V_2 , V_3 and V_4 are somewhat less than V_6 , and can be derived by reducing the V_5 voltage to appropriate levels in a manner similar to the derivation of the V_6 voltage.

The V_5 voltage is, in prior art circuits, regulated prior to being applied to the anodes of the display tubes. However, in accordance with this invention, V_5 is unregulated. In fact, V_5 can fluctuate 10 percent or 15 percent of its nominal value. The reason V_5 can fluctuate is that its fluctuations have no effect on the current operation of Q_1 . That is, D_4 , D_5 and D_1 provide a constant voltage across the Q_1 base-emitter electrodes and R_5 when Q_1 is pulsed. Because the Q_1 base-emitter voltage can be considered constant, the remaining voltage across R_5 and the current through R_5 is also constant. Since most of the current passing through R_5 goes into the emitter at Q_1 , the emitter current and, for all practical purposes, the collector current of Q_1 , are constant. More specifically, when Q_1 is pulsed on, it remains out of saturation with its current controlled by the voltage across R_5 . This constant current is applied to the display tubes T.

Because Q_1 provides a constant current to the display tubes T, they do not receive either an overcurrent or an undercurrent. It will be appreciated that an overcurrent would reduce the life of the display tubes by destroying their elements while an undercurrent would reduce the intensity of the light emitted by the elements of the tubes.

It will also be appreciated that, because the constant current generator circuit R_5 and Q_1 requires a voltage drop of only three diodes D_4 , D_5 and D_1 , V_5 need only be a small amount above the required tube potential. The voltage drop across R_6 can be essentially neglected because that resistor is a low voltage resistor and is merely included to protect the circuit from high current in the event of a Q_1 failure. Also, because V_5 is a lower voltage, Q_1 can be a lower voltage transistor than would be required if V_5 were required to be larger.

Turning first to the operation of the decimal point circuit 27, essentially A_2 is an inverter, hence, if S_2 is closed, V_3 is applied to the emitter of Q_3 and biases Q_3 off. If S_2 is open, the emitter of Q_3 is grounded and Q_3 passes current. Therefore, if it is desired that a decimal point be included in the indicia to be displayed, S_2 is opened. When S_2 is opened, a decimal point

is displayed on the display tube, T, connected to the individual contact intersecting the wiper arm of S_1 . It should be noted, that any tube, T, can display both a decimal point and a number at the same time. However, both displays will only occur when the anode is energized and the decimal point and number electrodes are also energized. The decimal point electrode is energized as just discussed.

The numerical electrodes are energized by the memory register 17 (FIG. 1) generating a binary code representing a numerical value. This code is recognized by one of the A_1 gates. That gate grounds the emitter of its transistor Q_2 . When the emitter Q_2 is grounded, it is turned on and passes current, and this current energizes one of the numerical electrodes of all of the tubes. The same numerical electrode is energized whether it be 0, 1, 2 or any other number up to 9. The tube that actually displays the number is determined by the energization of the anode control circuits.

The tube anodes are energized by the output signals from the column count decoder. The column count decoder applies a voltage to one of the terminals 29, the exact terminal being determined by the signals applied to the column count decoder by the column control counter. The energized terminal applies a voltage through its respective capacitor C_1 to its respective transistor Q_1 . This voltage energizes Q_1 and its associated display tube T. At this point both an electrode and the anode of a particular display tube are energized, hence, that display tube displays the chosen number. In addition, if S_1 is coupled to the same display tube and S_2 is open, that display tube also displays a decimal point.

FIG. 3 illustrates a column count decoder suitable for use with the invention and comprises 10 NPN transistors designated Q_4 through Q_{13} ; nine diodes designated D_6 through D_{14} ; and eight resistors designated R_8 through R_{15} . Eight input terminals are illustrated on the left of FIG. 3 and are adapted to receive signals from the column control counter. Preferably, the column control counter generates a 4-bit binary code. The eight input terminals receive the 4-bit signals and the complements of the 4-bit signals. For ease of discussion, the input terminals for the 4-bit signals are designated in FIG. 3 as X_1 through X_4 and input terminal for the complements are designated as $\bar{X}_1$ through $\bar{X}_4$. Hence, each of the eight input terminals receives either an X or an $\bar{X}$ signal.

The X_1 terminal is connected through R_{12} to the emitters of Q_9 through Q_{13} . The $\bar{X}_1$ terminal is connected through R_{13} to the emitters of Q_4 through Q_8 . R_{14} is connected in series with R_{15} between the emitters of Q_4 through Q_8 and the emitters of Q_9 through Q_{13} . The junction between R_{14} and R_{15} is connected to a bias source designated V_7 .

The X_2 terminal is connected to the cathodes of D_{13} and D_{14} and the $\bar{X}_2$ terminal is connected to the cathodes D_{11} and D_{12} . The X_3 terminal is connected to the cathodes of D_9 and D_{10} and the $\bar{X}_3$ terminal is connected to the cathodes of D_7 and D_8 . The $\bar{X}_4$ terminal is connected to the cathode of D_6 . The X_4 terminal is connected to the bases of Q_4 and Q_9 . The anodes of D_6 and D_7 are connected to the bases of Q_5 and Q_{10} . The anodes of D_8 and D_9 are connected to the bases of Q_6 and Q_{11} . Similarly, the anodes of D_{10} and D_{11} are connected to the bases of Q_7 and Q_{12} , and the anodes of D_{12} and D_{13} are connected to the bases of Q_8 and Q_{13} . The anode of D_{14} is connected to the bases of Q_5 and Q_{10} .

The anodes of D_{10} and D_{11} are also connected through R_8 to a voltage source designated V_8 . The anodes of D_{12} and D_{13} are connected through R_9 to V_8 , and the anodes of D_{14} and D_{15} are connected through R_{10} to V_8 . Also, the anodes of D_{16} and D_{17} are connected through R_{11} to V_8 . V_7 and V_8 are both positive for the transistor-diode polarity illustrated in Fig 3. The collectors of each of the transistors Q_4 through Q_{13} are separately connected to a plurality of output terminals that are adapted for connection through the capacitors C_1 to the transistors Q_1 of the anode drive circuits illustrated in FIG. 2.

The column count decoder merely decodes the signal from the column control counter and applies sequential signals to its output terminals. The sequence of the output signals is

determined by the sequence of the coded signal received from the column control counter.

The following is a table setting forth which transistor is on and generating an output signal for a particular binary sequence of input signals for the column count decoder illustrated in FIG. 3:

X_4	X_3	X_2	X_1	Transistor
0	0	0	0	Q_{10}
0	0	0	1	Q_5
0	0	1	0	Q_{11}
0	0	1	1	Q_6
0	1	0	0	Q_{13}
0	1	0	1	Q_8
0	1	1	0	Q_{12}
0	1	1	1	Q_7
1	0	0	0	Q_9
1	0	0	1	Q_4

It is evident from the table that as the count in the column control counter advances from binary 0 to the binary equivalent of 9, the column count decoder sequentially produces an output signal at each of its 10 outputs. Because these output signals are connected to the anode control circuits 21 of the drive circuit illustrated in FIG. 2, the anode control circuits are sequentially energized when the foregoing code sequence is applied to the column count decoder by the column control counter. It will be understood that the tube sequence is connected so that the tubes read from left to right to provide a number that can be viewed in the usual manner. After one sequence is complete, the column control counter senses the completion and recycles so that a continuous sequence of control signals is applied to the anode control circuits. Since the signals from the memory register are repetitively applied to the gates A_1 of FIG. 2 in synchronism with the signals from the memory register, it is evident that each display tube is repetitively energized. However, the rate of flicker is so great that it cannot be perceived by the human eye.

It will be appreciated from the foregoing description of the invention that an uncomplicated apparatus for driving a plurality of display tubes is provided. A column control counter generates a code that is decoded by a column count decoder. The decoder applies sequential control signals to anode control circuits connected to the display tubes, the control sequence being determined by the code signals applied to the decoder by the counter. Hence, tube control is provided. In addition, indicia control data is "readout" from a data source and controls the indicia electrodes of the tubes through an uncomplicated electrode control circuit. Therefore, both indicia and tube control is provided.

Because the anode control circuits are a constant current source for the anodes of the tubes, the life of the tubes is not reduced nor is the intensity of the tubes indicia reduced. The anode current is constant regardless of fluctuations.

The invention also provides means for selectively adding a decimal point to the indicia displayed on the tubes. That is, if the indicia are numbers of a decimal point can be added if desired to "point off" the number. And, the decimal point can be selectively inserted at any point in the sequence of numbers.

While the foregoing disclosure has described a preferred embodiment of the invention, it will be appreciated that certain changes can be made within the scope of the invention. For example, NPN transistors can be placed by PNP transistors and vice versa. Of course, appropriate bias changes must be made, and the polarity of the diodes must be changed to compensate for the transistor changes. In any event, the invention can be practiced otherwise than as specifically described herein.

What is claimed is:

1. In a data display system that comprises a plurality of data display tubes, each data display tube having at least one selectively energizable anode and a plurality of selectively energizable cathodes, an apparatus for limiting the current applied to the selectively energized anodes to a constant level when the anodes are energized, said apparatus comprising:

a plurality of current control transistors, each of said current control transistors having its emitter-collector terminals connected between an anode potential source and an anode of one of said plurality of data display tubes, the base of each of said current control transistors connected so as to be selectively energizable by a control voltage and thereby control the selective energization of the anodes of said plurality of data display tubes; and, a single voltage limiting diode connected to the bases of all of said plurality of current control transistors to limit the level of the control voltage applied to the bases of said plurality of current control transistors to a constant level.

2. Apparatus as claimed in claim 1 wherein said voltage limiting diode is a zener diode.

3. Apparatus as claimed in claim 2 wherein said current control transistors are PNP transistors having their collectors directly connected to said anodes.

4. Apparatus as claimed in claim 3 including a plurality of diodes, one of said plurality of diodes being connected between said zener diode and the base of each of said plurality of PNP transistors; and including a further diode connected between said anode potential source and said zener diode.

5. Apparatus as claimed in claim 4 including a plurality of series connected resistor-capacitor circuits, one of said circuits being connected to each of said plurality of PNP transistors so that the outer end of the resistor is connected to the emitter of the associated PNP transistor, the junction between the resistor and capacitor is connected to the base of the associated PNP transistor and the outer end of the capaci-

tor is connected to the control voltage that selectively energizes the associated PNP transistor; and including a further resistor connected between said anode potential source and the emitters of all of said PNP transistors.

6. Apparatus as claimed in claim 1 wherein said current control transistors are PNP transistors having their collectors directly connected to said anodes.

7. Apparatus as claimed in claim 1 including a plurality of diodes, one of said plurality of diodes being connected between said voltage limiting diode and the base of each of said plurality of current control transistors; and including a further diode connected between said anode potential source and said voltage limiting diode.

8. Apparatus as claimed in claim 1 including a plurality of series connected resistor-capacitor circuits, one of said circuits being connected to each of said plurality of current control transistors so that the outer end of the resistor is connected to the emitter of the associated current control transistor, the junction between the resistor and capacitor is connected to the base of the associated current control transistor and the outer end of the capacitor is connected to the control voltage that selectively energizes the associated current control transistor; and including a further resistor connected between said anode potential source and the emitters of all of said current control transistors, the collectors of said current control transistors being directly connected to said anodes.

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