United States Patent [19]

Marz

[11] **3,762,152**

[45] **Oct. 2, 1973**

[54] **RESET SYSTEM FOR DIGITAL ELECTRONIC TIMEPIECE**

[75] Inventor: **Frank H. Marz,** Delavan, Wis.

[73] Assignee: **Bunker Ramo Corporation,** Oak Brook, Ill.

[22] Filed: **Dec. 8, 1971**

[21] Appl. No.: **205,970**

[52] **U.S. Cl.** ..... **58/23 R,** 58/50 R, 58/85.5

[51] **Int. Cl.** **G04c 3/00,** G04b 19/30

[58] **Field of Search** ..... 58/23 R, 23 A, 23 AC, 58/34, 50, 85.5; 235/92 T; 340/309.4

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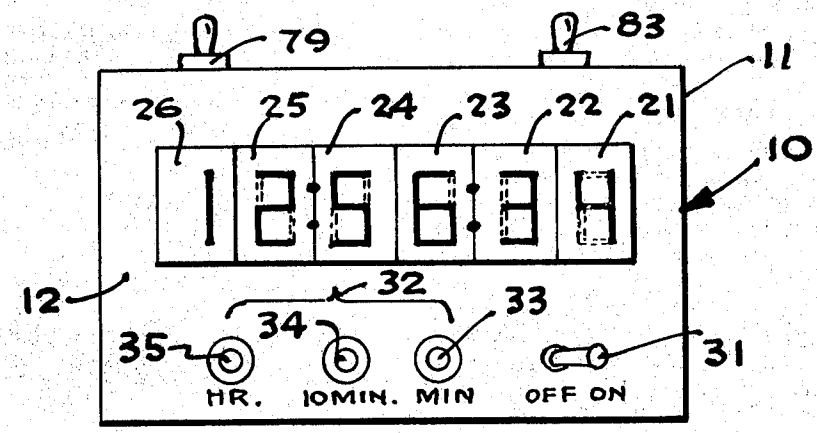
Primary Examiner—Richard B. Wilkinson
Assistant Examiner—Edith C. Simmons Jackmon
Attorney—Frederick M. Arbuckle

[57] **ABSTRACT**

A reset system for a digital electronic clock of the multi-stage countdown type, comprising a zero reset switch connected to the seconds stages of the clock to set and hold both at zero without disturbing the other clock stages, and separate reset switches for supplying a one hertz reset signal directly to the minutes and hours stages, on a selective basis, to set those stages as desired. Provision is also made for high speed setting of the various stages of the clock.

9 Claims, 2 Drawing Figures



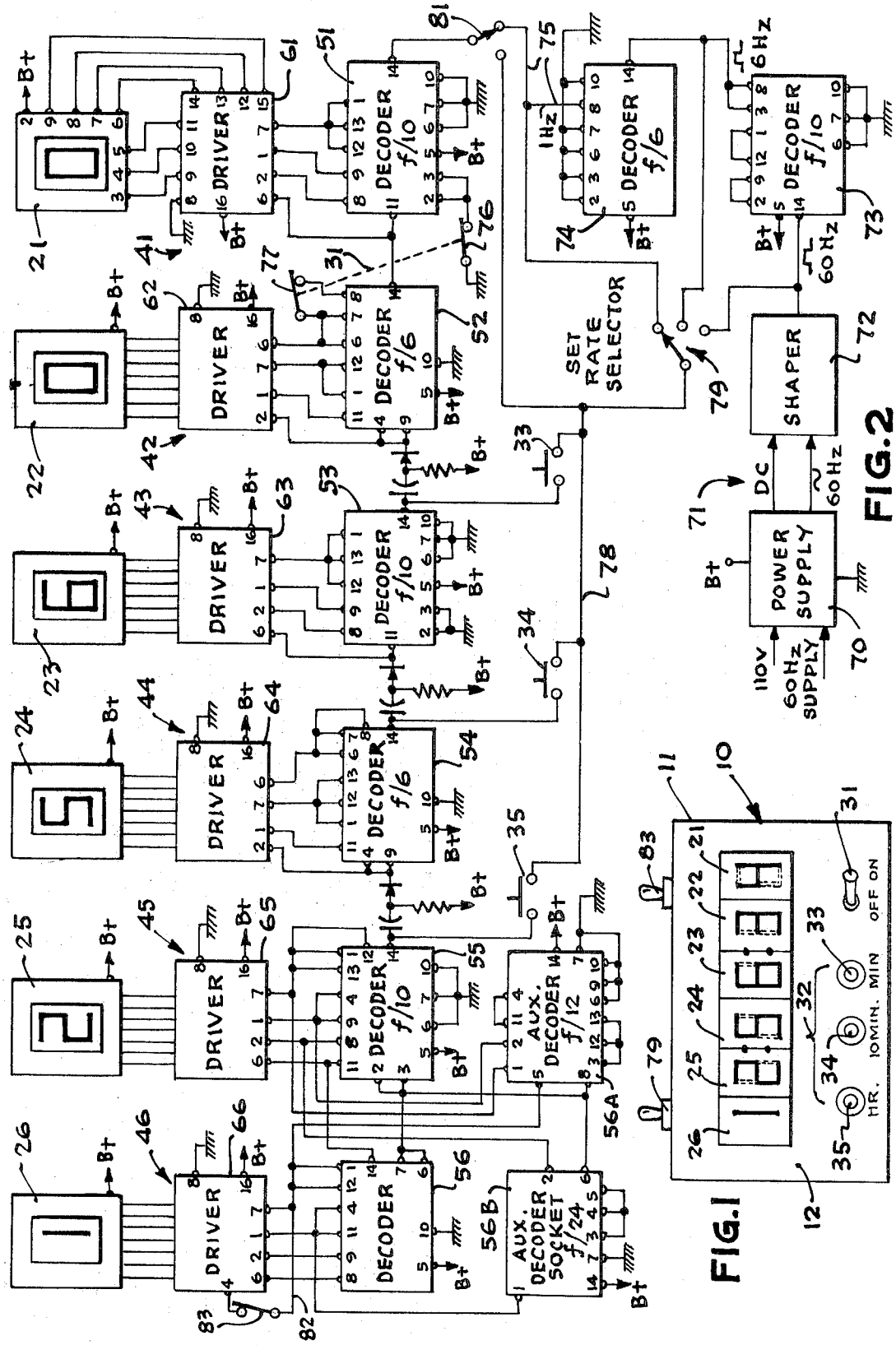

B+
DRIVER
DECODER f/10
DECODER f/6
AUX. DECODER f/12
AUX. DECODER SOCKET f/24
SET RATE SELECTOR
SHAPER
POWER SUPPLY
110V 60Hz SUPPLY
DC
60Hz
1Hz
6Hz
HR. 10MIN. MIN
OFF ON

FIG.2

FIG.1

RESET SYSTEM FOR DIGITAL ELECTRONIC TIMEPIECE

BACKGROUND OF THE INVENTION

Digital electronic clocks and other digital timepieces are expanding in use, both in business and technical applications and in domestic situations. Usually, a timepiece of this kind comprises a series of individual displays for seconds, minutes, and hours, with each display of a higher order being driven by an output signal from the next lower order display. The entire clock is actuated by a single input signal of stable frequency, ordinarily a one hertz signal, which is usually derived from the stable 60 hertz supply afforded by a public utility.

A number of different systems have been proposed for setting and resetting of digital electronic timepieces. Most frequently, an arrangement is provided for applying a high frequency signal to the clock input so that the clock cycles rapidly. When the desired setting is reached, the high frequency input is cut off and the normal low frequency input is resumed. A system of this kind is shown in Langley U.S. Pat. No. 3,485,033. In some systems, a stop switch is provided that permits limited resetting by simple delay in operation, when the clock is fast, an arrangement of this kind being shown in Walton U.S. Pat. No. 3,576,099. Some commercial clocks have also provided for resetting of the clock by applying a high speed setting signal each clock stage.

In all of these systems, there has been some difficulty in obtaining an accurate and prompt setting of the clock, particularly when the clock is to be reset in synchronism with a time signal from a radio or other source. If relatively low frequency signals are used for clock setting, the setting process may take an inordinate amount of time. If high frequency setting signals are utilized, on the other hand, the possibility of an over-run in the setting operation is increased. This may require substantial recycling of a major part of the clock, since reverse setting is not practical with devices of this kind.

SUMMARY OF THE INVENTION

It is a principal object of the present invention, therefore, to provide a new and improved reset system for a digital electronic timepiece that inherently eliminates or minimizes the disadvantages of previously known systems and that provides for substantially greater flexibility and versatility in setting of the clock.

A specific object of the invention is to provide a new and improved reset system for a digital electronic timepiece that allows individual resetting of the lower order stages, usually the seconds stages, at zero level without changing the recorded counts in the other stages of the timepiece.

A further object of the invention is to provide a new and improved reset system for a digital electronic clock that effectively minimizes the possibility of an overrun in setting of the clock and that also provides for convenient correction in the event that an overrun occurs.

An additional object of the invention is to provide a new and improved reset system for a digital electronic timepiece that affords versatile operation, yet simplifies the required electronic circuitry and provides for a reduction in the overall cost of the timepiece.

Accordingly, the invention relates to a reset system for a digital electronic timepiece of the kind comprising a series of individual displays for time intervals of successively higher order, each display including a frequency-divider decoder register for driving the display and for supplying an actuating signal to the decoder register in the display of the next higher order, the clock further comprising a base signal source for developing a base signal of suitable frequency and a base signal input circuit for applying the base signal to the decoder register of the first order display, usually the seconds display. The reset system of the invention comprises first reset switching means, connected to the first order display decoder, for setting the first order display to zero and simultaneously inhibiting transmission of actuating signals to the succeeding displays in the timepiece. In an ordinary clock, the first reset switching means is preferably connected to both the seconds display and the 10 seconds display and is effective to set both to zero. The reset system further comprises second reset switching means connected to the base signal input circuit and to the decoder registers in the higher order displays of the timepiece. The second reset switching means, which may comprise a plurality of momentary contact switches, is employed to apply the base signal directly to each higher order display decoder register, on an individual basis, to set each of the higher order displays.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a front elevation view of a digital electronic clock constructed in accordance with one embodiment of the present invention; and

FIG. 2 is a block diagram, partially schematic, of the operating circuit for the clock illustrated in FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIGS. 1 and 2 illustrate a digital electronic clock **10** which includes a reset system constructed in accordance with the present invention. Clock **10** comprises a housing **11** (FIG. 1) with a face plate **12**. A series of readout elements **21, 22, 23, 24, 25** and **26** are mounted in face plate **12**, arranged from right to left in ascending order of time intervals. Thus, the readout element **21** affords a numerical display indicative of seconds, the readout element **22** shows ten second intervals, the readout on device **23** is in terms of minutes, and the readout device **24** displays ten minute intervals. The readout devices **25** and **26** afford a reading of hours.

Clock **10** includes a first reset switching means comprising a reset switch **31**, shown as a toggle switch; other switch constructions can be employed. Clock **10** further comprises second reset switching means **32** including three individual pushbutton switches **33, 34,** and **35**. The first reset switch **31** is normally maintained in its "on" position as shown in FIG. **1**. When actuated to and held in its alternate "off" position, switch **31** resets the two seconds displays, comprising the readout devices **21** and **22**, to zero, and simultaneously interrupts operation of the clock. This first reset is particularly convenient in setting clock **10** in synchronism with a time signal from an external source, such as a radio. As long as switch **31** is held "off", the clock does not change its count; when reset switch **31** is released to return to its "on" position, the clock immediately resumes its count from a zero seconds base, coordinating the seconds portion of the clock with the time signal.

The pushbutton switch 33 in the second reset switching means 32 is used for selective individual resetting of the minutes display of clock 10. Similarly, pushbutton switch 34 resets only the ten minute stage of clock 10, comprising readout device 24. Pushbutton 35, on the other hand, is connected to the hours stage of clock 10 and is utilized to set and to reset the display that comprises readout device 25. There is no necessity for a separate reset for the decimal hours display comprising readout device 26; a single reset control for the hours portion of the clock is adequate.

FIG. 2 affords a detailed illustration of an operating circuit arrangement for clock 10. As shown therein, the seconds readout device 21 is a part of a first order display 41 that includes a frequency-divider decoder register 51 and a readout driver 61. The next higher order display 42 in clock 10 comprises the decimal second readout 22 actuated by a driver circuit 62 which is in turn controlled by a decoder 52, the input signal to decoder 52 being derived from the decoder 51 in the preceding lower order stage. This construction is carried forward through the clock, affording succeeding stages 43, 44 and 45 which include decoder registers 53, 54 and 55 controlling driver circuits 63, 64 and 65 respectively. In each display, the frequency-divider decoder register actuates the display and also supplies an actuating signal to the decoder register in the display of the next higher order.

The final display 46 of the clock 10 is of similar but slightly different construction. It includes the decimal hours readout device 26 actuated by a driver circuit 66. Driver circuit 66 is actuated by signals from a decoder 56, similar to decoders 52 and 54, to which an auxiliary decoder 56A is connected for use in a twelve hour clock. As indicated in FIG. 2, multiple interconnections are required between the decoder register 56, 56A and the decoder 55 in the preceding stage, since the decimal hours readout 26 operates on a somewhat different ratio than any of the other stages.

For the illustrated circuit, each of the decoder registers 51–56 may be constructed with individual transistors or like circuit elements in accordance with known shift register circuits. Preferably, however, integrated circuits of the TTL (transistor/transistor logic) type are employed. Specifically, the decoder registers 51,53 and 55 may be type 7490 TTL circuits, registers 52, 54 and 56 type 7492 circuits, and auxiliary decoder 56A a type 7400 circuit. Drivers 61–66 are selected to meet the needs of readout devices 21–26; if seven-element incandescent "Numitron" display tubes are used as the readout devices, type 7441 integrated circuits will serve as the drivers. FIG. 2 includes the pin connections for these specific TTL circuits, using the pin designations shown in the TTL Integrated Circuit Data Book of Motorola Semiconductor Products, Inc., First Edition, 1971.

As shown in FIG. 2, clock 10 further comprises a base signal source 71 for developing a base signal of stable frequency to be utilized in operation of the clock. The base signal source 71 includes a power supply 70 affording D.C. outputs and a 60 hertz output driven from a conventional 60 hertz sinusoidal power source. The succeeding stage 72 of signal source 71 may comprise a conventional wave-shaping circuit for developing an output pulse signal of rectangular waveform at the 60 hertz frequency. A conventional Schmitt trigger circuit may be utilized for the shaper 72; alternatively, for a less expensive construction, a rectifier-limiter circuit may be utilized.

The 60 hertz pulse output from shaper circuit 72 is supplied to a frequency divider 73 which reduces the signal frequency by a factor of ten. The frequency divider 73 may be an integrated circuit of the TTL type, specifically a type 7490 circuit. The output from frequency divider 73 is a 6 hertz pulse signal that is applied to a second frequency divider 74 having a division factor of six. The output signal from frequency divider 74 is a 1 hertz pulse signal that constitutes the base signal for operation of clock 10. Assuming a steady and stable power supply input signal to shaper 72, it will be seen that the base signal output from frequency divider 74 has the necessary stability for effective clock operation. The base signal from frequency divider 74 is applied to the input of the first stage decoder register 51 by a base signal input circuit 75.

Clock 10, as thus far described, is entirely conventional in operation. The base signal supplied from frequency divider 74 to decoder 51 through circuit 75 drives decoder register 51 directly at a one hertz rate. Decoder 51 supplies the necessary output signals to driver 61 to change the illuminated display on readout device 21 once every second. Each time a complete cycle of ten seconds has been recorded in the decoder register 51, that register recycles, starting a new count and supplying an output signal to the next higher stage decoder register 52. That is, the output signal from decoder 51 to decoder 52 has a frequency of 0.1 hertz, a new actuating pulse recurring every 10 seconds. Decoder 52 recycles for each six input pulses, triggering driver 62 on each input pulse to change the numerical display on readout device 22 and also supplying an actuating signal to the next higher stage decoder 53 at the end of each cycle. The same process is continued through the higher stages of clock 10, affording a continuing and accurate operation for the timepiece.

If even minor variations occur in the frequency of the input signal to clock 10, or if there is any momentary power interruption, it may be necessary or desirable to reset the clock. It is the reset system for clock 10 that constitutes the subject matter of the present invention.

As noted above, clock 10 includes a first reset switching means for setting the first order or seconds display 41 to zero and simultaneously inhibiting transmission of actuating signals to the succeeding higher order displays in the clock. As shown in FIG. 2, this first reset switching means comprises the switch 31, which is a two-pole normally closed momentary-action switch. The first pole 76 of switch 31 is connected to a reset circuit for the decoder register 51 in the first display 41 of the clock, and is returned to system ground. Using a type 7490 integrated circuit register, the reset switch connection is made to the "zero" reset circuit, pins 2 and 3. The second pole 77 of reset switch 31 is connected to decoder register 52; for a type 7492 register the connection is made from pins 6, 7 to pin 8. In normal operation, switch 31 remains closed as illustrated in FIG. 2.

Whenever switch 31 is actuated, however, opening the two switch poles 76 and 77, the two decoders 51 and 52 are both effectively reset to zero, actuating the associated driver circuits 61 and 62 that control the readout devices 21 and 22 so that a zero is displayed on each of the first two readouts. Furthermore, transmission of actuating signals to the succeeding stages of

clock 10 is inhibited because the first order display decoder register 51 is reset to and maintained at its zero setting and all succeeding stages are dependent upon an output of actuating signals from stage 41 to stage 42, which cannot now occur. Thus, operation of the clock is interrupted until switch 31 is returned to its original closed condition. Moreover, the settings of displays 23 through 26 do not change.

This mode of operation is particularly useful in setting clock 10 into exact synchronism with a received time signal, since switch 31 can be actuated to open condition and then released immediately upon receipt of a time tone or other like signal, restoring clock 10 to operation with the seconds displays both starting from zero. Furthermore, the actuation of switch 31 does not alter the operating conditions for any of the higher order stages 43–46 of the clock, a substantial convenience in setting the clock in exact synchronism with a time signal.

The reset system of clock 10 further comprises a second reset switching means 32 including the pushbutton switches 33, 34 and 35. Each of these switches is a normally open momentary-contact switch; other mechanical switch constructions could be used, if preferred, instead of pushbutton structures.

Switch 33 is electrically connected to the input stage of the decoder register 53 in the minutes display 43 (pin 14 in a type 7490 register) and is also connected to a conductor 78. Similarly, switch 34 is connected from conductor 78 to the input stage in the decoder register 54 and switch 35 is connected from conductor 78 to the input stage in the decoder register 55. Conductor 78 is connected, through a three-position selector switch 79, to the base signal input circuit 75. Switch 79 is normally maintained in the position shown in FIG. 2 but can be displaced to two alternate switching positions, as described more fully hereinafter.

In a given instance, it may happen that the 10-minute display readout 24 shows the numeral 4, when it should display a 5 as illustrated in FIG. 2. To reset the readout device 24 of display 44 to the correct value, switch 34 is closed long enough to supply a single pulse signal to decoder 54 and advance the count in the decoder by one. Since the input signal supplied to decoder 54 through switch 34 is the 1 hertz base signal from input circuit 75, the display 44 will be advanced the desired single count in a time interval of 1 second or less. If a greater increase in the count is necessary, switch 34 is maintained closed long enough to make the requisite correction.

In the same manner, reset switch 33 can be closed to correct the number appearing in readout device 23 of minutes display stage 43. Moreover, closing of switch 35 supplies the one hertz base signal as a reset signal to decoder 55 and can be used similarly to correct the hours displays 45 and 46. In no instance is the complete clock setting cleared; any error in setting is corrected at the level at which it appears without affecting any lower order stage in the clock. It may happen that a resetting of one stage, such as the minutes display 43, may run that display through a cycle point that produces an actuating signal to the next higher order display, in this instance display 44. In such an event, it is a simple matter to correct the next higher order display and thus complete the resetting of the entire clock.

The reset system for clock 10, as thus far described, is quite adequate for most applications. In some instances, however, particularly when frequent resetting of the clock is likely to be necessary, it may be desirable to equip the clock with a reset that operates more rapidly. To this end, the 6 hertz outlet signal from frequency divider 73 may be connected to one of the normally open input terminals of selector switch 79 and the 60 hertz pulse signal from shaper 72 may be applied to the other normally open input contact of switch 79. With this arrangement, switch 79 can be adjusted to select either a 6 hertz reset signal or a 60 hertz reset signal for actuation of displays 43, 44 and 45, using the intermediate stages of base signal source 71 as a high speed reset signal source. Thus, if the set rate selector switch 79 is adjusted to connect the output of frequency divider 73 to conductor 78, any of the clock displays 43–45 may be reset at a rate of six numeral changes per second instead of the one numeral change per second rate afforded when selector switch 79 is in its home position. For extremely rapid reset operation, the 60 hertz output from shaper 72 is utilized, although resetting at this high rate is normally unnecessary, particularly since it materially increases the chance of an overrun, and hence makes accurate setting rather difficult.

The rapid reset arrangement may also be employed in connection with displays 41 and 42, independently of the zero reset function provided by switch 31 and described in detail above. Thus, a single-pole double-throw switch 81 may be connected in series in the base signal input circuit 75. Normally, switches 79 and 81 are maintained in the illustrated positions so that the one hertz base signal from frequency divider 74 is applied to the input of the decoder register 51 in the seconds display 41. However, if switch 81 is actuated to its alternate position, and selector switch 79 is set to either of its two alternate positions, a high speed reset signal is supplied to the decoder register 51, affording a rapid reset operation for the 2 seconds displays 41 and 42.

In accordance with known practice, the decoder register 56 and driver 66 in display 46 may be provided with a connection to suppress the zero that would normally be displayed by device 26 throughout much of the day. This external circuit is illustrated by the circuit 82 in FIG. 2. A switch 83 may be incorporated in the zero suppression circuit 82 to permit the clock user to adjust the clock for displaying the zero if desired by opening switch 83.

It is also a relatively simple matter to construct clock 10 for operation as a 24 hour clock instead of a 12 hour clock. To this end, an additional auxiliary decoder socket 56B is incorporated in the 10-hours display 46 and is connected to the main decoder 56 of stage 46 and to the decoder register 55 in the preceding stage 45 with connections to afford appropriate decoding for 24 hour operation. To convert clock 10 to a 24 hour basis, it is only necessary to remove the auxiliary decoder register 56A from its normal position and replace it in the alternate socket 56B; switch 83 must also be opened, using TTL circuits of the types described above.

The reset switching system incorporated in clock 10 also makes it possible to use the clock as a high-accuracy timer. For this purpose, switch 79 may be set to connect the 60 hertz output of shaper 72 to conductor 78 and switch 81 may be set to connect the input of decoder 51 to conductor 78. With these switch settings, display 21 (ordinarily the seconds display) will read in increments of 1/60 second, display 22 reads in

1/6 second units, display **23** shows seconds, display **24** reads in 10-second units, and displays **25** and **26** actually show minutes up to a total of 12 or 24 minutes, depending on whether the auxiliary decoder is used in position **56A** or position **56B**. For use as a high-accuracy (1/60 second) timer, in this manner, switches **79** and **81** should be maintained-contact devices.

In order to afford a more complete disclosure of one embodiment of the invention, specific circuit parameters have been set forth hereinafter for a clock that uses the TTL circuits and other components described above. It should be understood that all specific components and parameters included in this specification are provided solely for purposes of illustration and in no sense as a limitation on the invention.

B+ — +5 volts D.C.
Interstage Coupling Capacitors 0.01 microfarad
Interstage Diodes 1N914
Interstage Shunt Resistors 4 kilohms

I claim:

1. A reset system for a digital electronic timepiece of the kind comprising a series of individual displays for time intervals of successively higher order, each display including a frequency-divider decoder register for driving the display and for supplying an actuating signal to the decoder register in the display of the next higher order, said timepiece further comprising a base signal source for developing a base signal of stable frequency, and a base signal input circuit for applying the base signal to the decoder register in the first order display, said reset system comprising:

first reset switching means, connected to the first order display decoder register, actuation of said first reset switching means setting said first order display to zero, regardless of the condition of said display at the instant said first reset switching means is actuated, and simultaneously inhibiting transmission of actuating signals to the succeeding displays in said timepiece;

and second reset switching means, connected to said base signal input source and to the decoder registers in the higher order displays of said timepiece, for applying said base signal directly to each higher order display decoder register, individually, to advance the higher order displays.

2. A reset system for a digital electronic timepiece, as set forth in claim **1**, in which said first reset switching means is connected to the decoder registers in both the first and second order displays to set both to zero without changing any of the higher order displays.

3. A reset system for a digital electronic timepiece, as set forth in claim **2**, in which said first reset switching means comprises a two-pole normally closed momentary-actuation switch, each pole individually connected to a single stage in a respective one of the decoder registers in said first and second order displays.

4. A reset system for a digital electronic timepiece of the kind comprising a series of individual displays for time intervals of successively higher order, each display including a frequency-divider decoder register for driving the display and for supplying an actuating signal to the decoder register in the display of the next higher order, said timepiece further comprising a base signal source developing a base signal of stable frequency, and a base signal input circuit for applying the base signal to the decoder register in the first order display, said reset system comprising:

first reset switching means, connected to the first and second order display decoder registers, actuation of said first reset switching means setting said first and second order displays to zero regardless of the condition of said displays at the instant said first reset switching means is actuated, and simultaneously inhibiting transmission of actuating signals to the succeeding displays in said timepiece;

second reset switching means, connected to said base signal input circuit and to the decoder registers in the higher order displays of said timepiece, for applying said base signal directly to each higher order display decoder register, individually, to advance the higher order displays, said second reset switching means comprising a plurality of momentary-actuation normally open reset switches, each connected from said base signal input source to a single stage of a respective one of said higher order decoder registers,

a reset signal source developing a high-speed reset signal having a frequency substantially higher than said base signal frequency, and

a set rate selector switch, for connecting said reset switches to either said base signal circuit for resetting at a normal rate or to said reset signal source for resetting at a high speed rate.

5. A reset system for a digital electronic timepiece of the kind comprising a series of individual displays for time intervals of successively higher order, each display including a frequency-divider decoder register for driving the display and for supplying an actuating signal to the decoder register in the display of the next higher order, said timepiece further comprising a **1** Hertz base signal source developing a base signal of stable frequency, and a base signal input circuit for applying the base signal to the decoder register in the first order display, said reset system comprising:

first reset switching means, connected to the first and second order display decoder registers, actuation of said first reset switching means setting said first and second order displays to zero and simultaneously inhibiting transmission of actuating signals to the succceeding displays in said timepiece;

second reset switching means, connected to said base signal input source and to the decoder registers in the higher order displays of said timepiece, for applying said base signal directly to each higher order display decoder register, individually, to advance the higher order displays,

a 60 Hertz signal source, and

switch means for connecting the first order display to said 60 Hertz signal source for operation of said timepiece as a high-accuracy timer.

6. A reset system for a digital electronic timepiece of the kind comprising a series of individual displays for time intervals of successively higher order, each display including a frequency-divider decoder register for driving the display and for supplying an actuating signal to the decoder register in the display of the next higher order, said timepiece further comprising a base signal source for developing a base signal of stable frequency, and a base signal input circuit for applying the base signal to the decoder register in the first order display, said reset system comprising:

control means included in at least said first order decoder register and responsive to the application of a single voltage change from a first level to a sec-

ond level to (a) reset said first order display to a predetermined display condition regardless of the display condition thereof at the instant said voltage change occurs and (b) simultaneously inhibit the application of actuating signals to successive higher decoder registers in said timepiece for the duration of said second voltage level,

a reset switching means coupled between said control means and a voltage source for conditionally changing the voltage level of said control means from said first level to said second level so as to permit the individual change of successively higher decoder registers during the period said second voltage level is applied to said control means.

7. Apparatus according to claim 6 wherein said predetermined display condition of first order decoder register is zero.

8. Apparatus according to claim 6 wherein additional reset switching means are coupled between said base signal source and the decoder registers in the higher order displays of said timepiece for conditionally applying said base signal directly to selected ones of said individual higher order display decoder registers for selectively advancing any given higher order display at a rate faster than that produced by the supply of the actuating signal to the decoder register of that display from the decoder register of the next lower order register, during the period said second voltage level is applied to said control means.

9. Apparatus according to claim 6 wherein is provided a secondary source providing a signal at a frequency higher than that of said base signal source, and additional switching means whereby a signal from said secondary source or a signal from said base signal source may be selectively applied to any one of the higher order displays during the period said second voltage level is applied to said control means.

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