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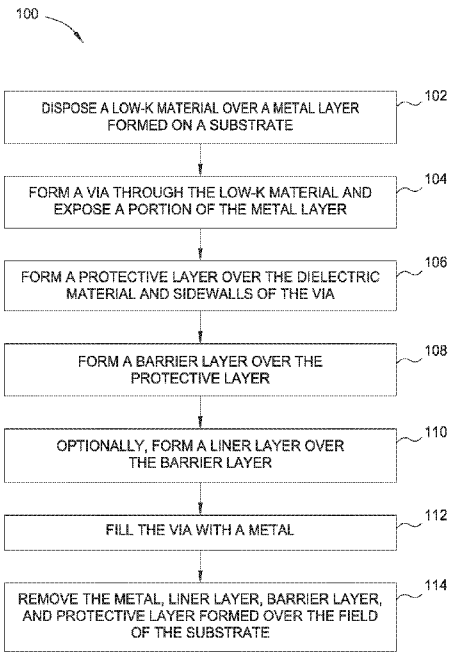


FIG. 1

(57) Abstract: A method and apparatus for forming an interconnect on a substrate is provided. A protective layer is formed on the substrate and in a via formed on the substrate wherein the protective layer is resistant to a halogen containing material. A barrier layer is formed on top of the protective layer. The barrier layer comprises a halogen containing material. A metal layer is deposited over the barrier layer. In another embodiment, the protective layer is selectively deposited in the via.

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METHOD AND APPARATUS FOR PROTECTING METAL INTERCONNECT FROM HALOGEN BASED PRECURSORS

BACKGROUND

[0001] Field

[0002] The present disclosure generally relates to a method and apparatus for forming interconnects and other conductive features in the fabrication of integrated circuits and other electronic devices. Specifically, the present disclosure relates to a method and apparatus for forming a protective layer resistant to halogen based precursors.

[0003] Description of the Related Art

[0004] As the structure size of integrated circuit (IC) devices is scaled down to sub-quarter micron dimensions, electrical resistance, and current densities have become an area for concern and improvement. Multilevel interconnect technology provides the conductive paths throughout an IC device, and are formed in high aspect ratio features including contacts, plugs, vias, lines, wires, and other features. A typical method for forming an interconnect on a substrate includes depositing one or more layers, etching at least one of the layer(s) to form one or more features, depositing a barrier layer in the feature(s), and depositing one or more layers to fill the feature. Typically, a feature is formed within a dielectric material disposed between a lower conductive layer and an upper conductive layer. The interconnect is formed within the feature to link the upper and lower conductive layers. Reliable formation of these interconnect features is important to the production of the circuits and the continued effort to increase circuit density and quality on individual substrates.

[0005] Copper is a choice metal for filling sub-micron high aspect ratio interconnect features because copper and its alloys have lower resisitivities than aluminum. However, copper diffuses more readily into surrounding materials and can alter the electronic device characteristics of the adjacent layers. The diffused copper can form a conductive path between layers thereby reducing the reliability of the overall circuit and may even result in device failure. Hence, barrier layers are deposited prior to copper metallization to prevent or impede diffusion of copper atoms. Barrier

layers typically are refractory metals such as tungsten, titanium, tantalum, and nitrides thereof, which all have a greater density than copper.

[0006] Halogen based precursors, such as chlorine and fluorine, aid in depositing a uniform barrier layer as compared to non-halogen based precursors. Halogen based precursors, however, may corrode the copper filling the high aspect ratio interconnect. This results in formation of various copper compounds that are difficult to remove from the substrate due to low volatility. Thus, the copper may corrode resulting in a reduction in reliability and loss of yield.

[0007] Therefore, there is a need to prevent adverse reaction between halogen based precursors and copper material comprising an interconnect.

SUMMARY

[0008] In one embodiment, a method of forming an interconnect on a substrate is disclosed herein. A protective layer is formed on a substrate and in a via formed on the substrate. The protective layer is resistant to a halogen containing material. A barrier layer is formed on the protective layer. The barrier layer comprises a halogen containing material. A blanket metal is deposited over the barrier layer.

[0009] In another embodiment, a method for forming an interconnect on a substrate is disclosed herein. A protective layer is selectively formed in a via formed on the substrate. The protective layer is resistant to a halogen containing material. A barrier layer is formed on the protective layer. The barrier layer comprises a halogen containing material. A blanket metal layer is deposited over the barrier layer.

[0010] In another embodiment, a method for forming an interconnect on a substrate is disclosed herein. A protective layer is formed on a via formed on a substrate. The protective layer is formed from ruthenium. A barrier layer is formed on the protective layer using a chlorine precursor. A liner layer is formed on the barrier layer. A blanket copper layer is deposited over the liner layer and fills the via.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the

disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0012] Figure 1 illustrates one embodiment of a method for forming a metal interconnect on a substrate.

[0013] Figures 2A-2G illustrate cross-sectional views of a substrate at different stages of the method of Figure 1.

[0014] Figure 3 illustrates one embodiment of a method for forming a metal interconnect on a substrate.

[0015] Figures 4A-4G illustrate cross-sectional views of a substrate at different stages of the method of Figure 3.

[0016] Figures 5 illustrate a schematic view of one embodiment of a processing system configured to carry out the methods according to Figure 1 and Figure 3.

[0017] Figure 6 illustrates a cross sectional view of a metal interconnect on a substrate, according to one embodiment.

[0018] For clarity, identical reference numerals have been used, where applicable, to designate identical elements that are common between figures. Additionally, elements of one embodiment may be advantageously adapted for utilization in other embodiments described herein.

DETAILED DESCRIPTION

[0019] Figure 1 illustrates one embodiment of a method 100 for forming a metal interconnect on a substrate. Figures 2A-2G illustrate cross-sectional views of a substrate at different stages of the method of Figure 1. Figure 2A depicts a substrate 200 having a metal layer 202 formed on the substrate 200. Method 100 begins at block 102 by disposing a dielectric material 204 on the metal layer 202 formed over the substrate 200, as shown in Figure 2B. The dielectric material 204

may be made, for example, from a low dielectric constant material such as silicon oxide, fluorine doped silicon oxide, or carbon fluorine. At block 104, a via 206 is formed through the dielectric material 204, as shown in Figure 2B. The via 206 extends from a top surface 205 of the dielectric material 204 to a top surface 207 of the metal layer 202 to expose the metal layer 202. The top surface 205 of the remaining dielectric material 204 defines a field 209 of the substrate 200.

[0020] At block 106, a protective layer 208 is formed over the surface of the dielectric material 204 and in the via 206, as shown in Figure 2C. The protective layer 208 may be deposited using a physical vapor deposition (PVD) process, an atomic layer deposition (ALD) process, a chemical vapor deposition (CVD) process, or other suitable processes. The protective layer 208 is made from a material that is resistant to a halogen containing material. Such suitable materials include, but are not limited to, ruthenium (Ru), titanium nitride (TiN), tantalum nitride (TaN), or ruthenium titanium nitride (RuTiN). The protective layer 208 acts as a barrier to prevent reaction between a halogen containing material and the underlying metal layer 202.

[0021] At block 108, a barrier layer 210 is deposited over the surface of the protective layer 208, as shown in Figure 2D. The barrier layer 210 may be deposited using PVD, ALD, CVD, or other suitable processes. The barrier layer 210 may be deposited by using a halogen containing precursor, such as a chlorine containing precursor or a fluorine containing precursor. The halogen containing precursors are used to deposit the barrier layer 210, such as, but not limited to, tantalum (Ta), TaN, or alloyed Ta (e.g. TiTa, TaAl). The barrier layer 210 prevents diffusion of a metal into the surrounding dielectric material 204. The barrier layer 210 also provides an adhesive layer on the surrounding dielectric material 204 onto which the metal can be deposited.

[0022] At block 110, an optional liner layer 212 may be deposited over the surface of the barrier layer 210, as shown in Figure 2E. The liner layer 212 may be deposited using PVD, ALD, CVD, or other suitable processes. Additionally, the liner layer 212 may be deposited in the same chamber as the barrier layer 210. The liner layer 212 may be copper, ruthenium, or any other suitable material.

[0023] At block 112, the via 206 is filled with a metal 214, as illustrated in Figure 2F. The metal 214 may be deposited in the via 206 by PVD, ALD, CVD, or other suitable processes. The metal 214 may be a conductive material, such as, but not limited to, copper (Cu) or cobalt (Co).

[0024] At block 114, the portion of the metal 214, which is formed over the field 209 of the substrate 200 may be removed using either chemical mechanical polishing, as shown in Figure 2G. The metal filled via 206 remains with the liner layer 212, the barrier layer 210, and the protective layer 208 formed between the metal 214 and the metal layer 202, following removal of the metal 214 from the field 209 above the dielectric material 204.

[0025] Figure 3 illustrates another embodiment of a method 300 for forming a metal interconnect over a substrate. Figures 4A-4G illustrate cross-sectional views of a substrate at different stages of the method of Figure 3. Figure 4A depicts a substrate 400 having a metal layer 402 formed on the substrate 400. Method 300 begins at block 302 by disposing a dielectric material 404 on the metal layer 402 formed over the substrate 400, as shown in Figure 4B. The dielectric material 404 may be made, for example, from a low dielectric constant material such as carbon-containing silicon oxides (SiOC), such as Black Diamond ® and Black Diamond ® II available from Applied Materials, Inc., of Santa Clara, Calif. At block 304, a via 406 is formed through the dielectric material 404, as shown in Figure 4B. The via 406 extends from a top surface 405 of the dielectric material 404 to a top surface 407 of the metal layer 402 to expose the metal layer 402. The top surface 405 of the remaining dielectric material 404 defines a field 409 of the substrate 400.

[0026] At block 306, a protective layer 408 is selectively deposited in the via 406 over the surface of the metal layer 402, as shown in Figure 4C. The protective layer 408 may be deposited using CVD, ALD, or other suitable processes. In one embodiment, the protective layer 408 may be made from a material that is resistant to a halogen containing material. Such suitable materials, include, but are not limited to, Ru, TiN, TaN, or RuTiN. The protective layer 408 acts as a barrier to prevent reaction between a halogen containing material and the underlying metal layer 402.

[0027] At block 308, a barrier layer 410 is deposited over the surface of the protective layer 408, and over the surface of the dielectric material 404, as shown in Figure 4D. The barrier layer 410 may be deposited using PVD, ALD, CVD, or other suitable processes. The barrier layer 410 may be deposited using halogen containing precursors, such as a chlorine containing precursor or a fluorine containing precursor. The barrier layer 410 deposited using halogen containing precursors may be comprised of materials, such as, but not limited to, Ta, TaN, or alloyed Ta (e.g. TiTa, TaAl). The barrier layer 410 prevents diffusion of a metal into the surrounding dielectric material 404. The barrier layer 410 also provides an adhesive layer on the surrounding dielectric material 404 onto which the metal can be deposited.

[0028] At block 310, an optional liner layer 412 may be deposited over the surface of the barrier layer 410, as shown in Figure 4E. The liner layer 412 may be deposited using PVD, ALD, CVD, or other suitable processes. Additionally, the liner layer 412 may be deposited in the same chamber as the barrier layer 410. The liner layer 412 may be copper, ruthenium, or any other suitable material.

[0029] At block 312, the via 406 is filled with a metal 414, as illustrated in Figure 4F. The metal 414 may be deposited in the via 406 by PVD, ALD, CVD, ECD, or other suitable processes. The metal 414 may be a conductive material, such as, but not limited to, copper (Cu) or cobalt (Co).

[0030] At block 314, the portion of the metal 414 which is formed over the field 409 of the substrate 400 may be removed using either chemical mechanical polishing as shown in Figure 4G. The metal filled via 406 remains with the liner layer 412, the barrier layer 410, and the protective layer 408 formed between the metal 414 and the metal layer 402, following removal of the metal 414 from above the field the dielectric material 404.

[0031] Figure 5 depicts a multi-chamber processing system 500. The processing system 500 may include load lock chambers 502, 504, robot 506, a transfer chamber 508, processing chambers 510, 512, 514, 516, 518, 528 and controller 520. The load lock chambers 502, 504 allow for the transfer of substrates (not shown) into and out of the processing system 500. Load lock chambers 502, 504 may pump down

the substrates introduced into the processing system 500 to maintain a vacuum seal. The robot 506 may transfer the substrates between load lock chambers 502, 504 and the processing chambers 510, 512, 514, 516, 518, and 528. The robot 506 may also transfer the substrates between the load lock chambers 502, 504, and the transfer chamber 508.

[0032] Each processing chamber 512, 514, 516, 518 and 528 may be outfitted to perform a number of substrate operations such as ALD, CVD, PVD, etch, pre-clean, de-gas, heat, orientation, and other substrate processes. Additionally, each processing chamber 512, 514, 516, 518, and 528 may be outfitted to respectfully deposit a protective layer, a barrier layer, a liner layer, and a metal layer.

[0033] The controller 520 may be used to operate all aspects of the processing system 500, such as the methods disclosed in Figure 1 and Figure 3. For example, the controller 520 may be configured to control the method of forming a metal interconnect on a substrate. The controller 520 includes a programmable central processing unit (CPU) 522 that is operable with a memory 524 and a mass storage device, an input control unit, and a display unit (not shown), such as power supplies, clocks, cache, input/output (I/O) circuits, and the like, coupled to the various components of the processing system 500 to facilitate control of the substrate processing. The controller 520 also includes hardware for monitoring substrate processing through sensors in the processing system 500, including sensors monitoring the precursor, process gas and purge gas flow. Other sensors that measure system parameters such as substrate temperature, chamber atmosphere pressure and the like may also provide information to the controller 520.

[0034] To facilitate control of the processing system 500 described above, the CPU 522 may be one of any form of general purpose computer processor that can be used in an industrial setting, such as a programmable logic controller (PLC), for controlling various chambers and sub-processors. The memory 524 is coupled to the CPU 522 and the memory 524 is non-transitory and may be one or more of readily available memory such as random access memory (RAM), read only memory (ROM), floppy disk drive, hard disk, or any other form of digital storage, local or remote. Support circuits 526 are coupled to the CPU 522 for supporting the processor in a conventional manner. Charged species generation, heating, and

other processes are generally stored in the memory 524, typically as a software routine. The software routine may also be stored and/or executed by a second CPU (not shown) that is remotely located from the hardware being controlled by the CPU 522.

[0035] The memory 524 is in the form of computer-readable storage media that contains instructions, that when executed by the CPU 522, facilitates the operation of the processing system 500. The instructions in the memory 524 are in the form of a program product such as a program that implements the method of the present disclosure. The program code may conform to any one of a number of different programming languages. In one example, the disclosure may be implemented as a program product stored on a computer-readable storage media for use with a computer system. The program(s) of the program product define functions of the embodiments (including the methods described herein). Illustrative computer-readable storage media include, but are not limited to: (i) non-writable storage media (*e.g.,* read-only memory devices within a computer such as CD-ROM disks readable by a CD-ROM drive, flash memory, ROM chips or any type of solid-state non-volatile semiconductor memory) on which information is permanently stored; and (ii) writable storage media (*e.g.,* floppy disks within a diskette drive or hard-disk drive or any type of solid-state random-access semiconductor memory) on which alterable information is stored. Such computer-readable storage media, when carrying computer-readable instructions that direct the functions of the methods described herein, are embodiments of the present disclosure.

EXAMPLE 1

[0036] The following example may be carried out using the processing chamber described in Figure 5. A substrate having a carbon containing silicon oxide layer formed over a conductive layer is used to form an interconnect according to one embodiment. The conductive layer in this example is fabricated from copper. A via is etched through the carbon containing silicon oxide layer, from the top surface of the carbon containing silicon oxide layer to the top surface of the copper layer to expose the copper layer. A robot moves the substrate from the load lock chamber to a first processing chamber for de-gas. The robot moves the substrate from the de-gas chamber to a second processing chamber for a pre-clean process after the de-

gas process. The de-gas and pre-clean processes ensure that the substrate is free from any native oxides.

[0037] The robot transports the substrate to a second processing chamber for deposition of the protective layer. In the protective layer processing chamber, a ruthenium layer is deposited on the surface of the dielectric layer and in the via. The ruthenium layer acts as a protective layer to prevent reaction of the chlorine precursor (used in the deposition of the barrier layer) with the underlying copper metal. The ruthenium layer prevents such undesirable reaction because ruthenium is resistant to reaction with chlorine. The ruthenium layer is deposited using a CVD process. The thickness of the ruthenium layer may be between 1 nm and 5 nm.

[0038] The robot moves the substrate from the protective layer processing chamber to the barrier layer processing chamber, after the deposition of the ruthenium protective layer is complete. The barrier layer is deposited over the surface of the ruthenium protective layer using a CVD process. A chlorine precursor gas is used for deposition of the barrier layer, where the barrier layer is a Ta film. The substrate may remain in the barrier layer processing chamber for deposition of a liner layer on the top surface of the barrier layer.

[0039] The robot may move the substrate from the barrier layer processing chamber to a processing chamber for deposition of a copper seed. The copper may be deposited to fill the via using a CVD process. The top surface of the liner layer on top of the dielectric material may also be layered with the copper material.

[0040] The substrate may be moved into a chemical mechanical polishing system to planarize the copper layer back to the liner layer, the liner layer back to the barrier layer, the barrier layer back to the protective layer, and the protective layer back to the dielectric material.

EXAMPLE 2

[0041] The following example may be carried out using the processing chamber described in Figure 5. A substrate having a carbon containing silicon oxide layer formed over a conductive layer is used to form an interconnect according to one embodiment. The conductive layer in this example is fabricated from copper. A via

is etched through the carbon containing silicon oxide layer from a top surface of the carbon containing silicon oxide layer to the top surface of the copper layer to expose the copper layer. A robot moves the substrate from the load lock chamber to a first processing chamber for de-gas. The robot moves the substrate from the de-gas chamber to a second processing chamber for a pre-clean process, after the de-gas process is complete. The de-gas and pre-clean processes ensure that the substrate is free from any native oxides.

[0042] The robot transports the substrate to a second processing chamber for deposition of the protective layer. In the protective layer processing chamber, a titanium nitride (TiN) layer is deposited on the surface of the dielectric layer and in the via. The TiN layer acts as a protective layer to prevent reaction of the fluorine precursor (used in the deposition of the barrier layer) with the underlying copper metal. The TiN layer prevents such undesirable reaction because TiN is resistant to reaction with fluorine. The TiN layer is deposited on the substrate using a CVD process. The thickness of the TiN layer may be between 1 nm and 5 nm.

[0043] The robot moves the substrate from the protective layer processing chamber to the barrier layer processing chamber, after deposition of the TiN protective layer is complete. The barrier layer is deposited over the surface of the TiN protective layer using a CVD process. A fluorine precursor gas is used for deposition of the barrier layer, where the barrier layer is a Ta film. The substrate may remain in the barrier layer processing chamber for deposition of a liner layer on the top surface of the barrier layer.

[0044] The robot may move the substrate from the barrier layer processing chamber to a processing chamber for deposition of a copper seed. The copper may be deposited to fill the via using a CVD process. The top surface of the liner layer on top of the dielectric material may also be layered with the copper material.

[0045] The substrate may be moved into a chemical mechanical polishing system to planarize the copper layer back to the liner layer, the liner layer back to the barrier layer, the barrier layer back to the protective layer, and the protective layer back to the dielectric material.

EXAMPLE 3

[0046] The following example may be carried out using the processing chamber described in Figure 5. A substrate having a carbon containing silicon oxide layer formed over a conductive layer is used to form an interconnect according to one embodiment. The conductive layer in this example is fabricated from cobalt. A via is etched through the carbon containing silicon oxide layer from the top surface of the carbon containing silicon oxide layer to the top surface of the cobalt layer to expose the cobalt layer. A robot moves the substrate from the load lock chamber to a first processing chamber for de-gas. The robot moves the substrate from the de-gas chamber to a second processing chamber for a pre-clean process, after the de-gas process is complete. The de-gas and pre-clean processes ensure that the substrate is free from any native oxides.

[0047] The robot transports the substrate to a second processing chamber for deposition of the protective layer. In the protective layer processing chamber, a ruthenium layer is selectively deposited in the via, on the surface of the cobalt layer. The ruthenium layer acts as a protective layer to prevent reaction of the chlorine precursor (used in the deposition of the barrier layer) with the underlying cobalt metal. The ruthenium layer prevents such undesirable reaction because ruthenium is resistant to reaction with chlorine. The selective deposition increases the volume of cobalt because the protective material on the side walls of the via is decreased through the selective deposition. The ruthenium layer is deposited on the substrate using a CVD process. The thickness of the ruthenium layer may be between 1 nm to 5 nm.

[0048] After the deposition of the ruthenium protective layer is complete, the robot moves the substrate from the protective layer processing chamber to the barrier layer processing chamber. The barrier layer is deposited over the surface of the ruthenium protective layer and over the surface of the dielectric material using a CVD process. A chlorine precursor gas is used for deposition of the barrier layer, where the barrier layer is a Ta film. The substrate may remain in the barrier layer processing chamber for deposition of a liner layer on the top surface of the barrier layer.

[0049] The robot may move the substrate from the barrier layer processing chamber to a processing chamber for deposition of a cobalt seed. The cobalt may be deposited to fill the via using a CVD process. The top surface of the liner layer on top of the dielectric material may also be layered with the cobalt material.

[0050] The substrate may be moved into a chemical mechanical polishing system to planarize the cobalt layer back to the liner layer, the liner layer back to the barrier layer, the barrier layer back to the protective layer, and the protective layer back to the dielectric material.

EXAMPLE 4

[0051] The following example may be carried out using the processing chamber described in Figure 5. A substrate having a carbon containing silicon oxide layer formed over a conductive layer is used to form an interconnect according to one embodiment. The conductive layer in this example is copper. A via is etched through the carbon containing silicon oxide layer, from a top surface to the carbon containing silicon oxide layer to the top surface of the copper layer to expose the copper layer. A robot moves the substrate from the load lock chamber to a first processing chamber for de-gas. The robot moves the substrate from the de-gas chamber to a second processing chamber for a pre-clean process, after the de-gas process is complete. The de-gas and pre-clean processes ensure that the substrate is free from any native oxides.

[0052] The robot transports the substrate to a second processing chamber for deposition of the protective layer. In the protective layer processing chamber, a ruthenium layer is selectively deposited in the via on the surface of the exposed copper metal layer. The ruthenium layers acts as a protective layer to prevent reaction of the chlorine precursor (used in the deposition of the barrier layer) with the underlying copper metal. The ruthenium layer prevents such undesirable reaction because ruthenium is resistant to reaction with chlorine. The ruthenium layer is deposited using a PVD process. A collimator is disposed in the PVD chamber so that the ruthenium may be selectively deposited on the exposed copper surface. The volume of copper is thus, increased, because the protection material on the side

walls of the via is decreased. The thickness of the ruthenium layer may be between 1 nm to 5 nm.

[0053] The robot moves the substrate from the protective layer processing chamber to the barrier layer processing chamber, when the deposition of the ruthenium protective layer is complete. The barrier layer is deposited over the surface of the ruthenium protective layer and over the surface of the dielectric material using a CVD process. A chlorine precursor gas is used for deposition of the barrier layer, where the barrier layer is a Ta film. The substrate may remain in the barrier layer processing chamber for deposition of a liner layer on the top surface of the barrier layer.

[0054] The robot may move the substrate from the barrier layer processing chamber to a processing chamber for deposition of a copper seed. The copper may be deposited to fill the via using a CVD process. The top surface of the liner layer on top of the dielectric material may also be layered with the copper material.

[0055] The substrate may be moved into a chemical mechanical polishing system to planarize the copper layer back to the liner layer, the liner layer back to the barrier layer, the barrier layer back to the protective layer, and the protective layer back to the dielectric material.

EXAMPLE 5

[0056] The following example may be carried out using the processing chamber described in Figure 5. A substrate having a carbon containing silicon oxide layer formed over a conductive layer is used to form an interconnect according to one embodiment. The conductive layer in this example is copper. A via is etched through the carbon containing silicon oxide layer, from a top surface to the carbon containing silicon oxide layer to the top surface of the copper layer to expose the copper layer. A robot moves the substrate from the load lock chamber to a first processing chamber for de-gas. The robot moves the substrate from the de-gas chamber to a second processing chamber for a pre-clean process, after the de-gas process is complete. The de-gas and pre-clean processes ensure that the substrate is free from any native oxides.

[0057] The robot transports the substrate to a second processing chamber for deposition of the protective layer. In the protective layer processing chamber, a ruthenium layer is selectively deposited in the via on the surface of the exposed copper metal layer. The ruthenium layers acts as a protective layer to prevent reaction of the chlorine precursor (used in the deposition of the barrier layer) with the underlying copper metal. The ruthenium layer prevents such undesirable reaction because ruthenium is resistant to reaction with chlorine. The ruthenium layer is deposited using a PVD process. A collimator is disposed in the PVD chamber so that the copper may be selectively deposited on the exposed copper surface. The volume of copper is thus, increased, because the protection material on the side walls of the via is decreased. The thickness of the ruthenium layer may be between 1 nm to 5 nm.

[0058] The robot moves the substrate from the protective layer processing chamber to the barrier layer processing chamber, when the deposition of the ruthenium protective layer is complete. The barrier layer is deposited over the surface of the ruthenium protective layer and over the surface of the dielectric material using a CVD process. A chlorine precursor gas is used for deposition of the barrier layer, where the barrier layer is a Ta film. The substrate may remain in the barrier layer processing chamber for deposition of a liner layer on the top surface of the barrier layer.

[0059] The robot may move the substrate from the barrier layer processing chamber to a processing chamber for deposition of a cobalt seed. The cobalt may be deposited to fill the via using a CVD process. The top surface of the liner layer on top of the dielectric material may also be layered with the cobalt material.

[0060] The substrate may be moved into a chemical mechanical polishing system to planarize the cobalt back to the liner layer, the liner layer back to the barrier layer, the barrier layer back to the protective layer, and the protective layer back to the dielectric material.

EXAMPLE 6

[0061] The following example may be carried out using the processing chamber described in Figure 5. A substrate having a carbon containing silicon oxide layer

formed over a conductive layer is used to form an interconnect according to one embodiment. The conductive layer in this example is cobalt. A via is etched through the carbon containing silicon oxide layer, from a top surface to the carbon containing silicon oxide layer to the top surface of the cobalt layer to expose the cobalt layer. A robot moves the substrate from the load lock chamber to a first processing chamber for de-gas. The robot moves the substrate from the de-gas chamber to a second processing chamber for a pre-clean process, after the de-gas process is complete. The de-gas and pre-clean processes ensure that the substrate is free from any native oxides.

[0062] The robot transports the substrate to a second processing chamber for deposition of the protective layer. In the protective layer processing chamber, a ruthenium layer is selectively deposited in the via on the surface of the exposed copper metal layer. The ruthenium layers acts as a protective layer to prevent reaction of the chlorine precursor (used in the deposition of the barrier layer) with the underlying cobalt metal. The ruthenium layer prevents such undesirable reaction because ruthenium is resistant to reaction with chlorine. The ruthenium layer is deposited using a PVD process. A collimator is disposed in the PVD chamber so that the ruthenium may be selectively deposited on the exposed cobalt surface. The volume of cobalt is thus, increased, because the protection material on the side walls of the via is decreased. The thickness of the ruthenium layer may be between 1 nm to 5 nm.

[0063] The robot moves the substrate from the protective layer processing chamber to the barrier layer processing chamber, when the deposition of the ruthenium protective layer is complete. The barrier layer is deposited over the surface of the ruthenium protective layer and over the surface of the dielectric material using a CVD process. A chlorine precursor gas is used for deposition of the barrier layer, where the barrier layer is a Ta film. The substrate may remain in the barrier layer processing chamber for deposition of a liner layer on the top surface of the barrier layer.

[0064] The robot may move the substrate from the barrier layer processing chamber to a processing chamber for deposition of a copper seed. The copper may be

deposited to fill the via using a CVD process. The top surface of the liner layer on top of the dielectric material may also be layered with the copper material.

[0065] The substrate may be moved into a chemical mechanical polishing system to planarize the copper layer back to the liner layer, the liner layer back to the barrier layer, the barrier layer back to the protective layer, and the protective layer back to the dielectric material.

[0066] The preceding embodiments depict a process flow that implements a single damascene structure. It is also contemplated that a single process flow can be implemented for a dual damascene structure. Figure 6 illustrates one embodiment of the dual damascene structure.

[0067] The dual damascene structure implements a process where a via 606 and/or trench 616 are etched into a dielectric material 604. The dielectric material 604 is deposited onto a metal layer 602. The metal layer 602 is formed on a substrate 600. A protective layer 608 may be deposited over the dielectric material 604 and into the via 606 and the trench 616 on a top surface 607 of the metal layer 602. A barrier layer 610 may be deposited over the protective layer 608. An optional liner layer 612 may be deposited over the barrier layer 610. A metal layer may be deposited over the optional liner layer 612. The metal layer 614 is used to fill the via 606 and the trench 616. The layers 608-614 may be removed from a top surface 605 of the dielectric material 604, the via 606, and trench 616 using a chemical mechanical process.

[0068] While the foregoing is directed to specific embodiments, other and further embodiments may be devised without departing from the basis scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. An interconnect on a substrate, the interconnect comprising:

a protective layer formed on a first metal layer exposed through a dielectric material, the protective layer formed on the dielectric material, wherein the protective layer is resistant to a halogen based precursor;

a barrier layer formed on the protective layer; and

a second metal layer deposited over the barrier layer.

2. The interconnect of claim 1, further comprising:

a liner layer formed on the protective layer.

3. The interconnect of claim 1, wherein the protective layer comprises:

ruthenium.

4. The interconnect of claim 3, wherein the second metal layer fills a trench or via.

5. The interconnect of claim 1, wherein the protective layer comprises:

titanium nitride.

6. The interconnect of claim 5, wherein the second metal layer fills a trench or via.

7. The interconnect of claim 1, wherein the protective layer comprises one of:

ruthenium, titanium nitride, tantalum nitride, or ruthenium titanium nitride.

8. A method of forming an interconnect on a substrate comprising:

forming a protective layer on a first metal layer exposed through a dielectric material, the protective layer formed on the dielectric material, wherein the protective layer is resistant to a halogen based precursor;

forming a barrier layer on the protective layer; and

depositing a second metal layer over the barrier layer.

9. A method for forming an interconnect on a substrate comprising:

selectively forming a protective layer on a first metal layer exposed through a dielectric material, wherein the protective layer is resistant to a halogen based precursor;

forming a barrier layer on the protective layer; and

depositing a second metal layer over the barrier layer.

10. The method according to claims 8 or 9, further comprising:

depositing a liner layer over the barrier layer.

11. The method of claim 10, wherein the protective layer comprises:

ruthenium.

12. The method of claim 11, wherein the barrier layer is deposited using chlorine based precursors.

13. The method according to claims 8 or 9, wherein the protective layer comprises:

titanium nitride.

14. The method of claim 13, wherein the barrier layer is deposited using fluorine based precursors.

15. The method according to claims 8 or 9, wherein the protective layer is made from one of ruthenium, titanium nitride, tantalum nitride, or ruthenium titanium nitride.

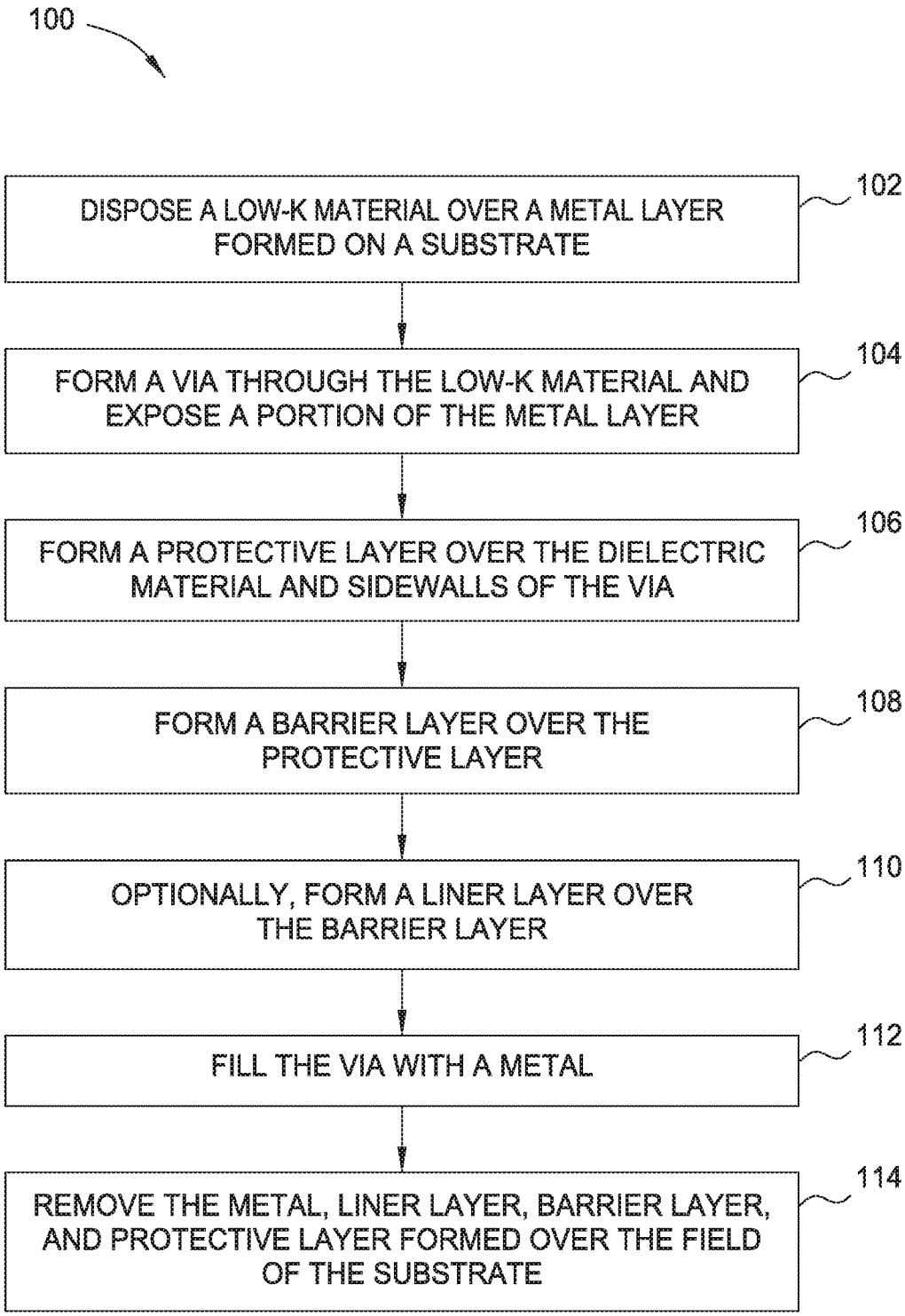

100
DISPOSE A LOW-K MATERIAL OVER A METAL LAYER FORMED ON A SUBSTRATE
102
FORM A VIA THROUGH THE LOW-K MATERIAL AND EXPOSE A PORTION OF THE METAL LAYER
104
FORM A PROTECTIVE LAYER OVER THE DIELECTRIC MATERIAL AND SIDEWALLS OF THE VIA
106
FORM A BARRIER LAYER OVER THE PROTECTIVE LAYER
108
OPTIONALLY, FORM A LINER LAYER OVER THE BARRIER LAYER
110
FILL THE VIA WITH A METAL
112
REMOVE THE METAL, LINER LAYER, BARRIER LAYER, AND PROTECTIVE LAYER FORMED OVER THE FIELD OF THE SUBSTRATE
114

FIG. 1

FIG. 2A



FIG. 2B

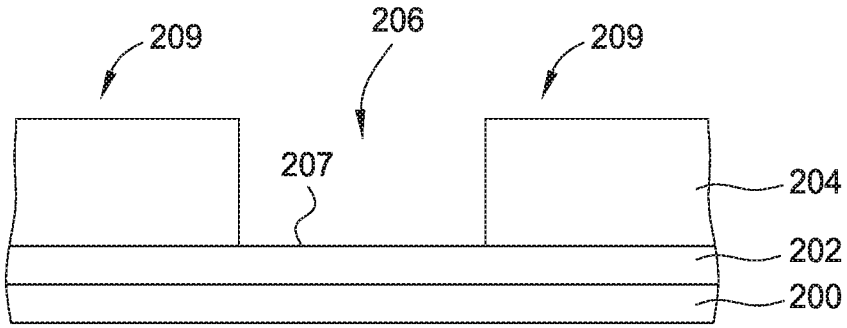


FIG. 2C

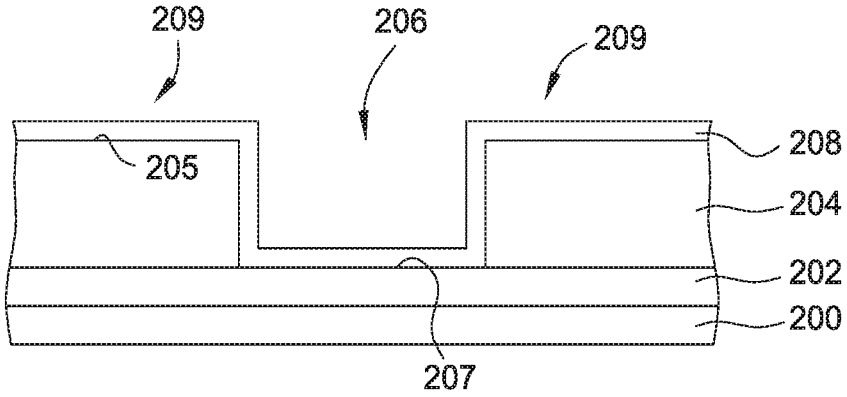


FIG. 2D

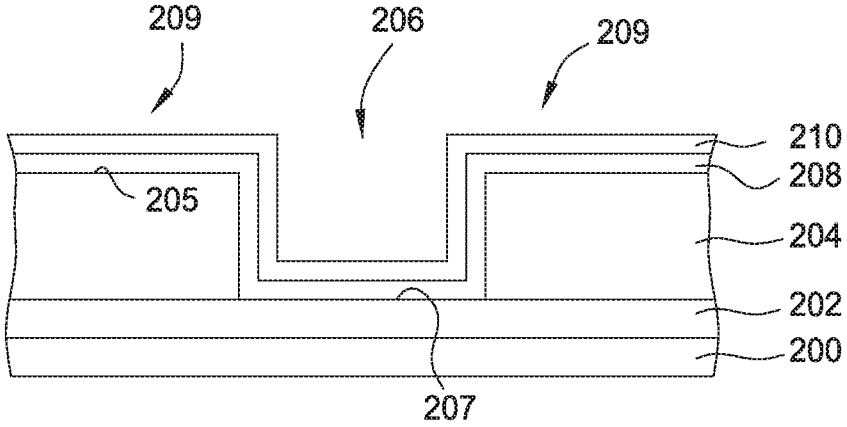


FIG. 2E

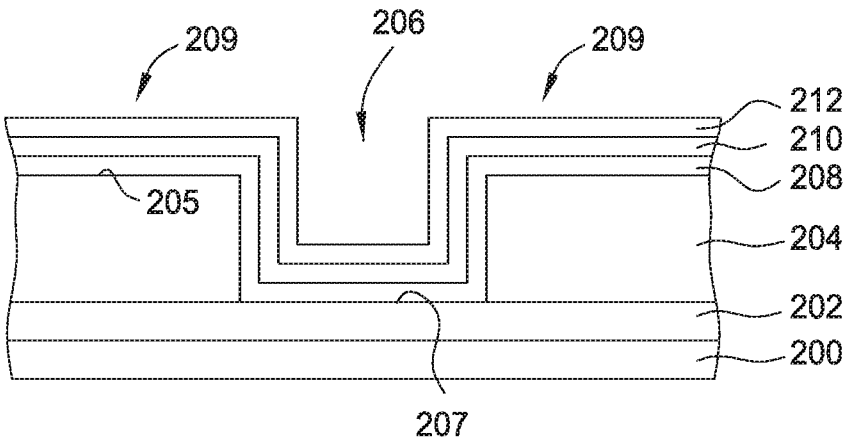


FIG. 2F

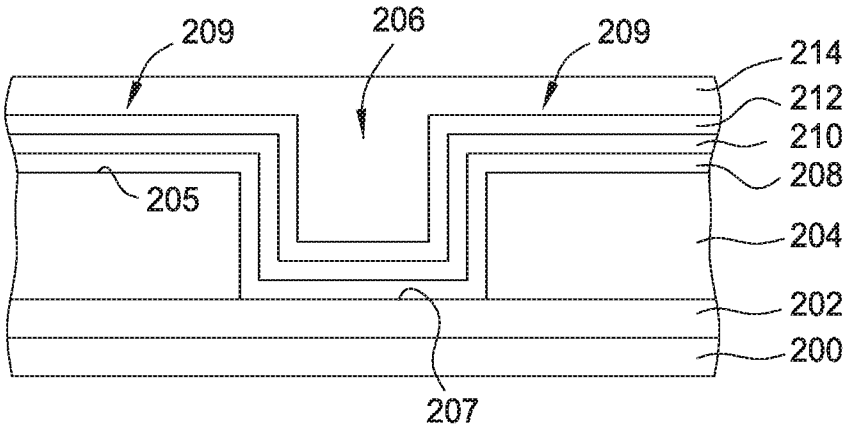
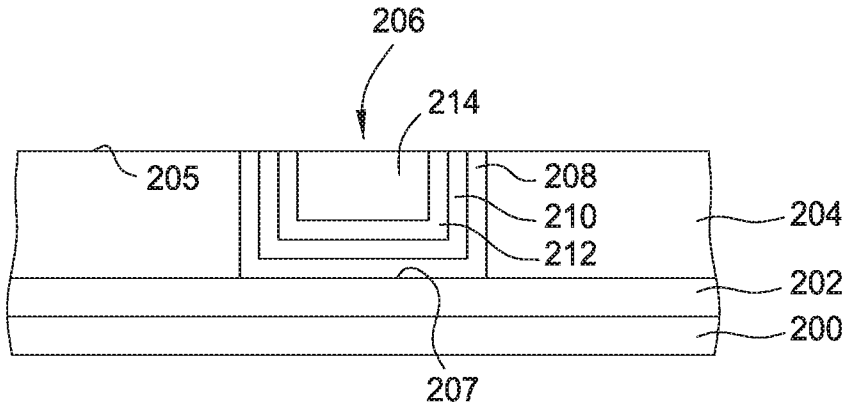


FIG. 2G



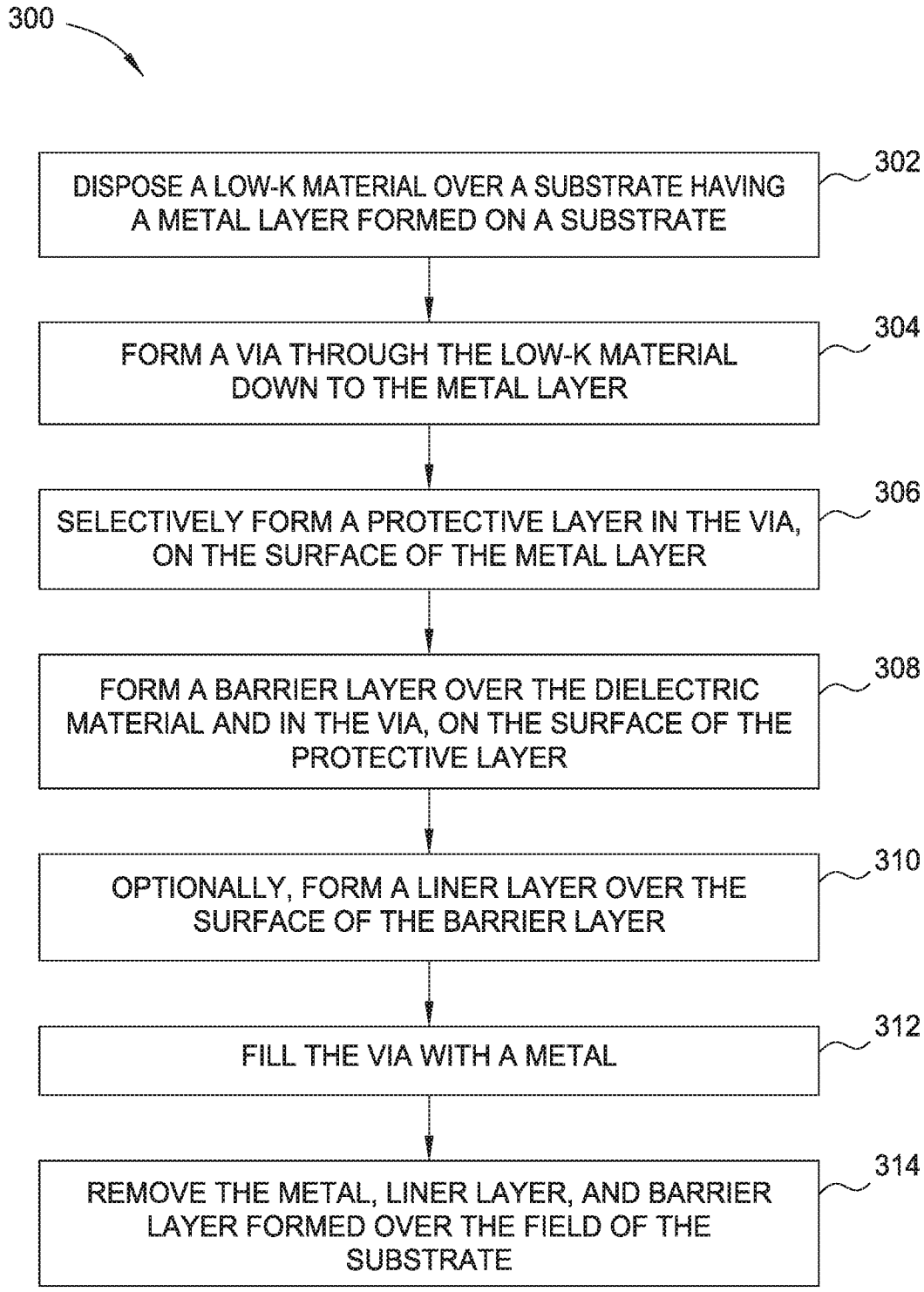

300
DISPOSE A LOW-K MATERIAL OVER A SUBSTRATE HAVING A METAL LAYER FORMED ON A SUBSTRATE
302
FORM A VIA THROUGH THE LOW-K MATERIAL DOWN TO THE METAL LAYER
304
SELECTIVELY FORM A PROTECTIVE LAYER IN THE VIA, ON THE SURFACE OF THE METAL LAYER
306
FORM A BARRIER LAYER OVER THE DIELECTRIC MATERIAL AND IN THE VIA, ON THE SURFACE OF THE PROTECTIVE LAYER
308
OPTIONALLY, FORM A LINER LAYER OVER THE SURFACE OF THE BARRIER LAYER
310
FILL THE VIA WITH A METAL
312
REMOVE THE METAL, LINER LAYER, AND BARRIER LAYER FORMED OVER THE FIELD OF THE SUBSTRATE
314

FIG. 3

FIG. 4A



FIG. 4B

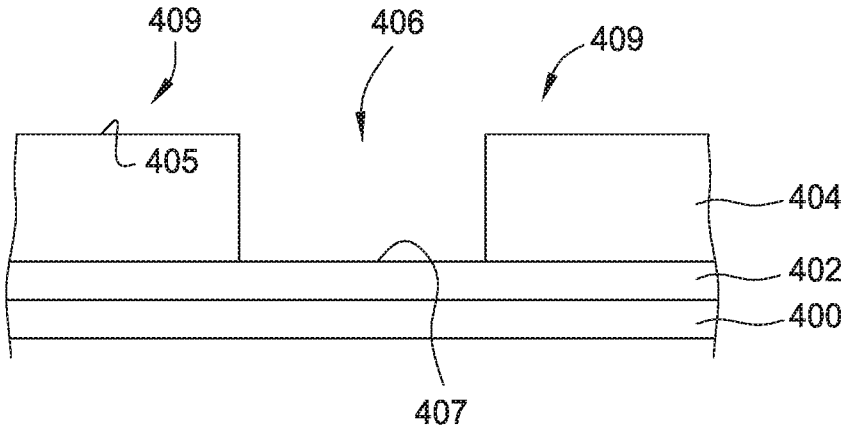


FIG. 4C

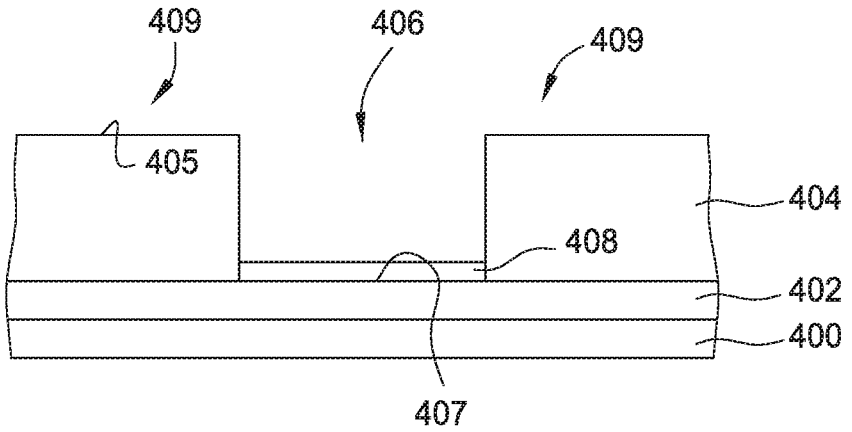


FIG. 4D

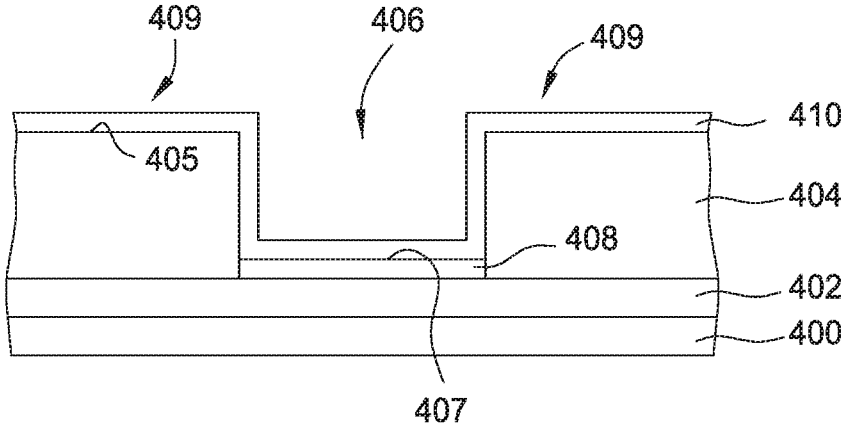


FIG. 4E

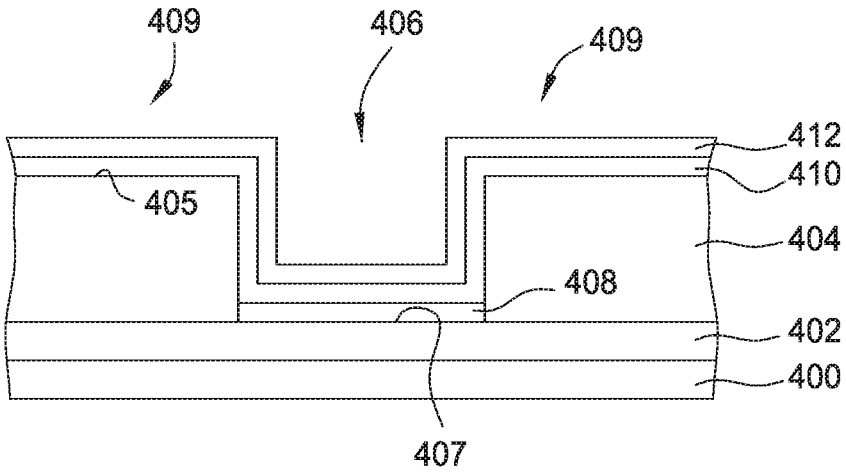


FIG. 4F

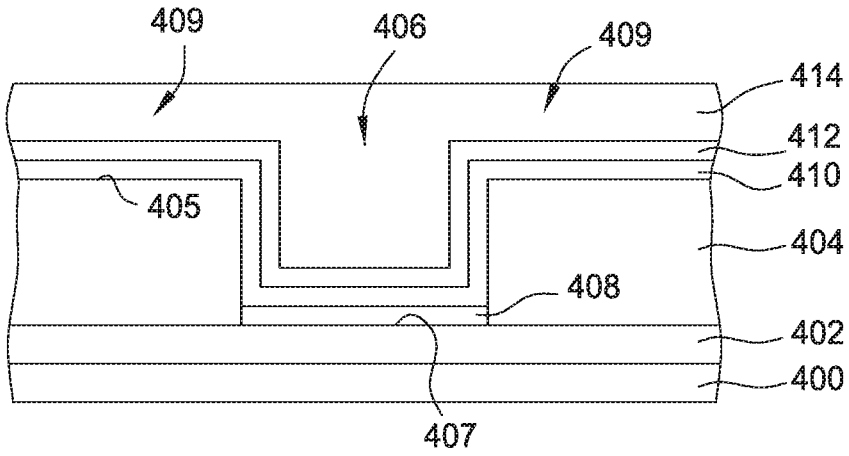
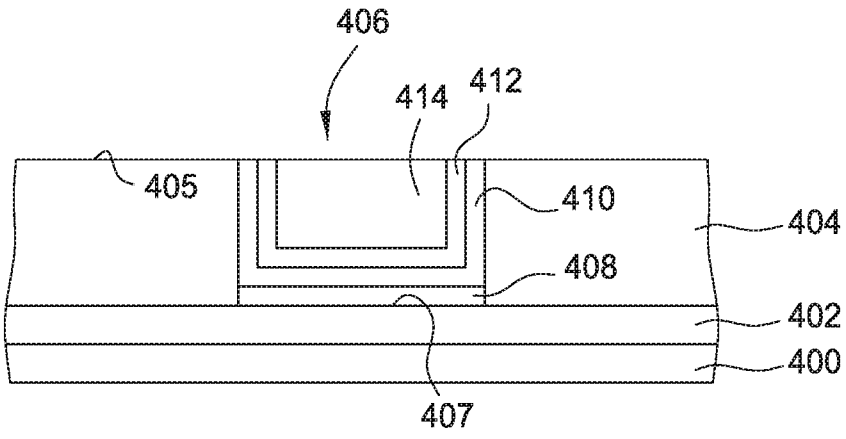


FIG. 4G



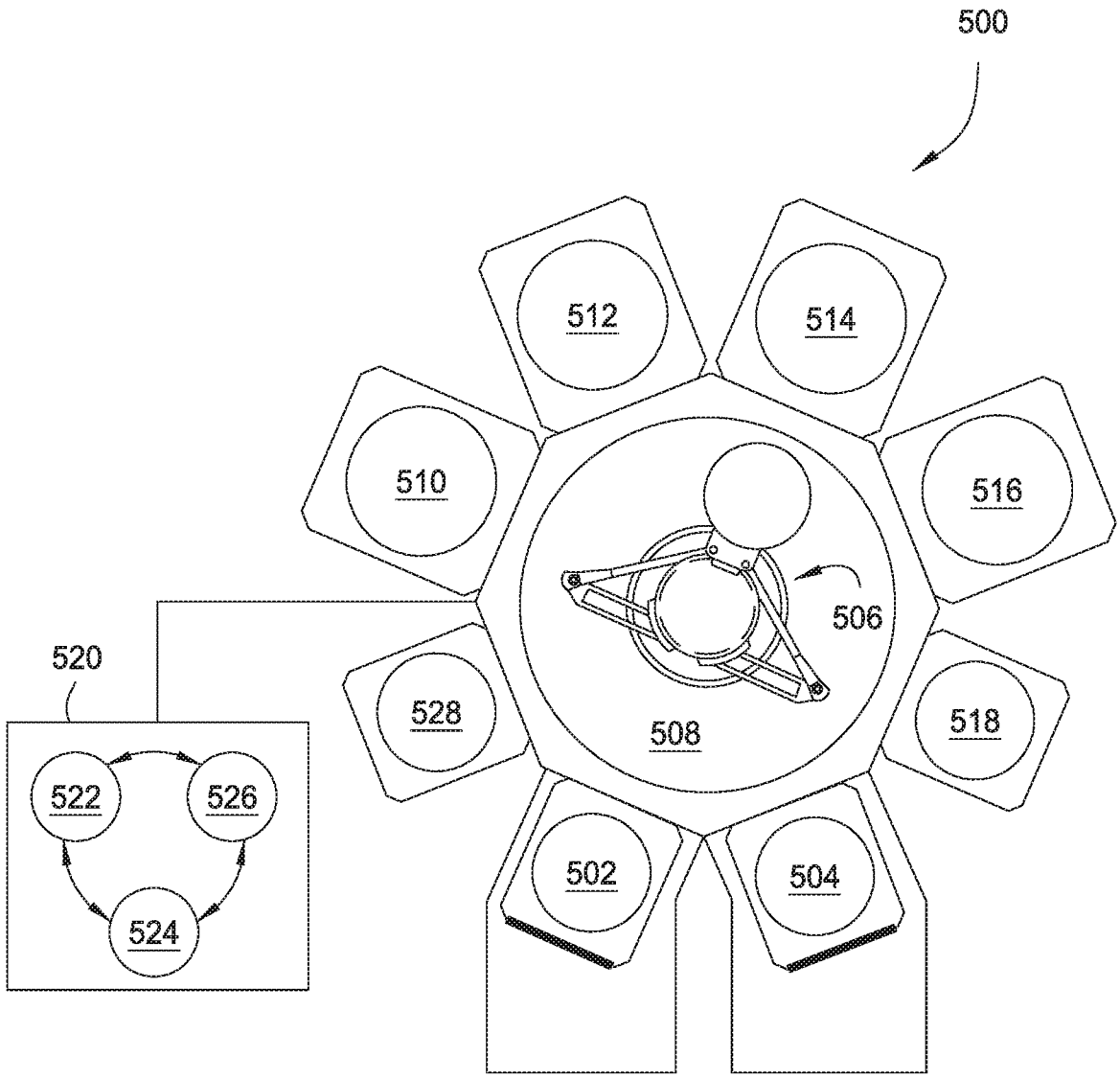


FIG.5

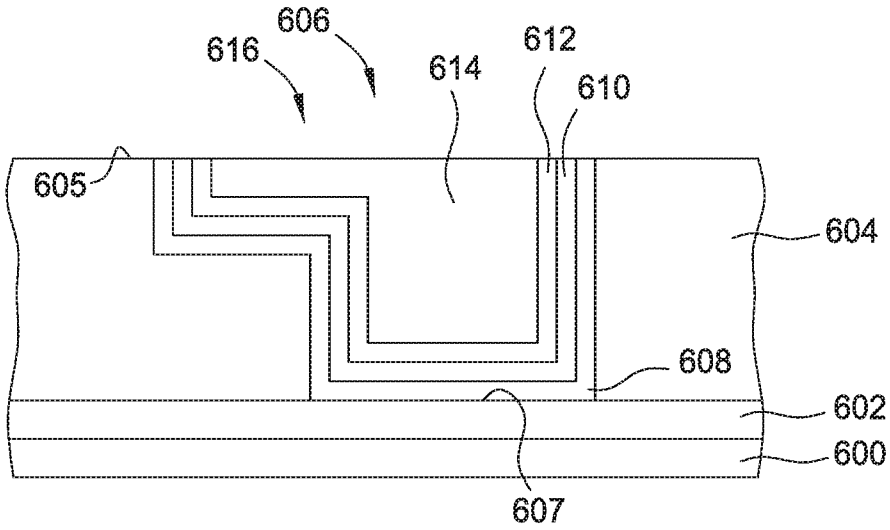


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/015754

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 23/52; H01L 21/311; H01L 21/4763; H01L 29/40; H01L 23/538; H01L 21/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: halogen, protective layer, interconnect, metal, barrier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001-0022398 A1 (ALFRED GRILL et al.) 20 September 2001 See abstract, paragraphs [0030]-[0082] and figures 4-8.	1-2,5-10,13-15
Y		3-4,11-12
Y	US 2010-0244252 A1 (CHRISTOPHER J. JEZEWSKI et al.) 30 September 2010 See abstract, paragraphs [0019], [0021] and figures 2, 4.	3-4,11-12
A	US 2009-0045517 A1 (MASAHITO SUGIURA et al.) 19 February 2009 See abstract, paragraphs [0101]-[0109] and figures 3A-3E.	1-15
A	US 2003-0119325 A1 (CHEOL MO JEONG et al.) 26 June 2003 See abstract, paragraphs [0032]-[0043] and figures 6A-6C.	1-15
A	US 2005-0142862 A1 (IN-KYU CHUN) 30 June 2005 See abstract, paragraphs [0042]-[0049] and figures 3-5.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2016 (29.04.2016)	**29 April 2016 (29.04.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/015754

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