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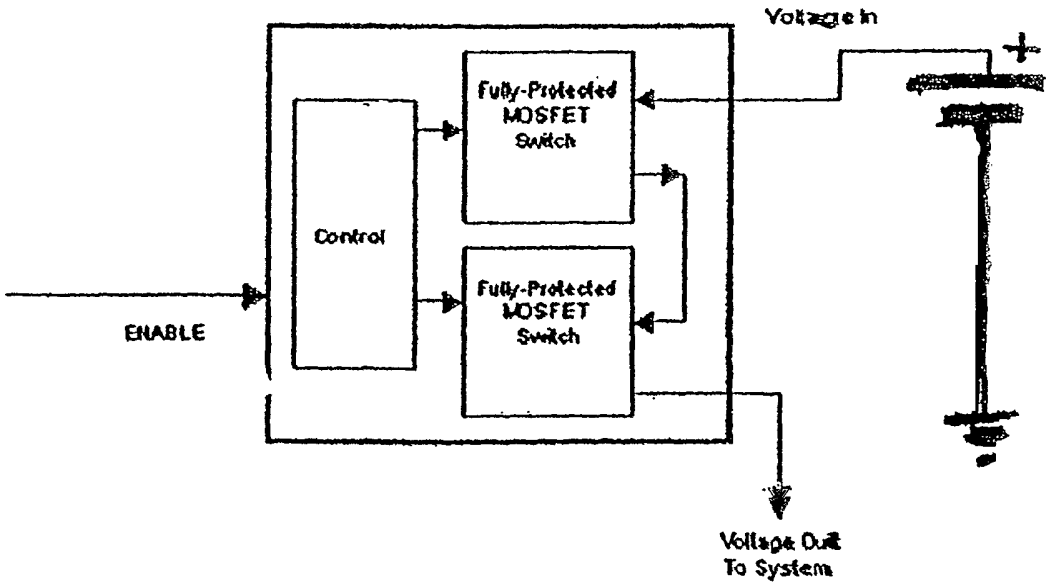
(54) Title: DIGITAL SQUIB



(57) Abstract: An intelligent switch system, a so-called squib, for providing power to sensitive equipment, such as missiles, rockets and the like, comprises a pair of serially connected power switches which are separately and sequentially enabled and which will not deliver power from their input to their outputs unless both switches turn on. These switches are controlled by an electronic microcontroller that is normally left unpowered, except when a trigger input is temporarily applied to the microcontroller.

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DIGITAL SQUIB

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit and priority of U.S. Provisional patent application Serial No. 60/563,670 filed April 19, 2004 entitled DIGITAL SQUIB, the entire disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to squibs and, more particularly, to electronically controlled digital squibs. Squibs are electrical switches with a built-in, ultrasecure mechanism to prevent accidental turn on of the switch.

[0003] Rockets, missiles, space platforms, drilling equipment, remote robotic controls and the like, have triggerable systems or devices which, when triggered or launched, result in significant events that cannot be easily reversed or stopped. Therefore, very elaborate steps are taken in the design of squibs to assure foolproof operation without any chance for accidental triggering of the switching device.

[0004] Conventional squibs are expensive, elaborate and electromechanical, as well as chemical, devices which sometimes include explosive components that destroy a trigger prevention protector when it is decided that the squib is to be enabled. It would be advantageous to obtain a squib that avoids the drawbacks of conventional squibs, including relative to the complexity, construction and cost thereof and obtain a squib with enhanced programmability and versatility features.

SUMMARY OF THE INVENTION

[0005] It is an object of the present invention to provide a squib that is not pyrotechnically operable, can be safely reset to its initial state, and comprises programmable timing for turning on, i.e. "firing".

[0006] Another object of the invention is to provide an electronically controlled squib.

[0007] The foregoing and many other objects of the invention are realized with an electronic squib which incorporates several levels of protection such as to meet the requirements and specifications for conventional squibs, that are typically utilized in providing power to sensitive equipment, such as missiles, rockets, space platforms, drilling equipment, remote robotic controls and the like.

[0008] Essentially, the intelligent squib of the present invention comprises a pair of serially connected power switches which are separately and sequentially enabled and which will not deliver power from their input to their outputs unless both switches turn on. These switches are controlled by an electronic microcontroller that is normally left unpowered, except when a trigger input (VOLTAGE) is temporarily applied to the microcontroller, which then begins its operation by enabling the first of the pair of series switches and at the same time, becomes electrically powered from the enablement of the first switch.

[0009] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a mechanical drawing of the digital squib of the present invention.

[0011] Figures 2a and 2b are circuit diagrams of the digital squib of the present invention, with Figure 2b representing the continuation of Figure 2a.

[0012] Figure 3 is a block diagram of the digital squib of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0013] Figure 1 illustrates the layout and dimensional sizes, as well as pin assignment for an intelligent, digital squib constructed in accordance with one PCB (printed circuit board) layout thereof, although it should be appreciated that the varieties and possibilities for the layout of the device is virtually infinite. Nonetheless, and in accordance with Figure 1, there is illustrated a dual inline package which utilizes 16 pins.

[0014] Turning to Figure 2, it is noted that the main component of the squib comprises the microcontroller denominated as integrated circuit (IC) U2 which can preferably be a PIC12F6291(E)SN device. The main power switches are denominated as IPS1 and IPS3 and each preferably comprises an IPS521G FET switch.

[0015] The operational concept of the intelligent squib of Figure 2 can be appreciated from the following generalized description of the illustrated circuit. Thus, when a momentary power pulse is applied as a signal switch power at PIN 16 (or PIN 15), the power flows through the diode D1 to the U1 integrated circuit which produces a power supply voltage of 5v at 50ma, at the power input PIN 1 (VCC) of the microcontroller U2. If the protect signal at PIN 6 is in a state that does not disable the microcontroller U2, it issues a first enabling signal to the IPS1 FET as a signal EN 1. This causes the FET switch IPS1 to close (turn on), providing an output voltage signal. This causes the voltage to appear at the Vout PIN 4 of the IPS1 switch which then supplies power as in input power to the voltage regulator U1 (for example, an LM2936MM-5.0 device), which then permits the microcontroller U2 to continue to be powered, even after the SwitchPower signal at PIN 16 of the device has been removed.

[0016] Subsequently, and after a programmable time delay, the microcontroller issues a second enable signal EN 2 which is provided to the second FET switch IPS3. Once the second switch is enabled, the power signal which is provided as

a Vin voltage at the device pins 3, 4 and 5, ultimately appears as the Vout signal at the device pins 10, 11 and 12. It is this Vout signal at the pins 10, 11 and 12 that is supplied to the ultimately controlled device being controlled, e.g., the missile, rocket, etc. The pair of FET switches identified as parts IPS2 and IPS4 (utilizing IPS5451S FETs) can be utilized for lower voltage but higher sustained current applications. The PCB is designed to accept either type of FET device.

[0017] Figure 3 is a block diagram of the circuit of Figure 2 showing the control device and the fully protected MOSFET switches, as described above.

[0018] The intelligent squib of the present invention has been constructed and found to be highly reliable and well protected. It can be provided in normally open or closed models. It can handle inductive loads and its protection includes short circuit ESD, user fully protected power MOSFET switches utilizing the above-described two-level in-series MOSFETS. The novel device can provide programmable delay from enable to circuit closure and it can be provided in small package sizes, as well as in surface mounted technology packages or in conventional dual inline construction.

[0019] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. An electrical, digital switch system for a load, the switch system including a built-in secure mechanism to prevent accidental turn on, the switch system comprising:

a normally unpowered controller and an input circuit for receiving a pulse of temporary power for the controller, the controller being operable to produce a first enable output and a second enable output;

a first switch coupled to the first enable output and being operable responsive thereto to provide a first output voltage, said first output voltage being coupled to said controller to continue powering said controller, even after said pulse of temporary power has been inactivated; and

a second switch coupled to the first output voltage and coupled to the second enable output and being responsive thereto to provide a second output voltage which is suitable for being coupled to the load.

2. The digital switch system of claim 1, wherein the controller comprises a digital circuit.

3. The digital switch system of claim 2, wherein the first switch and the second switch comprise a respective field effect transistor.

4. The digital switch system of claim 2, wherein the input circuit includes a diode.

5. The digital switch system of claim 2, including a disable signal input for the controller which renders the controller inoperable, even in the presence of the pulse of temporary power.

6. The digital switch system of claim 2, including a printed circuit board having socket arrangements for receiving and housing the controller, and the first switch and the second switch.

7. The digital switch system of claim 6, wherein the printed circuit board includes a pair of sockets to accommodate a third switch for use, instead of the first switch, and a fourth switch for use instead of the second switch.

8. The digital switch system of claim 7, wherein the first and second switches are operable to output a first high voltage at a lower first current and whereas the third and the fourth switches are operable to output a second voltage lower than the first voltage and to produce a second current higher than that the first current.

9. The digital switch system of claim 2, wherein the controller includes a delay circuit for delaying outputting the second enable output for a predetermined time period after activation of the first enable output.

10. The digital switch system of claim 9, wherein the predetermined delay is programmable.

11. A method of switching an electrical output to a load in a manner which prevents accidental turn-on of the output to the load, the method comprising the steps of:

Providing a pulse of temporary power to an normally unpowered digital controller of the type that is operable to produce a first enable output and a second enable output;

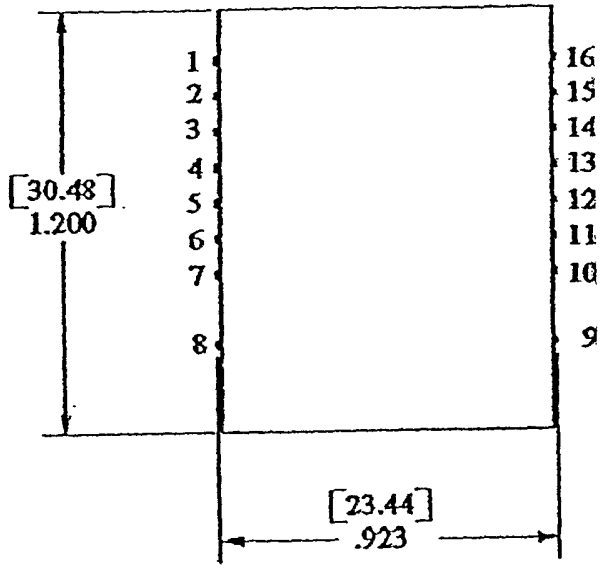
applying the first enable output of the controller to a first switch which is operable in response to the first enable output to provide a first output voltage, and coupling back the first output voltage of the first switch to the digital controller to continue powering the controller, even after said pulse of temporary power has been inactivated; and

applying the first output voltage to a second switch and coupling the second enable output to the second switch to cause the second switch to provide in response thereto, a second output voltage which is suitable for being coupled to the load.

12. The method of claim 11, including applying the pulse of temporary power through a diode.

13. The method of claim 11, including selectively applying a disable signal to the controller to render the controller inoperable, even in the presence of the pulse of temporary power.

14. The method of claim 11, including the outputting of the second enable output relative to the first enable output.



PIN NO.	FUNCTION
1	NC
2	GND
3	VIN
4	VIN
5	VIN
6	PROTECT
7	~~GND~~ PROTECT
8	GND
9	GND
10	VOUT
11	VOUT
12	VOUT
13	GND
14	GND
15	~~GND~~ POWER SW
16	POWER SW

Figure 1

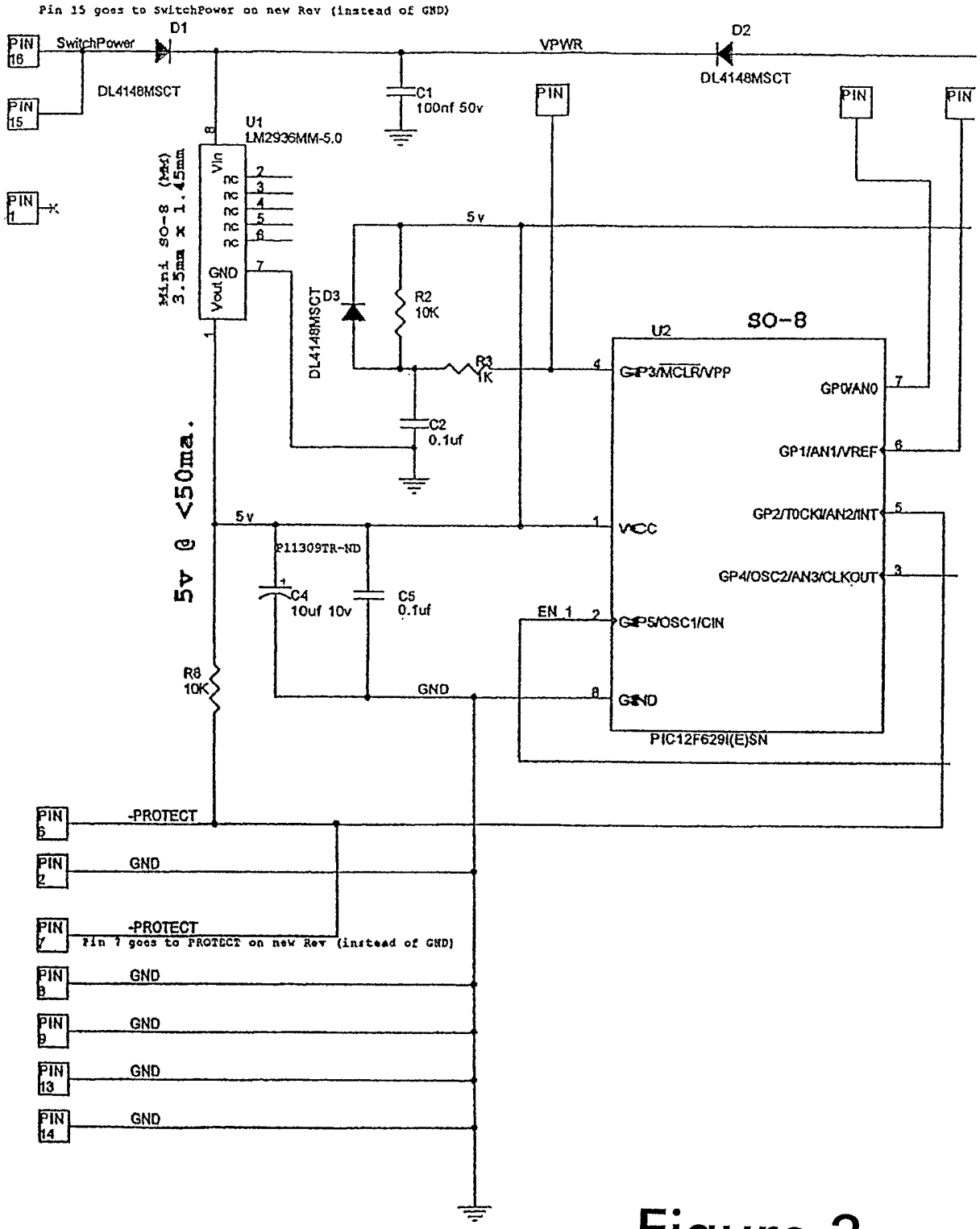

Pin 15 goes to SwitchPower on new Rev (instead of GND)
PIN 16
SwitchPower
D1
DL4148MSCT
PIN 15
VPWR
D2
DL4148MSCT
C1
100nf 50v
U1
LM2936MM-5.0
Mini SO-8 (Md)
3.5mm x 1.45mm
Vin
GND
Vout
PIN 1
5v
D3
DL4148MSCT
R2
10K
R3
1K
C2
0.1uf
U2
SO-8
GP3/MCLR/VPP
GP0/AN0
GP1/AN1/VREF
GP2/T0CKI/AN2/INT
GP4/OSC2/AN3/CLKOUT
GP5/OSC1/CIN
VCC
GND
EN 1
PIC12F629I(E)SN
5v @ <50ma.
P11309TR-ND
C4
10uf 10v
C5
0.1uf
R8
10K
PIN 6
-PROTECT
PIN 2
GND
PIN 7
-PROTECT
Pin 7 goes to PROTECT on new Rev (instead of GND)
PIN 8
GND
PIN 9
GND
PIN 13
GND
PIN 14
GND

Figure 2a

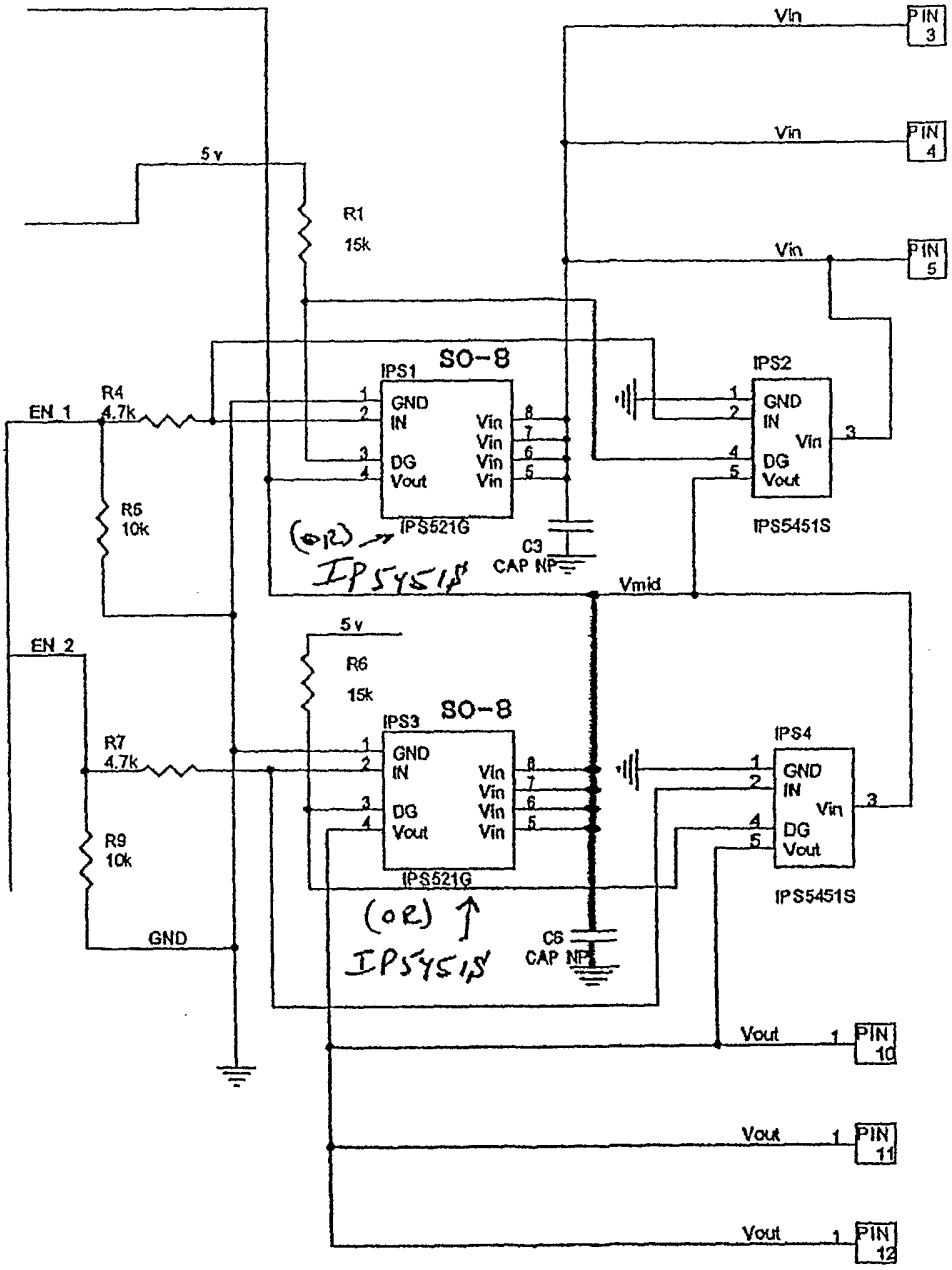

Vin
PIN 3
Vin
PIN 4
Vin
PIN 5
5 v
R1
15k
SO-8
IPS1
GND
IN
DG
Vout
Vin
IPS521G
IPS2
IPS5451S
R4
4.7k
EN_1
R5
10k
C3
CAP NP
Vmid
5 v
R6
15k
EN_2
SO-8
IPS3
IPS4
R7
4.7k
R9
10k
GND
C6
CAP NP
Vout
PIN 10
PIN 11
PIN 12

Figure 2b

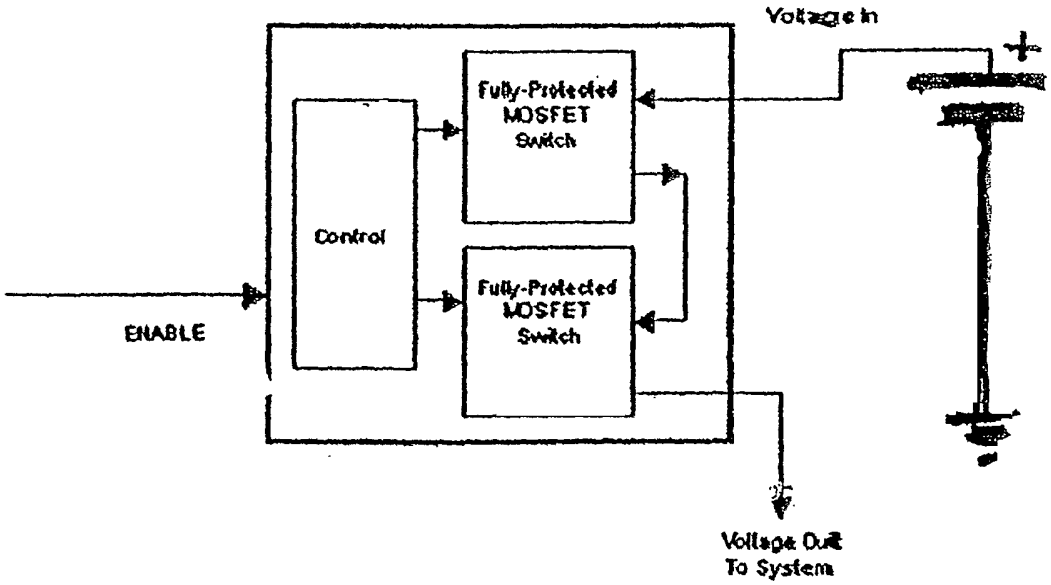

Voltage In
Fully-Protected MOSFET Switch
Control
Fully-Protected MOSFET Switch
ENABLE
Voltage Out To System

Figure 3