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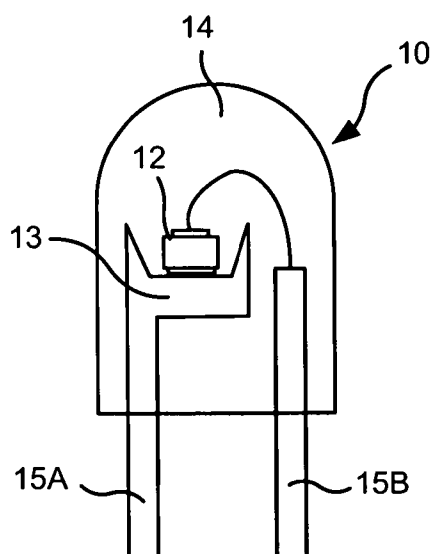
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[Continued on next page]

(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE PACKAGES AND METHODS



**FIGURE 1A**

(57) Abstract: A submount for a light emitting device package includes a rectangular substrate. A first bond pad and a second bond pad are on a first surface of the substrate. The first bond pad includes a die attach region offset toward a first end of the substrate and configured to receive a light emitting diode thereon. The second bond pad includes a bonding region between the first bond pad and the second end of the substrate and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate. First and second solder pads are on the second surface of the substrate. The first solder pad is adjacent the first end of the substrate and contacts the second bond pad. The second solder pad is adjacent the second end of the substrate and contacts the first bond pad. Related LED packages and methods of forming LED packages are disclosed.



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## SEMICONDUCTOR LIGHT EMITTING DEVICE PACKAGES AND METHODS

### FIELD OF THE INVENTION

**[0001]** This invention relates to semiconductor light emitting devices, and more particularly to packages for semiconductor light emitting devices.

### BACKGROUND

**[0002]** Light emitting diodes and laser diodes are well known solid state electronic devices capable of generating light upon application of a sufficient voltage. Light emitting diodes and laser diodes may be generally referred to as light emitting devices (LEDs). Light emitting devices generally include a p-n junction formed in an epitaxial layer grown on a substrate such as sapphire, silicon, silicon carbide, gallium arsenide and the like. The wavelength distribution of the light generated by the LED depends on the material from which the p-n junction is fabricated and the structure of the thin epitaxial layers that include the active region of the device.

**[0003]** Typically, an LED includes a substrate, an n-type epitaxial region formed on the substrate and a p-type epitaxial region formed on the n-type epitaxial region (or vice-versa). In order to facilitate the application of a voltage to the device, an anode ohmic contact is formed on a p-type region of the device (typically, an exposed p-type epitaxial layer) and a cathode ohmic contact is formed on an n-type region of the device (such as the substrate or an exposed n-type epitaxial layer).

**[0004]** In order to use an LED in a circuit, it is desirable to package the LED to protect it from environmental harm and mechanical damage. An LED package also includes means, such as electrical leads, for electrically connecting the LED chip to an external circuit. In a typical package 10 illustrated in FIG. 1A, an LED 12 is mounted on a reflective cup 13 by means of a solder bond or epoxy. One or more wirebonds connect the ohmic contacts of the LED to leads 15A, 15B which may be attached to or integral with the reflective cup 13. The entire assembly is then encapsulated in a

clear protective resin 14 which may be molded in the shape of a lens to collimate the light emitted from the LED chip 12.

**[0005]** In another conventional package 20 illustrated in FIG. 1B, a plurality of LED chips 22 are mounted onto a printed circuit board (PCB) carrier 23. One or more wirebond connections are made between ohmic contacts on the LEDs 22 and electrical traces 25A, 25B on the PCB 23. Each mounted LED 22 is then covered with a drop of clear resin 24 which may provide environmental and mechanical protection to the chip while also acting as a lens. The individual packaged LEDs 22 are then separated by sawing the PCB board 23 into small squares, each of which contains one or more LED chips 22.

**[0006]** One figure of merit for users of light emitting devices is cost per lumen, that is, the cost of obtaining a given level of light output. The high cost of conventional packaging techniques may be one factor that keeps the cost per lumen of solid state lighting relatively high. In addition, conventional packaging techniques may result in large, bulky packages that are unsuitable for certain miniaturized applications such as cellular telephone backlights. Conventional packaging techniques may also have poor thermal resistance characteristics that limit the power levels at which the LED chip may be driven and place constraints on system designers with respect to placement of LEDs.

**[0007]** Some packages for light emitting diodes are described in U.S. Pre-grant Publication Nos. 2004/0079957, 2004/0126913, and 2005/0269587 which are assigned to the assignee of the present invention, and which are incorporated herein by reference as if set forth fully herein.

## SUMMARY

**[0008]** Some embodiments of the invention provide a submount for a light emitting device package. The submount includes a generally rectangular substrate having a first surface and a second surface opposite the first surface, a first end and a second end opposite the first end. A first bond pad and a second bond pad are on the first surface of the substrate. The first bond pad may include a die attach region offset toward the first end of the substrate and configured to receive a light emitting diode thereon. The

second bond pad may include a bonding region that is between the first bond pad and the second end of the substrate and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate.

**[0009]** The substrate further includes first and second solder pads on the second surface of the substrate. The first solder pad is adjacent the first end of the substrate and the second solder pad is adjacent the second end of the substrate. The second bond pad is in electrical contact with the first solder pad, and the first bond pad is in electrical contact with the second solder pad.

**[0010]** The substrate may include a castellation at the corner of the substrate and an electrical trace on the castellation that extends from the first surface of the substrate to the second surface of the substrate and that electrically connects the second bond pad and the first solder pad.

**[0011]** The side of the substrate may include a first side and the corner of the substrate may include a first corner, and the first bond pad may further include a first bond pad extension that extends from the die attach region along a second side of the substrate, opposite the first side of the substrate, towards a second corner of the substrate at the second end of the substrate and diagonally opposed to the first corner.

**[0012]** The substrate may include a castellation at the second corner of the substrate. A second electrical trace may be on the second castellation and may extend from the first surface of the substrate to the second surface of the substrate to electrically connect the first bond pad and the second solder pad.

**[0013]** The submount may further include a neutral pad on the second surface of the substrate between the first solder pad and the second solder pad. The neutral pad may be electrically isolated from the first solder pad and the second solder pad.

**[0014]** The substrate may include an electrically insulating material, such as aluminum nitride, silicon carbide, diamond, and/or alumina.

**[0015]** The submount may further include at least one via hole through the substrate extending from the first surface of the substrate to the second surface of the substrate. A conductive material may be in the at least one via

hole and may electrically connect the first bond pad and the second solder pad.

**[0016]** The first bond pad may include a seed layer on the substrate and a thermal spreading layer on the seed layer. The thermal spreading layer may include a layer of copper having a thickness greater than about 5  $\mu\text{m}$ .

**[0017]** The first bond pad may further include a barrier layer on the thermal spreading layer opposite the seed layer, and a reflective layer on the barrier layer opposite the thermal spreading layer. The first bond pad may further include second barrier layer between the seed layer and the thermal spreading layer.

**[0018]** A light emitting device package according to some embodiments of the invention includes a generally rectangular substrate having a first surface and a second surface opposite the first surface, a first end and a second end opposite the first end, and a first bond pad on the first surface of the substrate. The first bond pad may include a die attach region offset from a center of the first surface toward the first end of the substrate and configured to receive a light emitting diode thereon. The substrate may further include a second bond pad on the first surface of the substrate including a bonding region that is between the first bond pad and the second end of the substrate, and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate.

**[0019]** The substrate further includes first and second solder pads on the second surface of the substrate. The first solder pad is adjacent the first end of the substrate and the second solder pad is adjacent the second end of the substrate. The second bond pad is in electrical contact with the first solder pad, and the first bond pad is in electrical contact with the second solder pad.

**[0020]** A light emitting device having an electrical contact is mounted on the first bond pad, and a bond wire is bonded to the electrical contact of the light emitting device and to the second bond pad.

**[0021]** An encapsulant may be on the first surface of the substrate. The encapsulant may include an integrated lens arranged over the light emitting device. The integrated lens may have an optical axis that is aligned

over a center of the light emitting device, so that the integrated lens is offset from a center of the substrate toward the first end of the substrate.

**[0022]** The package may further include an ESD protection chip including an electrical contact, the ESD protection chip mounted on the first bond pad, and a second bond wire electrically connecting the electrical contact of the ESD protection chip and the second bond pad.

**[0023]** The encapsulant may include a wavelength conversion material and/or a disperser. In some embodiments, the package may include a wavelength conversion material between the light emitting device and the encapsulant. The package may further include a secondary optical element on the encapsulant.

**[0024]** Some embodiments of the invention provide methods of forming a submount for a light emitting diode (LED) package. The methods include providing a generally rectangular substrate having a first surface and a second surface opposite the first surface, a first end and a second end opposite the first end, a first corner at the first end and a second corner at the second end and diagonally across the substrate from the first corner. A seed layer is formed on the first surface of the substrate, and is patterned to form a first bond pad pattern and a second bond pad pattern on the first surface of the substrate.

**[0025]** A first bond pad is formed on the first bond pad pattern. The first bond pad may include a die attach region offset from a center of the first surface toward the first end of the substrate and configured to receive a light emitting diode thereon. A second bond pad is formed on the second bond pad pattern. The second bond pad may include a bonding region that is between the first bond pad and the second end of the substrate and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate. The methods further include etching the first bond pad and the second bond pad to increase a separation between the first bond pad and the second bond pad.

**[0026]** The methods may further include forming first and second solder pads on the second surface of the substrate. The first solder pad may be formed adjacent the first end of the substrate and the second solder pad may

be formed adjacent the second end of the substrate. The second bond pad may be in electrical contact with the first solder pad and the first bond pad may be in electrical contact with the second solder pad.

**[0027]** The methods may further include removing material from the first corner and the second corner to provide respective first and second castellations at the first corner and the second corner. A first electrical via may be formed on the first castellation to electrically connect the second bond pad and the first solder pad. A second electrical via may be formed on the second castellation to electrically connect the first bond pad and the second solder pad.

**[0028]** Some embodiments of the invention provide methods of forming a plurality of packaged light emitting diodes. The methods include providing a sheet of ceramic material including a two-dimensional array of light emitting devices mounted thereon, providing a mold including a plurality of cavities therein, dispensing a liquid encapsulant material into respective ones of the plurality of cavities, and bringing the sheet of ceramic material into contact with the mold so that respective ones of the light emitting devices extend into a corresponding one of the plurality of cavities. The liquid encapsulant is at least partially cured so as to form encapsulant coatings around the respective light emitting devices.

**[0029]** The sheet of ceramic material may include a plurality of metallized holes therethrough, and the methods may further include separating the sheet of ceramic material along separation lines that extend through a subset of the plurality of holes to thereby define individual light emitting diode substrates including at least one castellation at a corner thereof including an electrical via thereon extending from a first surface of a substrate to a second surface of the substrate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0030]** The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate certain embodiment(s) of the invention. In the drawings:



**[0031]** Figures 1A and 1B illustrate some conventional packaged light emitting devices (LEDs).

**[0032]** Figures 2A to 2C are plan, bottom and sectional views, respectively, of a submount for an LED package according to some embodiments of the invention;

**[0033]** Figure 2D is a partial cross section of a substrate including a metal stack according to some embodiments of the invention.

**[0034]** Figures 3A and 3B are plan and perspective views, respectively, of a submount for an LED package on which an LED chip has been mounted, according to some embodiments of the invention; and

**[0035]** Figures 4A to 4C are side, top perspective and bottom perspective views, respectively, of an LED package according to some embodiments of the invention;

**[0036]** Figures 5A to 5C are plan, top perspective and bottom perspective views, respectively, of a submount for an LED package on which an LED chip has been mounted, according to further embodiments of the invention;

**[0037]** Figures 6A and 6B are side and perspective views, respectively, of an LED package according to further embodiments of the invention;

**[0038]** Figures 7A and 7B are bottom and perspective views, respectively, of a submount for an LED package according to further embodiments of the invention;

**[0039]** Figure 8 is a plan view of a group of connected submounts prior to separation, according to some embodiments of the invention;

**[0040]** Figure 9 is a plan view of a sheet of submounts according to some embodiments of the invention;

**[0041]** Figures 10A to 10C illustrate packaging systems/methods according to some embodiments of the invention;

**[0042]** Figures 11A to 11C illustrate packaging systems/methods according to further embodiments of the invention;

**[0043]** Figure 12 is a flowchart illustrating systems/methods according to some embodiments of the invention. It's safe

## DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

**[0044]** The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like numbers refer to like elements throughout.

**[0045]** It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. It will be understood that if part of an element, such as a surface, is referred to as "inner," it is farther from the outside of the device than other parts of the element. Furthermore, relative terms such as "beneath" or "overlies" may be used herein to describe a relationship of one layer or region to another layer or region relative to a substrate or base layer as illustrated in the figures. It will be understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures. Finally, the term "directly" means that there are no intervening elements. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

**[0046]** It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

**[0047]** As used herein, the term semiconductor light emitting device may include a light emitting diode, laser diode and/or other semiconductor

device which includes one or more semiconductor layers, which may include silicon, silicon carbide, gallium nitride and/or other semiconductor materials, a substrate which may include sapphire, silicon, silicon carbide and/or other microelectronic substrates, and one or more contact layers which may include metal and/or other conductive layers. In some embodiments, ultraviolet, blue and/or green light emitting diodes ("LEDs") may be provided. Red and/or amber LEDs may also be provided. The design and fabrication of semiconductor light emitting devices are well known to those having skill in the art and need not be described in detail herein.

**[0048]** Figures 2A to 2C are plan, bottom and sectional views, respectively, of a submount 30 for an LED package according to some embodiments of the invention. In particular, Figure 2C is a cross section of the submount 30 taken along line C-C of Figures 2A and 2B.

**[0049]** Referring to Figures 2A to 2C, a submount 30 includes a generally rectangular substrate 32 having a first side 31 and a second side 33. A first bondpad 36 and a second bond pad 34 are formed on the first side 31 of the substrate 32. The first bond pad 36 includes a die attach region 36A that is offset from a center of the substrate 32 towards a first end 32A of the substrate 32. The second bond pad 34 includes a bonding region 34A that is between the die attach region 36A and a second end 32B of the substrate 32, that is opposite the first end 32A.

**[0050]** The second bond pad 34 includes a second bond pad extension 34B that extends from the bonding region 34A along a side 32D of the substrate 32 toward a corner 35A of the substrate 32 at the first end 32A of the substrate 32.

**[0051]** First and second solder pads 46, 44 are formed on the second side 33 of the substrate 32. The first solder pad 46 is adjacent the first end 32A of the substrate 32, and the second solder pad 44 is adjacent the second end 32B of the substrate 32. The second bond pad 34 is in electrical contact with the first solder pad 46 and the first bond pad 36 is in electrical contact with the second solder pad 44.

**[0052]** The substrate 32 includes a castellation 40A at the corner 35A of the substrate 32. An electrical trace 42A on the castellation 40A extends from the first surface 31 of the substrate 32 to the second surface 33 of the

substrate 32. The electrical trace 42 electrically connects the second bond pad 34 and the first solder pad 46.

**[0053]** The first bond pad further includes a first bond pad extension 36B that extends from the die attach region 36A along a second side 32C of the substrate 32, opposite the first side 32D of the substrate 32, towards a second corner 35B of the substrate 32 at the second end 32B of the substrate 32 and diagonally opposed to the first corner 35A across the substrate 32.

**[0054]** The substrate 32 includes a castellation 40B at the second corner 35B of the substrate 32. A second electrical trace 42B is formed in the second castellation 40B and extends from the first surface 31 of the substrate 32 to the second surface 33 of the substrate 32. The second electrical trace 42B electrically connects the first bond pad 36 and the second solder pad 44.

**[0055]** In some embodiments, the submount 30 may include at least one via hole 38 through the substrate 32 extending from the first surface 31 of the substrate 32 to the second surface 33 of the substrate 32. A conductive material, such as metal, deposited in the via hole 38 electrically connects the first bond pad 36 and the second solder pad 44, as shown in Figure 2C.

**[0056]** The substrate 32 may include a nonconductive material such as alumina, aluminum nitride, silicon carbide and/or chemical vapor deposited (CVD) diamond on which a plurality of electrical traces (not shown) may be formed. The substrate 32 may in some cases include a composite of ceramics and/or organic materials and/or metals. The thermal conductivity of aluminum nitride and silicon carbide is about 200 W/MK, while the thermal conductivity of CVD diamond is about 800 W/MK. The thickness of the substrate 32 may be from about 150 to about 400  $\mu\text{m}$ , although other thicknesses may be used.

**[0057]** In some embodiments, the specific heat of a material may be considered in selecting an appropriate material for the substrate 32. For example, in some applications, such as camera flashes, it may be desirable for a material to have a high thermal capacity (thermal mass) in order to absorb a high heat flux that is generated for a very brief time, which may increase the transient temperature dissipation time constant of the package. This may particularly be desirable for applications in which an external heatsink is not provided. As alumina may have about 44% more thermal

capacitance than AlN, alumina may be an appropriate choice of material for the substrate 32 for some applications, and in particular for applications in which an external heat sink is not provided. In some embodiments, a 96% alumina substrate having a thickness of about 340  $\mu\text{m}$  and a flatness of about 0.015 mm/linear mm may be used for the substrate 32.

**[0058]** The first bond pad 36 and the second bond pad 34 may include relatively thick traces for improved electrical and/or thermal conductivity. In particular, the first bond pad 36 and the second bond pad 34 may include about 75  $\mu\text{m}$  thick copper plating.

**[0059]** In some embodiments, the first bond pad 36 and the second bond pad 34 may be formed by sputtering a thin seed layer of platinum or titanium/platinum onto the substrate 32 and forming a thick layer on the seed layer. For example, the first bond pad 36 is illustrated in partial cross section in Figure 2D. The first bond pad 36 includes a seed layer 36a, an optional first barrier layer 36b on the seed layer 36a, and a relatively thick thermal spreading layer 36c on the first barrier layer 36b. A second barrier layer 36d is on the thermal spreading layer 36c, and a reflector 36e is on the second barrier layer 36d. The second bond pad 34 will typically be formed at the same time as the first bond pad 36 and may have the same structure as the first bond pad 36.

**[0060]** The seed layer 36a, which may have a thickness of about 0.006  $\mu\text{m}$ , may be sputtered onto the substrate 32 and then may be patterned using standard lithographic processes to form the desired outline of the bond pads 36, 34. The optional barrier layer 36b, which may include about 0.2 of nickel, may then be formed on the seed layer 36a.

**[0061]** A thermal spreading layer 36c as described above may then be formed on the seed layer 36a, for example, using an electrolytic or electroless plating technique. The thermal spreading layer 36c may include a layer of copper having a thickness of about 5  $\mu\text{m}$  up to hundreds of microns thick, and in some cases may be about 75  $\mu\text{m}$  thick. The thickness of the thermal spreading layer 36c will influence the heat transfer properties of the package. A thicker thermal spreading layer 36c may preferentially spread heat laterally, while a thinner thermal spreading layer 36c may preferentially spread heat

vertically. Thus, a thinner thermal spreading layer 36c may be used with a substrate 32 having a larger thermal conductivity for vertical heat spreading.

**[0062]** A clean-up etch, such as a wet copper etch, may be performed to remove any material undesirably bridging between the bond pads 36, 34. The second barrier layer 36d, which may include nickel, may then be formed on the thermal spreading layer 36c. The second barrier layer 36d may have a thickness of about 0.2  $\mu\text{m}$  to about 2  $\mu\text{m}$ . The reflective layer 36e may be formed on the second barrier layer 36d. The reflective layer 36e may include silver having a thickness of 2  $\mu\text{m}$  or more, and may improve light extraction.

**[0063]** A bonding layer (not shown), such as a layer of gold, may also be provided on the reflective layer 36e and/or the barrier layer 36d.

**[0064]** The thick thermal spreading layer 36c may provide improved heat spreading/extraction for the package. Furthermore, the thick thermal spreading layer 36c may enable heat to be quickly diffused into the core of the substrate 32. Once heat flux is diffused into the substrate 32, it may be extracted into an external heatsink, such as an MCPCB and/or heatsink fins, via a thermal joint. Heat may also be extracted from the substrate through natural and/or forced convection.

**[0065]** The electrical traces 42A, 42B and/or the first and second solder pads 46, 44 may be formed in a manner similar to the bond pads 36, 34. The vias 38 may be filled, for example, with copper.

**[0066]** An LED chip may be mounted onto the first bond pad 36 or the second bond pad 34 by solder joints, eutectoid joints, and/or Ag-epoxy joints. The first and/or second solder pad 46, 44 can be soldered or chemically bonded to external interconnects. It will be appreciated that any suitable surface of the substrate 32 can be metallized to form a terminal and/or heatsink pad for external electrical and/or heatsink interconnects to meet a particular application requirement.

**[0067]** Due in part to the configuration of the bond pads 36, 34, the castellations 40A, 40B, the vertical traces 42A, 42B and the solder pads 46, 44, an LED package as illustrated herein may include a substrate 32 having a single layer of material, which may simplify manufacturing processes and/or reduce manufacturing costs compared to packages including multiple layers for electrical routing purposes.

**[0068]** Furthermore, the use of castellations 40A, 40B to located the traces 42A, 42B may free up space on the surfaces 31, 33 of the substrate 32 that can be used, for example, for mounting chips, connecting wirebonds, or other purposes. The castellations 40A, 40B can also be used as electrical contacts, providing increased flexibility for mounting the package.

**[0069]** Figures 3A and 3B are plan and perspective views, respectively, of a submount 30 for an LED package on which an LED chip 50 has been mounted. The LED chip 50 includes a pair of bond pads 54 and a current spreading network 56 on an upper surface thereof. The bond pads 54 of the LED chip 50 may provide cathode (-) connections to the LED chip 50, while the anode (+) connection of the LED chip may be in electrical contact with the first bonding region 36A of the first bond pad 36. The cathode of the LED chip 50 is electrically connected to the bonding region 34A of the second bond pad 34 by at least one wire bond connection 52 that may include, for example, a gold or aluminum wire.

**[0070]** The cathode of the LED chip 50 is thereby electrically connected to the first solder pad 46 on the second side of the substrate 32, which is located adjacent the first end 32A of the substrate. Accordingly, both the center of the LED chip 50 and the solder pad 46 corresponding to the cathode of the LED chip 50 may be offset towards the same end of the substrate 32. This configuration may provide a desirable optical and/or electrical arrangement for the resulting package.

**[0071]** As can be seen in Figures 3A and 3B, a substrate 32 may have a surface area that is only about 2-3 times the size of the LED chip 50 mounted thereon, to provide a truly chip-scale package.

**[0072]** Figures 4A to 4C are side, top perspective and bottom perspective views, respectively, of an LED package 100 according to some embodiments of the invention. As shown in Figures 4A to 4C, an encapsulant 60 is formed over the first surface 31 of the substrate 32 to provide mechanical and/or environmental protection for the LED chip 50, as well as the first and second bond pads 36, 36 and the wire bond connections 52.

**[0073]** Accordingly, the finished package may have a three-dimensional solid body. While a rectangular body is illustrated in Figures 4A to 4C, the

package body may have a rectangular, square, semihemispheric, parabolic or other regular and/or irregular shape.

**[0074]** The encapsulant 60 may be optically transparent and/or may provide an appropriate index of refraction to match the chip 50 encapsulated therein and/or to provide a transition to an external index of refraction in order to increase light extraction from the package.

**[0075]** Additives such as wavelength conversion materials (e.g. phosphors) and/or dispersers can be added to the encapsulant 60. In some embodiments, a wavelength conversion material, such a phosphors embedded in an optical medium such as a silicone gel can be coated onto the chip 50 before formation of the encapsulant 60.

**[0076]** Figures 5A and 5B are plan and top perspective views, respectively, of a submount 130 for an LED package according to further embodiments of the invention. As shown therein, the substrate 32 may include generally semi-circular castellations 40C, 40D at opposite corners thereof.

**[0077]** Moreover, an electrostatic discharge (ESD) protection chip 62 may be mounted in parallel with the LED 50 to provide ESD protection to the LED chip 50. As shown in Figures 5A and 5B, the ESD protection chip is mounted on the first bond pad 36 along with the LED chip 50. In particular, the ESD chip 62 may be mounted on the first bond pad extension 36B. A wire bond connection 64 connects the ESD protection chip 62 to the second bond pad 34.

**[0078]** Figures 6A and 6B are side and perspective views, respectively, of an LED package 200 according to further embodiments of the invention. The LED package 200 includes an encapsulant 60 on the first side of the substrate 32. The encapsulant 60 includes an optical element, such as an integrated lens portion 60A that is offset from a center of the substrate 32 towards the first end 32A of the substrate. In particular, an optical axis 70 of the lens portion 60A may be vertically aligned with a center of the LED chip 50, which is also offset towards the first end 32A of the substrate 32.

**[0079]** An optical element, such as the lens portion 60A, that is integral with the encapsulant body 60 may improve the luminous efficiency of the



package and/or may provide a desired radiation pattern for the packaged device.

**[0080]** As is apparent from Figures 6A and 6B, the optical center of the package may be placed in any desired location, including the geometrical center of the package. The bond pads 36, 34 may be modified from the configurations illustrated herein in order to achieve a package having a desired shape.

**[0081]** Furthermore, additional optical elements may be added to the package 100 after formation thereof. For example, a secondary optical element such as a lens, reflector and/or other imaging or non-imaging component can be bonded to the encapsulant 60 using a refractive index-matching adhesive.

**[0082]** Figures 7A and 7B are bottom and perspective views, respectively, of a submount 230 for an LED package according to further embodiments of the invention. In addition to first and second solder pads 46, 44, the submount 230 includes a neutral pad 48 on the second surface 33 of the substrate 32 between the first solder pad 46 and the second solder pad 44. The neutral pad 48 is electrically isolated from the first solder pad 46 and the second solder pad 44; and may be used to provide a thermal connection between the submount 230 and a surface on which the submount 230 is mounted. The neutral pad 48 may have the same material composition as the first and second solder pads 46, 44 (which, in turn, may be formed in the manner described above with respect to the first and second bond pads 36, 34).

**[0083]** Some embodiments of the invention provide methods of forming submounts. In some embodiments, a sheet of a submount material, such as a sheet of ceramic material, may be patterned and metallized to form a plurality of connected submounts 32. For example, Figure 8 is a plan view of a rectangular piece 72 including a group of four connected substrates 32-1 to 32-4 prior to separation thereof. The group of substrates 32-1 to 32-4 are defined by forming a square castellation hole 140B at a center of the rectangular piece 72, which forms the second castellation 40B for each of the substrates 32-1 to 32-4. Square castellation holes 140A are formed at the corners of the rectangular piece 72, and provide the first castellations 40A for

each of the substrates 32-1 to 32-4. Since a single square castellation hole 140B forms four castellations 40B (i.e. one for each of the substrates 32-1 to 32-4), when the substrates 32-1 to 32-4 are separated along horizontal and vertical separation lines 75, 77, the size of the castellations 40B may be reduced.

**[0084]** Figure 9 is a plan view of a sheet 74 of rectangular pieces 72, each of which may include four substrates 32-1 to 32-4, according to some embodiments of the invention. Accordingly, the substrates 32 may be fabricated in large numbers by patterning and metallizing many substrates 32 at once. Figure 9 also illustrates castellation holes 140B at the centers of the pieces 72 and castellation holes 140A arranged at corners of the pieces. When the individual substrates 32 are separated, for example by sawing the sheet 74 along horizontal separation lines 75 and vertical separation lines 77, each resulting substrate 32 will have first and second castellations 40A, 40B at opposite corners thereof on which electrical traces 42A and 42B are respectively formed. The sheet 74 may also include alignment features 73, such as 1/4 circle holes at corners thereof and a 1/2 circle hole at an edge thereof, which may be used to align the sheet 74 in manufacturing processes from die attach through encapsulation and sawing.

**[0085]** Figures 10A to 10C illustrate packaging systems/methods according to some embodiments of the invention. As shown therein, a mold 80 including a plurality of mold cavities 81 is provided. The mold cavities 81 are separated by sidewalls 82 and are arranged to correspond to individual submounts 30 in a sheet 74 of metallized submounts 30 on which LED chips 50 have been mounted. A liquid casting material 68, such as a clear liquid thermoset material, is dispensed into the cavities 81, and the sheet 74 is brought into contact with the mold 80 so that the LED chips 50 extend into the mold cavities 81 and become covered with the casting material 68. The casting material 68 is then at least partially cured, for example by heating.

**[0086]** After the casting material has been at least partially cured, the sheet 72 is separated from the mold 80, as shown in Figure 10B, leaving solidified encapsulant coatings 60 on the LED chips 50. The submounts 30 may then be separated from one another, as shown in Figure 10C, to form singulated packaged LEDs 100. In particular, the submounts 30 may be

separated by sawing through the sheet 74 through the holes 140B, 140A, to leave castellations 40A, 40B in the corners of the substrates 32.

**[0087]** It may be beneficial to provide separate cavities 81 for each LED package being cast in order to reduce the effect of differences in coefficient of thermal expansion (CTE) between the casting material 68 and the material of the substrate sheet 74. For example, if the casting material 68 were cast over an entire sheet 74, differences in CTE between the casting material 68 and the sheet 74 may cause undesired cracking, warping and/or de-lamination of the encapsulant coatings 60.

**[0088]** Figures 11A to 11C illustrate packaging systems/methods according to further embodiments of the invention. In the embodiments illustrated in Figures 11A to 11C, a mold 90 including a plurality of individual mold cavities 91 is provided. The individual mold cavities 91 are separated by sidewalls 92 and are arranged to correspond to individual submounts 30 in a sheet 74 of metallized submounts 30 on which LED chips 50 have been mounted. Furthermore, each mold cavity 91 includes a lens molding surface 94 that is shaped to mold the casting material 68 into a desired lens shape at a desired location on the substrate 32.

**[0089]** As shown in Figure 11B, when the encapsulant 60 is formed, it includes an integral lens portion 60A corresponding to the lens molding surface 94.

**[0090]** Figure 12 is a flowchart illustrating systems/methods according to some embodiments of the invention. A panel of substrate material, such as a panel of alumina and/or AlN is provided. A plurality of castellation holes 140B, and optionally, via holes 38, may be formed in the panel, for example, by etching (Block 510). The panel is then metallized to form bond pads, solder pads, and conductive vias in the via holes 38 and/or the castellation holes 140B (Block 520).

**[0091]** A plurality of LED chips are then mounted on respective bond pads on the panel (Block 530). Optionally, a plurality of ESD protection chips may also be mounted on corresponding bond pads. Wire bonds may then be formed from the chips to corresponding bond pads (Block 540).

**[0092]** An encapsulant material, such as a thermoset, may then be cast over the chips (Block 550). As described above, a mold including individual

mold cavities may be at least partially filled with a liquid encapsulant material, and the panel may be placed in contact with the mold, so that the chips on the panel extend into the mold cavities. The mold may be pressurized, and may be at least partially cured before separating the panel from the mold.

**[0093]** A thermoset that may be used according to some embodiments of the invention may include an epoxy, polyimide, a phenolic resin and/or any other thermosettable material. A thermoset for use in some embodiments of the invention can be transfer molded onto a leadframe, such as a stamped or etched dual-gauge leadframe. Other types of molding may be used to form a body on a leadframe, such as injection molding and/or casting.

**[0094]** When the thermoset is chemically cross-linked (i.e., cured), it will chemically bond to the substrate to form a robust 3-dimensional solid thermoset body.

**[0095]** A thermoset body may offer enhanced structural and/or environmental protection to the device(s) mounted in the package compared to other types of materials.

**[0096]** Thermoset materials, such as thermosetting plastics are polymer materials that may be dispensed in precursor form, such as a resin, and then cured to a stronger form through the addition of energy, such as heat (generally near 200 °C) or irradiation. The curing process transforms the resin into a solid plastic by a cross-linking process in which the molecular chains of the material react at chemically active sites and link into a rigid, three-dimensional structure. The cross-linking process forms a molecule with a larger molecular weight, resulting in a material with a higher melting point or that simply changes to carbon and residue without melting. Thus, a thermoset material may not be melted and re-shaped after it is cured. As a result of the formation of a three-dimensional network of bonds during the cross-linking phase, thermoset materials are generally stronger than thermoplastic materials. Thus, thermoset materials may be better suited for high-temperature applications than thermoplastic materials.

**[0097]** Most thermosets, such as epoxy and/or polyimide, will bond to organic and/or inorganic surfaces when they come into contact with the surface during the cross-linking (curing) phase. This bond at the surface may be very strong and/or may be impervious to fluids or gases, such that a soft-

gel encapsulant surrounding the semiconductor device(s) mounted in the package may not leak out. Furthermore, the bond between the thermoset and the leadframe may reduce or prevent the entry of moisture into the package, which could otherwise cause device failure.

**[0098]** In contrast, in a package including a thermoplastic molded body, there may be no bonding between the plastic body and the surface on which it is molded. As such, fluids and/or gases can pass in both directions through the interface between the thermoplastic and the leadframe. Accordingly, an advantage of using thermosets such as epoxy or phenolic resin may be found in the bonding and sealing properties of thermosets at the interface with an organic and/or inorganic surface on which it is molded. This bonding may reduce and/or prevent moisture and/or other fluids or gases from passing through the interface. Thus, a thermoset may provide a higher degree of hermeticity at the interface than a thermal plastic can offer.

**[0099]** Many thermosets can withstand temperatures in excess of 350 °C without becoming deformed or distorted. In general, thermosets may be able to withstand higher temperatures than conventional thermoplastic materials, such as PPA (e.g., Amodel®) and/or LCP (e.g., Vectra®), each of which can only withstand temperatures up to about 280 °C. Accordingly, most thermal plastic materials cannot withstand the high solder reflow temperatures typically used for surface mount technology, which may be used to mount some LED packages.

**[00100]** Thermosets, such as many epoxies, can be molded by transfer molding, compression molding and/or casting processes to create plastic bodies having very fine details and/or intricate designs. During the molding/casting process, a thermoset may typically first transform into a flowable state before it is cured into a solid state. During this fluid state, high pressure can be applied to the material to allow the fluidic resin to fill even very small crevices in a mold. A thermal plastic may not be able to fill spaces as small as a thermoset can, because the injection mold for a thermal plastic is typically set at a temperature below the melting temperature of the thermal plastic, which may start to cool the thermal plastic to a solid state as soon as it enters the mold cavity.

**[00101]** Examples of thermoset materials are epoxy resins and phenol-novolac resins from Nitto Denko. Such materials may be loaded with filler particles, such as spherical fused silica and/or irregularly-shaped TiO<sub>2</sub> (titanium dioxide) solid particles, and/or carbon fibers at predetermined percentage by weight in order to obtain desired physical properties, such as coefficient of thermal expansion (CTE), flexural modulus, optical surface reflectance, heat deflection temperature (HDT), etc.

**[00102]** The thermoset resin, in solid or liquid form, is then loaded or dispensed into the mold cavity, which is set at a high temperature (typically at about 175 °C). Pressure (hundreds of psia) is applied to the thermoset resin to push the resin into the runner system of the mold. At this time, the solid resin will melt into a solution of very low viscosity. The liquid resin may then flow easily through the mold runners into the mold cavities, filling small crevices and corners. The pressure on the mold is increased to about 1,000 psia to pack the resin into the smallest gaps in the mold.

**[00103]** Inside the mold cavities, the liquid thermoset is continuously subjected to the high mold temperature of about 175 °C or more and a high material pressure of about 1,000 psia. Under these conditions, the liquid thermoset will solidify/cure in about 3-5 minutes. As noted above, when a thermoset cures, a cross-linking process occurs in which its constituent monomers or polymers chemically react with one another to form large, three-dimensional molecules that give solid thermoset material rigidity and a high melting point. The cross-linking action also causes the thermoset to chemically adhere or bond to the dual-gauge leadframe, imparting high mechanical stability to the resulting body/leadframe structure as well as providing a tight seal to the leadframe. This phenomenon of bonding may be desirable for a package for a semiconductor light emitting diode, in that an encapsulant can then be contained and retained inside without leaking out from the package.

**[00104]** Since the thermoset resin bonds readily to surfaces, the mold cavity may be made of hardened mold steel and polished to a mirror finish to reduce the tendency of the hardened thermoset to bond to the mold cavity. In addition, strong ejectors may be used to eject the molded panel from the mold. In some embodiments, the mold may have a Teflon® coating to

promote separation and/or a mold release material may be provided in the cavities 81, 91 to promote separation.

**[00105]** After separation of the panel from the mold, the packaged chips may be separated from the panel (Block 560) to provide individual chip-scale packaged diodes.

**[00106]** Packaged light emitting diodes according to some embodiments of the invention may provide improved luminous flux per unit area, due in part to the chip-scale size of the package footprint. For example, a package according to some embodiments of the invention that includes a model EZXT-1000 LED power chip manufactured by Cree, Inc., operating at 350 mA and 100% duty cycle can deliver about 26 lumens/mm<sup>2</sup> or more. Such a package may be particularly useful in applications in which a small, lightweight package is desirable, such as portable security lights, camera flashes, and/or backlighting for portable electronic devices. Furthermore, some embodiments may be mounted together in a cluster to provide a high-intensity light source in applications such as automotive headlamps, brake lamps, traffic lamps, etc. Providing package-level optical elements, such as the lens 60A, may also ease the design and/or manufacture of secondary optical elements in systems using packages according to embodiments of the invention.

**[00107]** The foregoing description is illustrative of the present invention and is not to be construed as limiting thereof. Although a few exemplary embodiments of this invention have been described, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention as defined in the claims. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims. The invention is defined by the following claims, with equivalents of the claims to be included therein.

That which is claimed is:

1. A submount for a light emitting device package, comprising:
  - a generally rectangular substrate having a first surface and a second surface opposite the first surface, a first end and a second end opposite the first end;
  - a first bond pad on the first surface of the substrate, wherein the first bond pad includes a die attach region offset toward the first end of the substrate and configured to receive a light emitting diode thereon;
  - a second bond pad on the first surface of the substrate, wherein the second bond pad includes a bonding region that is between the first bond pad and the second end of the substrate and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate; and
  - first and second solder pads on the second surface of the substrate, wherein the first solder pad is adjacent the first end of the substrate and the second solder pad is adjacent the second end of the substrate, and wherein the second bond pad is in electrical contact with the first solder pad and the first bond pad is in electrical contact with the second solder pad.
2. The submount of Claim 1, wherein the substrate includes a castellation at the corner of the substrate and an electrical trace on the castellation that extends from the first surface of the substrate to the second surface of the substrate and that electrically connects the second bond pad and the first solder pad.
3. The submount of Claim 1, wherein the side of the substrate comprises a first side and the corner of the substrate comprises a first corner, and wherein the first bond pad further comprises a first bond pad extension that extends from the die attach region along a second side of the substrate, opposite the first side of the substrate, towards a second corner of the substrate at the second end of the substrate and diagonally opposed to the first corner.



4. The submount of Claim 3, wherein the substrate includes a castellation at the second corner of the substrate, and a second electrical trace on the second castellation that extends from the first surface of the substrate to the second surface of the substrate and that electrically connects the first bond pad and the second solder pad.

5. The submount of Claim 1, further comprising a neutral pad on the second surface of the substrate between the first solder pad and the second solder pad, wherein the neutral pad is electrically isolated from the first solder pad and the second solder pad.

6. The submount of Claim 4, wherein the first corner and the second corner are diagonally opposed to one another across the substrate.

7. The submount of Claim 1, wherein the substrate comprises an electrically insulating material.

8. The submount of Claim 7, wherein the substrate comprises aluminum nitride, silicon carbide, diamond, and/or alumina.

9. The submount of Claim 1, further comprising at least one via hole through the substrate extending from the first surface of the substrate to the second surface of the substrate, and a conductive material in the at least one via hole and electrically connecting the first bond pad and the second solder pad.

10. The submount of Claim 1, wherein the first bond pad includes:  
a seed layer on the substrate; and  
a thermal spreading layer on the seed layer, wherein the thermal spreading layer comprises a layer of copper having a thickness greater than about 5  $\mu\text{m}$ .

11. The submount of Claim 10, wherein the first bond pad further comprises a barrier layer on the thermal spreading layer opposite the seed layer.

12. The submount of Claim 11, wherein the first bond pad further comprises a reflective layer on the barrier layer opposite the thermal spreading layer.

13. The submount of Claim 10, wherein the first bond pad further comprises a first barrier layer on the thermal spreading layer opposite the seed layer and a second barrier layer between the seed layer and the thermal spreading layer.

14. A light emitting device package, comprising:

- a generally rectangular substrate having a first surface and a second surface opposite the first surface, a first end and a second end opposite the first end;

- a first bond pad on the first surface of the substrate, wherein the first bond pad includes a die attach region offset from a center of the first surface toward the first end of the substrate and configured to receive a light emitting diode thereon;

- a second bond pad on the first surface of the substrate, wherein the second bond pad includes a bonding region that is between the first bond pad and the second end of the substrate and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate;

- first and second solder pads on the second surface of the substrate, wherein the first solder pad is adjacent the first end of the substrate and the second solder pad is adjacent the second end of the substrate, and wherein the second bond pad is in electrical contact with the first solder pad and the first bond pad is in electrical contact with the second solder pad;

- a light emitting device having an electrical contact and mounted on the first bond pad;

a bond wire bonded to the electrical contact of the light emitting device and to the second bond pad; and  
an encapsulant on the first surface of the substrate.

15. The package of Claim 14, wherein the encapsulant comprises an integrated lens arranged over the light emitting device, wherein the integrated lens has an optical axis that is aligned over a center of the light emitting device, so that the integrated lens is offset from a center of the substrate toward the first end of the substrate.

16. The package of Claim 14, further comprising an ESD protection chip including an electrical contact, the ESD protection chip mounted on the first bond pad, and a second bond wire electrically connecting the electrical contact of the ESD protection chip and the second bond pad.

17. The package of Claim 14, wherein the substrate includes a castellation at the corner of the substrate and an electrical trace on the castellation that extends from the first surface of the substrate to the second surface of the substrate and that electrically connects the second bond pad and the first solder pad.

18. The package of Claim 14, wherein the first bond pad further comprises a first bond pad extension that extends from the die attach region along a second side of the substrate towards a second corner of the substrate at the second end of the substrate.

19. The package of Claim 18, wherein the substrate includes a castellation at the second corner of the substrate, and a second electrical trace on the second castellation that extends from the first surface of the substrate to the second surface of the substrate and that electrically connects the first bond pad and the second solder pad.

20. The package of Claim 19, wherein the first corner and the second corner are diagonally opposed to one another across the substrate.

21. The package of Claim 14, further comprising a neutral pad on the second surface of the substrate between the first solder pad and the second solder pad, wherein the neutral pad is electrically isolated from the first solder pad and the second solder pad.

22. The package of Claim 14, wherein the substrate comprises an electrically insulating material.

23. The package of Claim 22, wherein the substrate comprises aluminum nitride and/or alumina.

24. The package of Claim 14, further comprising at least one via hole through the substrate extending from the first surface of the substrate to the second surface of the substrate, and a conductive material in the at least one via hole and electrically connecting the first bond pad and the second solder pad.

25. The package of Claim 14, wherein the encapsulant comprises a wavelength conversion material and/or a disperser.

26. The package of Claim 14, further comprising a wavelength conversion material between the light emitting device and the encapsulant.

27. The package of Claim 14, further comprising a secondary optical element on the encapsulant.

28. A method of forming a submount for a light emitting diode (LED) package, comprising:

providing a generally rectangular substrate having a first surface and a second surface opposite the first surface, a first end and a second end opposite the first end, a first corner at the first end and a second corner at the second end and diagonally across the substrate from the first corner;

forming a seed layer on the first surface of the substrate;

patterning the seed layer to form a first bond pad pattern and a second bond pad pattern on the first surface of the substrate;

forming first bond pad on the first bond pad pattern, wherein the first bond pad includes a die attach region offset from a center of the first surface toward the first end of the substrate and configured to receive a light emitting diode thereon;

forming a second bond pad on the second bond pad pattern, wherein the second bond pad includes a bonding region that is between the first bond pad and the second end of the substrate and a second bond pad extension that extends from the bonding region along a side of the substrate toward a corner of the substrate at the first end of the substrate; and

etching the first bond pad and the second bond pad to increase a separation between the first bond pad and the second bond pad.

29. The method of Claim 28, further comprising forming first and second solder pads on the second surface of the substrate, wherein the first solder pad is adjacent the first end of the substrate and the second solder pad is adjacent the second end of the substrate, and wherein the second bond pad is in electrical contact with the first solder pad and the first bond pad is in electrical contact with the second solder pad.

30. The method of Claim 29, further comprising removing material from the first corner and the second corner to provide respective first and second castellations at the first corner and the second corner;

forming a first electrical via on the first castellation, the first electrical via electrically connecting the second bond pad and the first solder pad; and

forming a second electrical via on the second castellation, the second electrical via electrically connecting the first bond pad and the second solder pad.

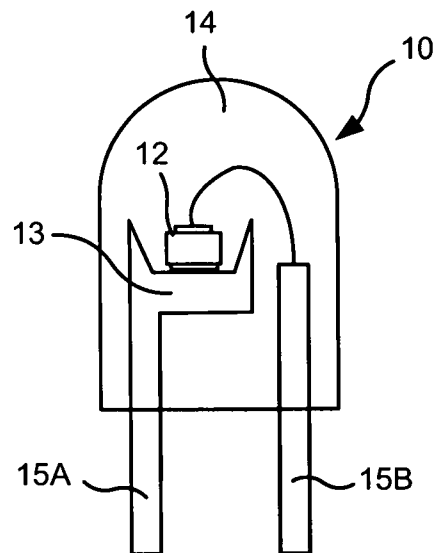
31. A method of forming a plurality of packaged light emitting diodes, comprising:

providing a sheet of ceramic material including a two-dimensional array of light emitting devices mounted thereon;

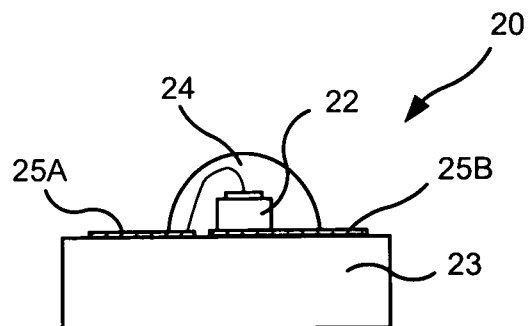
providing a mold including a plurality of cavities therein;  
dispensing a liquid encapsulant material in respective ones of the plurality of cavities;  
bringing the sheet of ceramic material into contact with the mold so that respective ones of the light emitting devices extend into a corresponding one of the plurality of cavities; and  
at least partially curing the liquid encapsulant so as to form encapsulant coatings around the respective light emitting devices.

32. The method of Claim 31, wherein the sheet of ceramic material includes a plurality of metallized holes therethrough, the method further comprising:

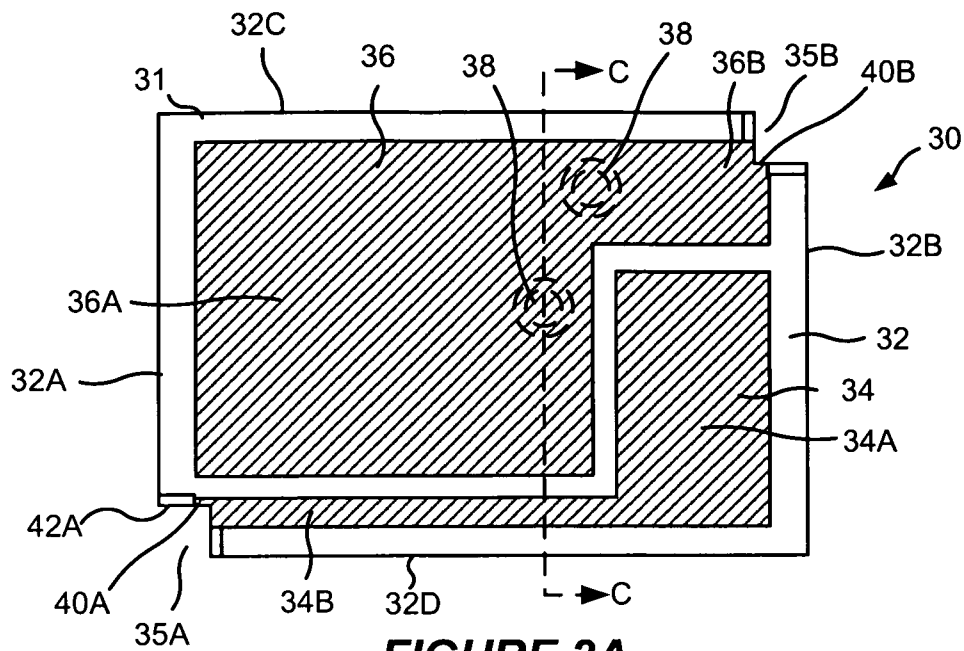
separating the sheet of ceramic material along separation lines that extend through a subset of the plurality of holes to thereby define individual light emitting diode substrates including castellations at corners thereof, the castellations including respective electrical vias thereon extending from first surfaces of the substrates to second surfaces of the substrates opposite the first surfaces.



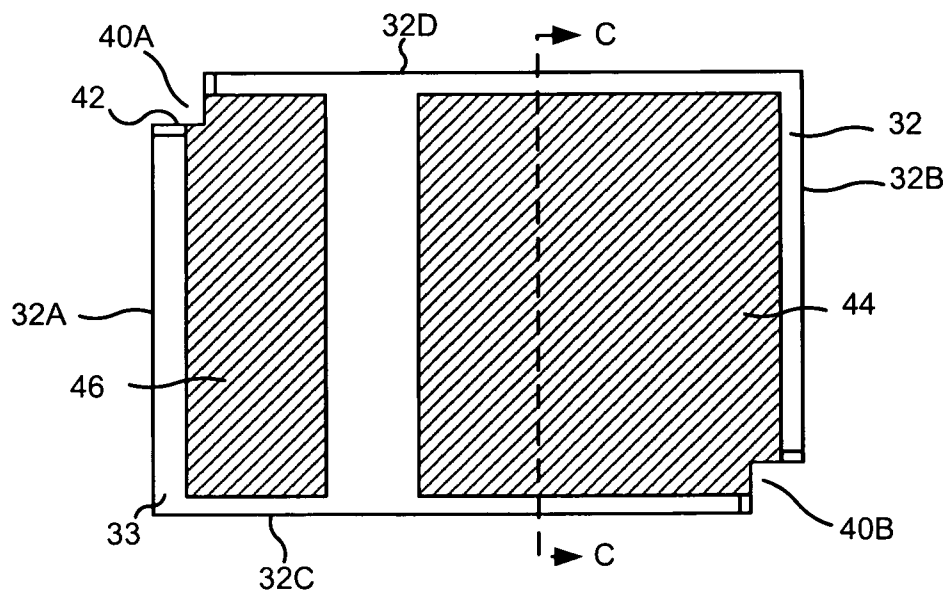
**FIGURE 1A**  
**(PRIOR ART)**



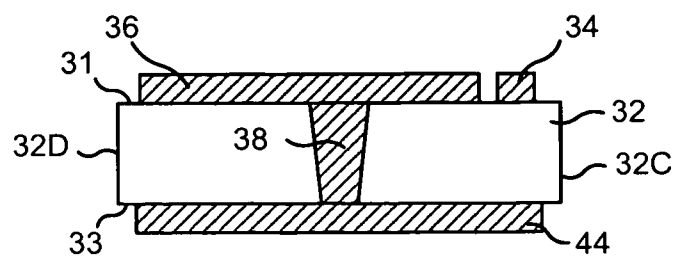
**FIGURE 1B**  
**(PRIOR ART)**



**FIGURE 2A**

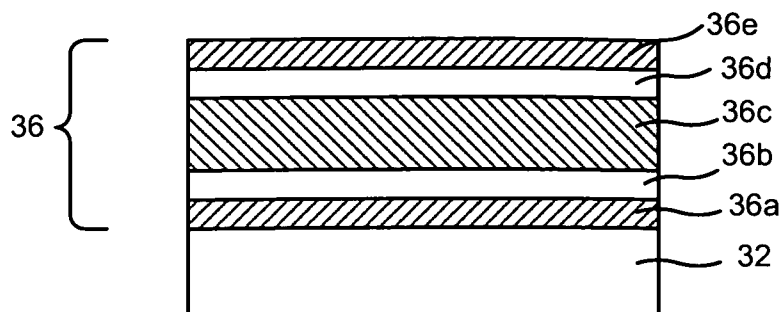


**FIGURE 2B**

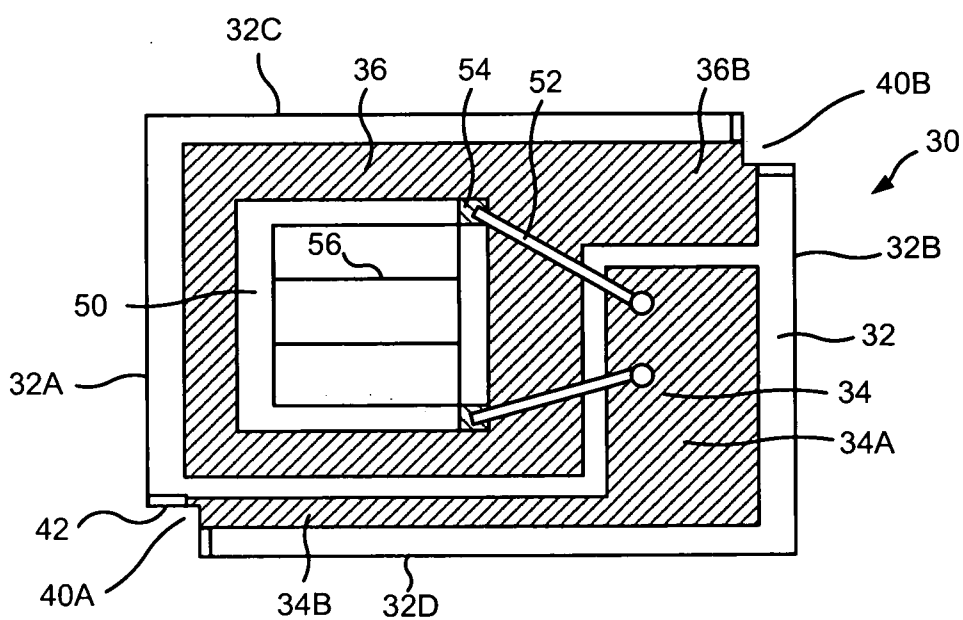


**FIGURE 2C**

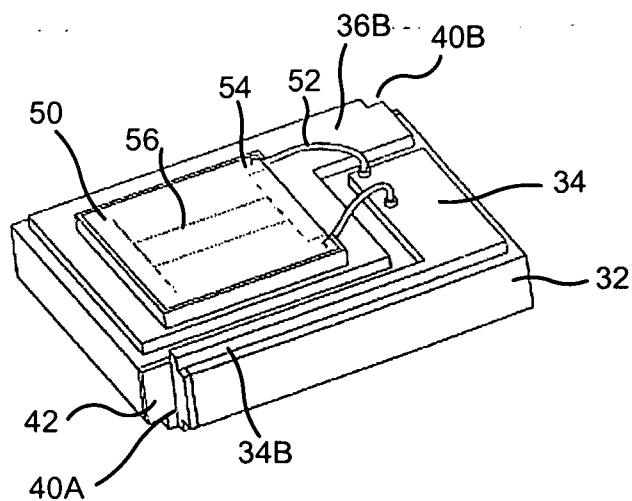




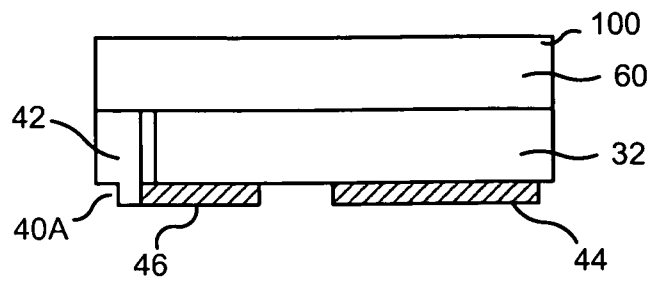
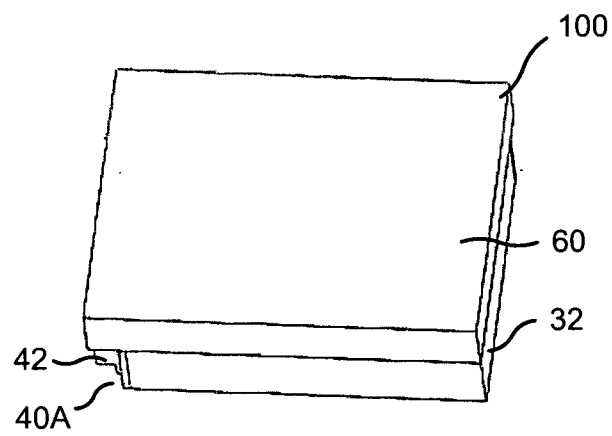
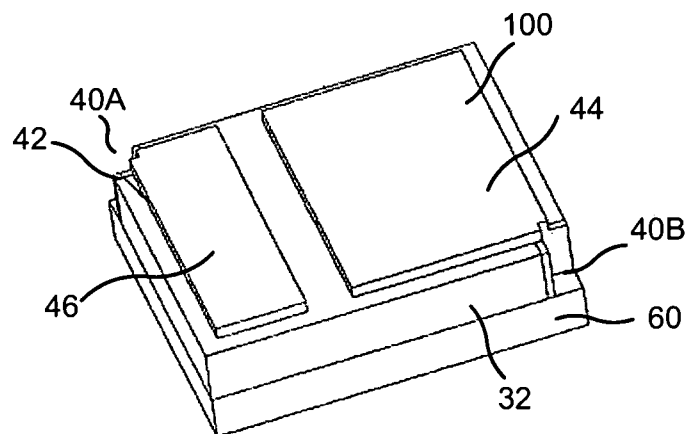
**FIGURE 2D**

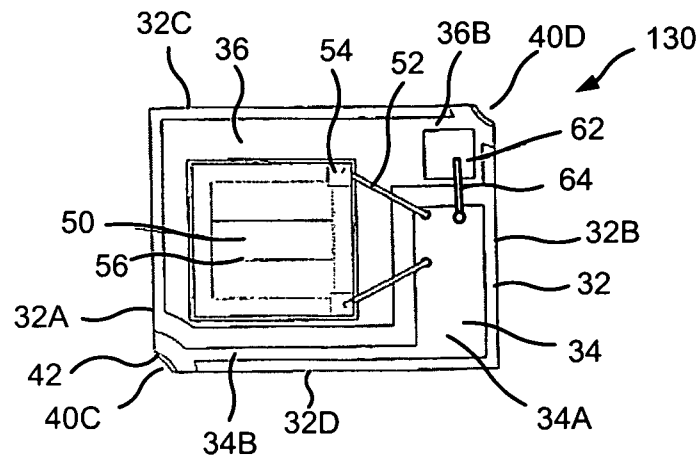
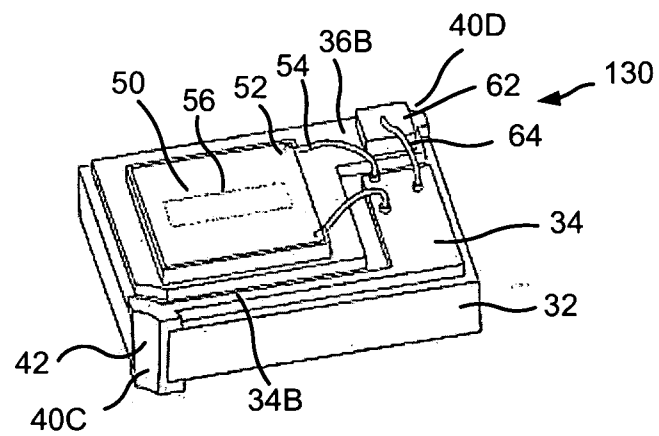


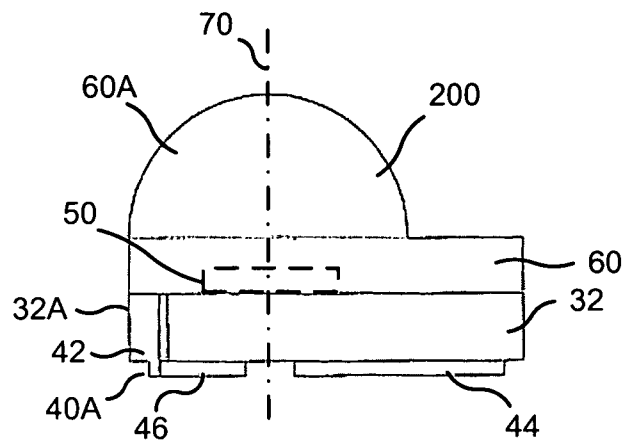
**FIGURE 3A**



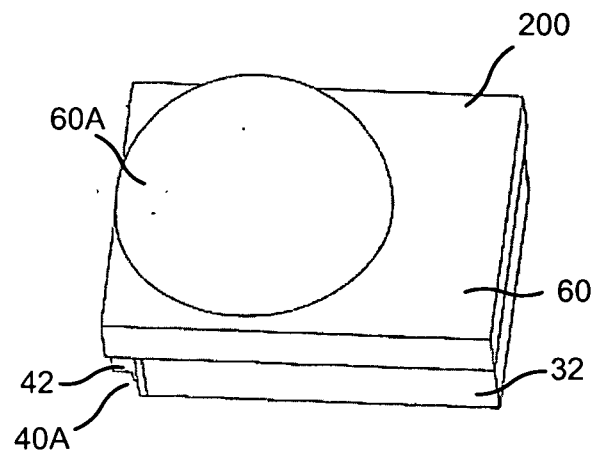
**FIGURE 3B**

**FIGURE 4A****FIGURE 4B****FIGURE 4C**

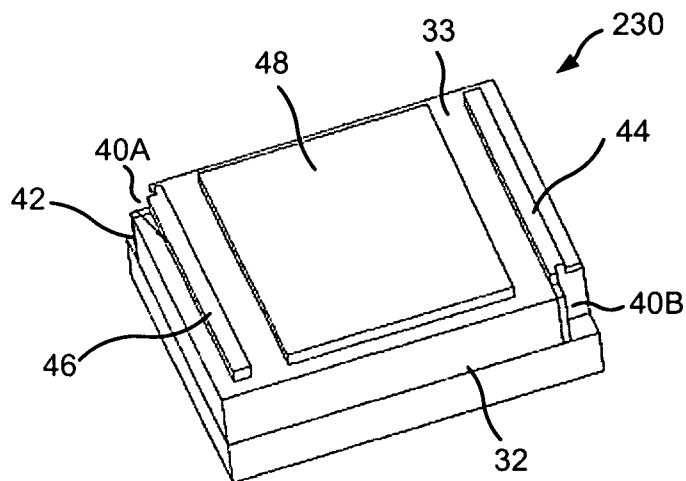
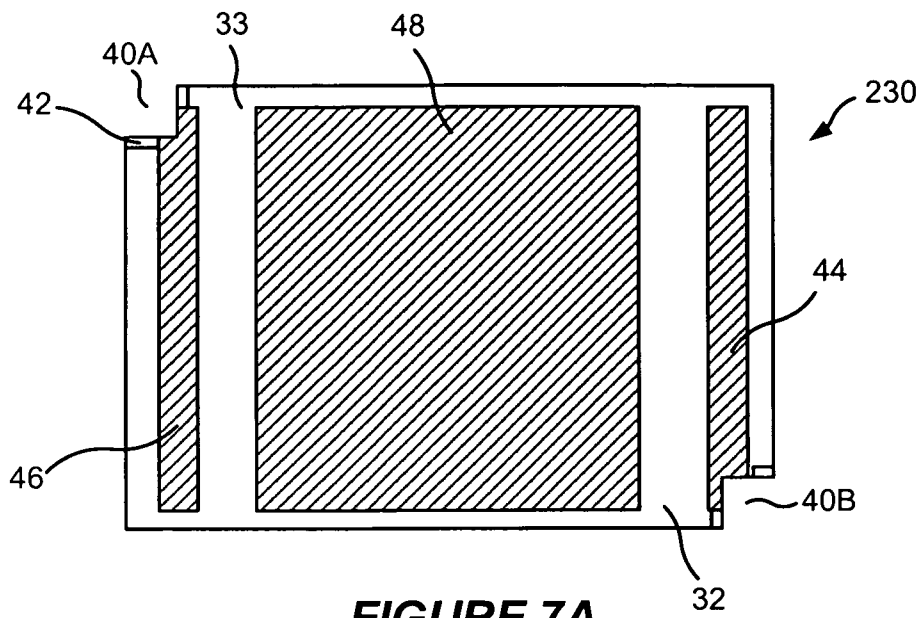
**FIGURE 5A****FIGURE 5B**

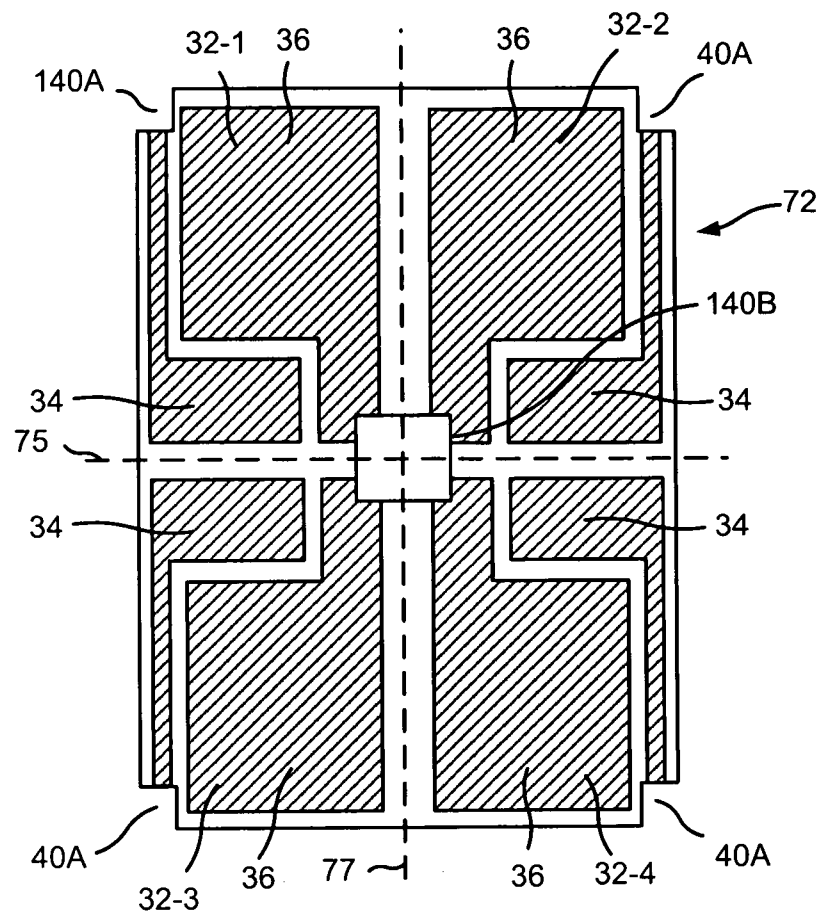
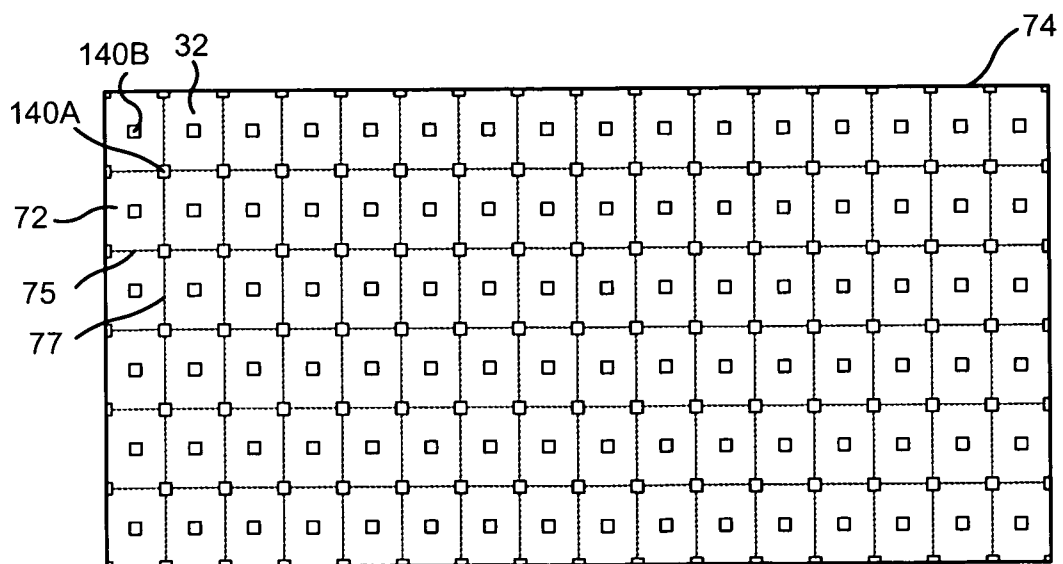


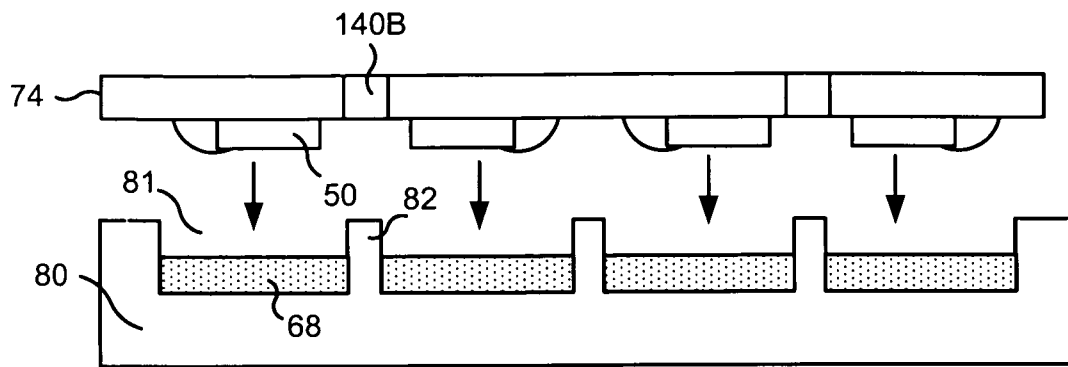
**FIGURE 6A**



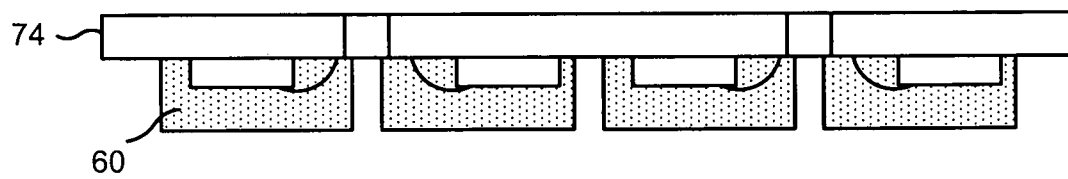
**FIGURE 6B**



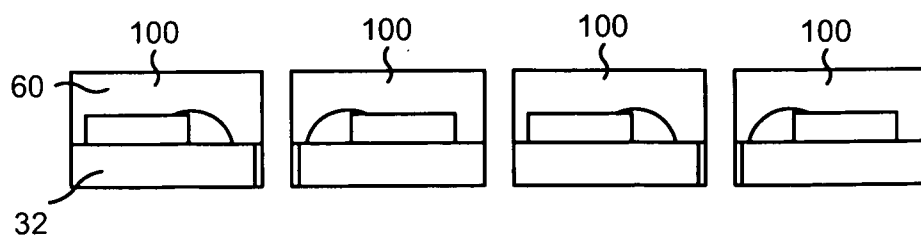
**FIGURE 8****FIGURE 9**



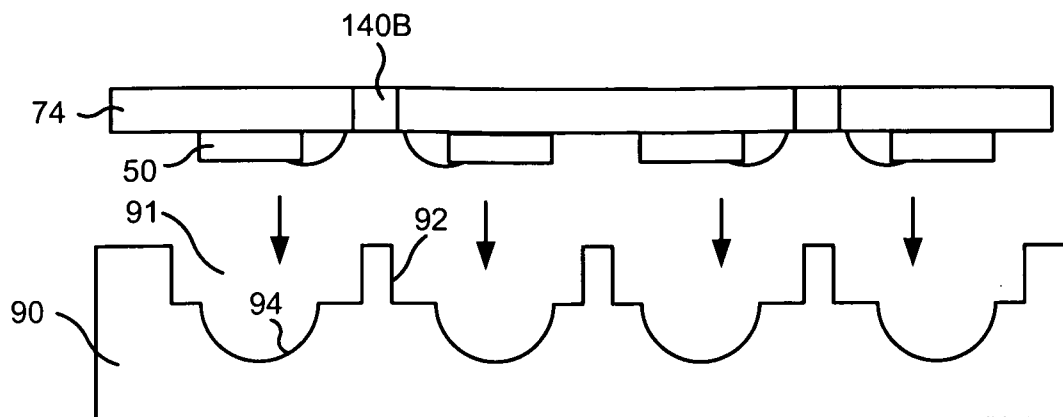
**FIGURE 10A**



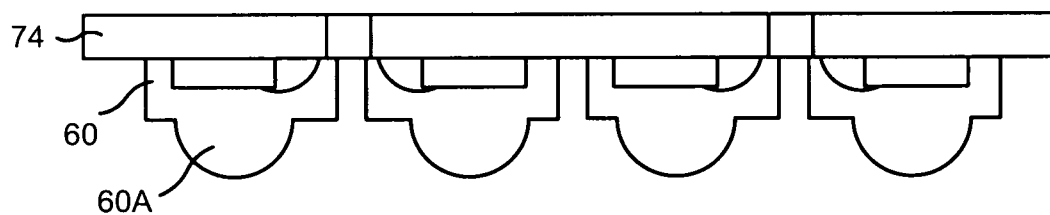
**FIGURE 10B**



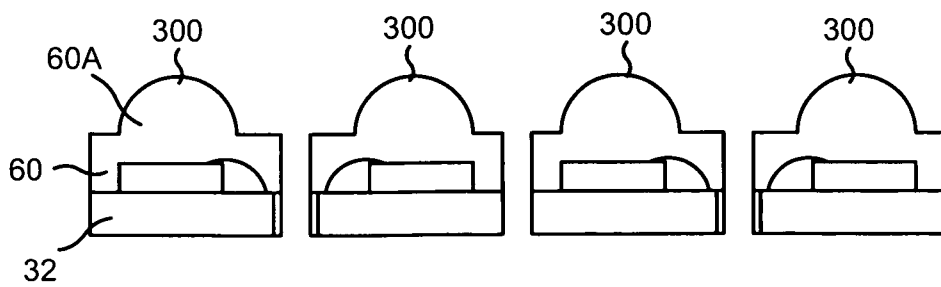
**FIGURE 10C**



**FIGURE 11A**

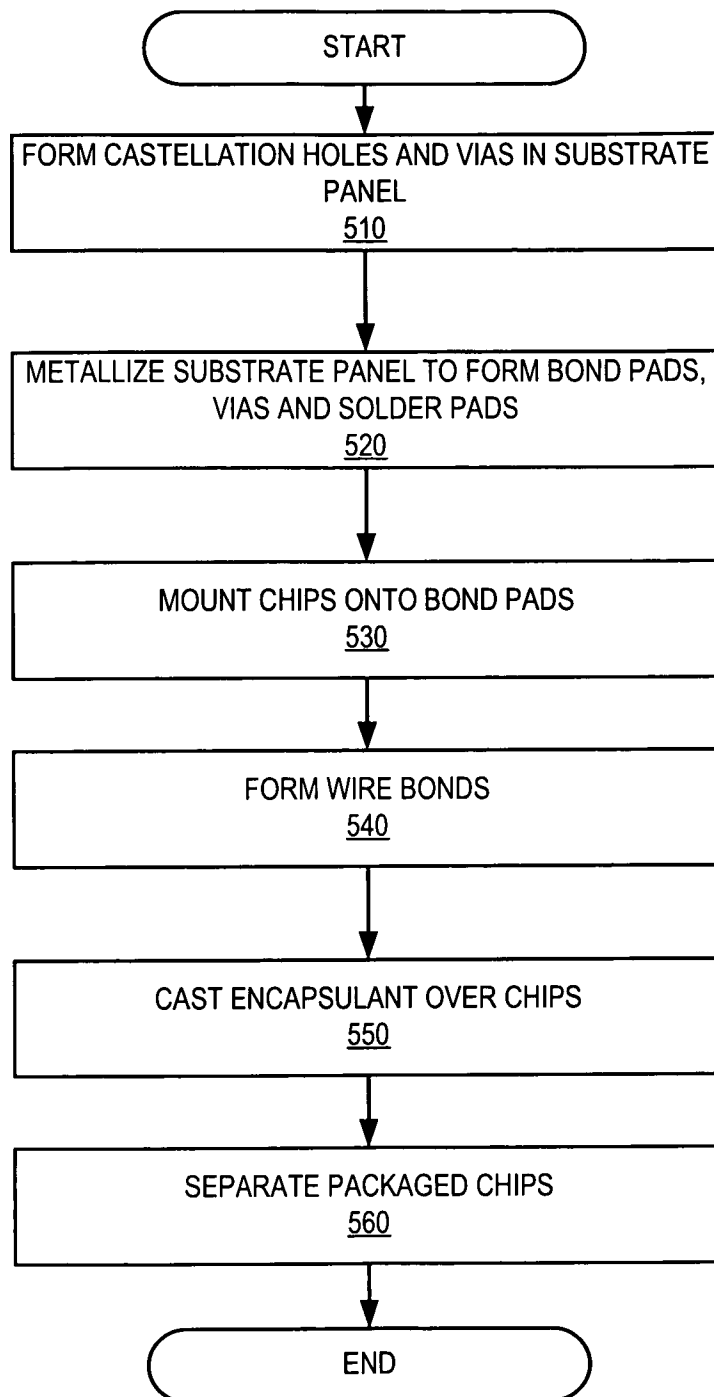


**FIGURE 11B**



**FIGURE 11C**



**FIGURE 12**