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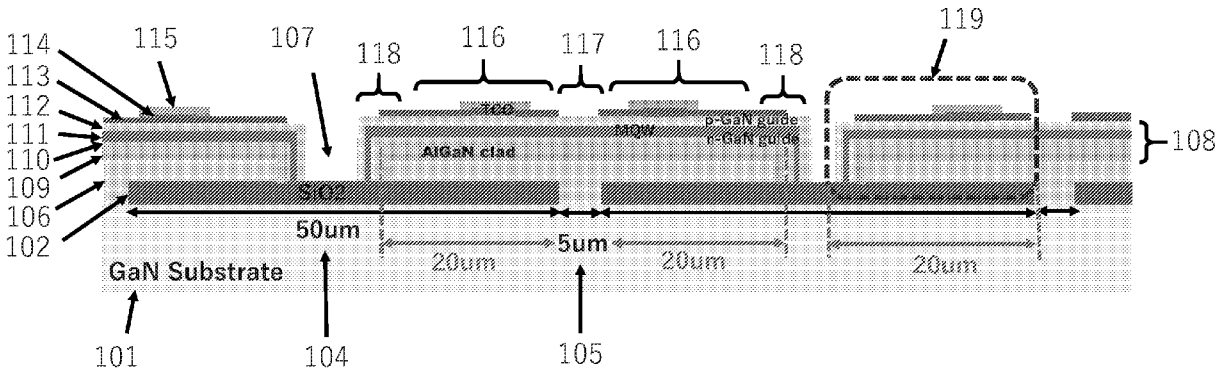



FIG. 1

(57) Abstract: A method of removing a substrate, comprising: forming a growth restrict mask with a plurality of striped opening areas directly or indirectly upon a GaN-based substrate; and growing a plurality of semiconductor layers upon the GaN-based substrate using the growth restrict mask, such that the growth extends in a direction parallel to the striped opening areas of the growth restrict mask, and growth is stopped before the semiconductor layers coalesce, thereby resulting in island-like semiconductor layers. A device is processed for each of the island-like semiconductor layers. Etching is performed until at least a part of the growth restrict mask is exposed. The devices are then bonded to a support substrate. The GaN-based substrate is removed from the devices by a wet etching technique that at least partially dissolves the growth restrict mask. The GaN substrate that is removed then can be recycled.

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# METHOD OF REMOVING A SUBSTRATE

## CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit under 35 U.S.C. Section 119(e) of the following co-pending and commonly-assigned application:

U.S. Provisional Patent Application No. 62/502,205, filed on May 5, 2017, by Takeshi Kamikawa, Srinivas Gandrothula, Hongjian Li and Daniel A. Cohen, entitled "METHOD OF REMOVING A SUBSTRATE," attorney's docket no. 30794.653-US-P1 (UC 2017-621-1);

which application is incorporated by reference herein.

## BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to a method for removing a substrate, including removing GaN-based substrates from GaN-based semiconductor layers.

2. Description of the Related Art.

The industrial value of a high-value semiconductor obtained uquality upon a low-priced substrate made of different materials is extremely high. Therefore, research and development have sought to realize this goal for a long time.

This is especially true in a gallium arsenide (GaAs)-based semiconductor thin film growth upon a silicon (Si) substrate and gallium nitride (GaN)-based semiconductor thin film growth upon a sapphire ($Al_2O_3$) substrate. In both instances, a relatively good quality semiconductor thin film can be obtained using an epitaxial lateral overgrowth (ELO) technique.

However, using a substrate made of different materials involves a number of problems. For example, due to different thermal expansion constants, the substrate may bow or become curved during epitaxial growth under high temperature.

Moreover, the substrate may be subjected to non-uniform temperatures, which may cause non-uniformity of the doping concentration, the thickness of the layers, the content of indium (In). This situation may cause a decrease in yield.

With regard to GaN-based semiconductors, many researchers have tried to avoid these issues using GaN substrates. However, GaN substrates, which are typically produced using HVPE (hydride vapor phase epitaxy), are very expensive.

For example, 2-inch c-plane polar GaN substrates cost about $1000/wafer, while 2-inch semipolar GaN substrates cost about $10000/wafer. Thus, there is a desire to recycle GaN substrates.

It is easy to remove a GaN device from a substrate of different materials, such as a sapphire substrate. For example, there are many defects at the GaN/sapphire interface, which means that bonding strength at the interface is weak. See, e.g., US Patent Publication No. 2012/0280363 A1.

However, a mechanical removal method, such as ultra-sonic removal, may damage the semiconductor layers. This is a problem especially for edge emitting laser diodes (EELDs), which need smooth facets. With a mechanical removal method, cracks may occur. For example, when cleaving the device, damage may cause cracks in unintended directions. It is necessary to reduce any such damage.

Furthermore, the GaN/sapphire interface absorbs laser light due to the many defects at the interface. Consequently, a laser ablation method may be used to remove the substrate from the semiconductor layers.

On the other hand, the use of a GaN substrate, in order to obtain high quality GaN-based semiconductor layers and avoid bowing or curvature of the substrate during

epitaxial growth, makes it hard to remove the substrate, because there is no heterointerface, such as with GaN/sapphire.

One conventional technique is the use of photoelectrochemical (PEC) etching of sacrificial layers to remove device structures from GaN substrates, but this takes a long time and involves several complicated processes. Moreover, the yield from these processes have not reached industry expectations.

Thus, there is a need in the art for improved methods of removing substrates, especially where GaN thin films are grown on GaN substrates. The present invention satisfies this need.

## SUMMARY OF THE INVENTION

To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding this specification, the present invention discloses a method for removing a substrate, and specifically, a method of removing GaN-based substrates from GaN-based semiconductor layers in an easy manner, so that the GaN-based substrates can be recycled.

## BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIGS. 1 and 2 are schematics of device structures fabricated according to the present invention.

FIGS. 3(a) and 3(b) illustrate the growth restrict mask and the opening areas of the growth restrict mask.

FIGS. 4(a) and 4(b) illustrate the growth restrict mask, the opening areas of the growth restrict mask, the flat surface region and the layer bending region.

FIGS. 5(a) and 5(b) illustrate the etching at the layer bending region.

FIGS. 6(a), 6(b) and 6(c) illustrate the etching at the layer bending region, as well as the overwrap regions.

FIG. 7 is a schematic of a device structure including a bended active region.

FIG. 8 is a schematic of a device structure formed by the island-like semiconductor layers.

FIG. 9 is a schematic of a device structure where there has been dry etching below a surface of the GaN-based substrate.

FIG. 10 is a schematic of bonding a support substrate.

FIG. 11 is a schematic of dissolving a growth restrict mask by wet etching.

FIG. 12 is a schematic of n-electrode deposition.

FIGS. 13(a) and 13 (b) illustrate a method of making facets for a laser diode device, as well as chip scribing techniques.

FIGS. 14(a) and 14(b) also illustrate a method of making facets for a laser diode device, as well as chip scribing techniques.

FIG. 15 is a flowchart illustrating the steps and functions of the present invention, according to one embodiment.

## DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

### Overview

Generally, the present invention describes a method for manufacturing a GaN-based semiconductor device, so that a GaN-based substrate can be removed from the

GaN-based semiconductor device, and the GaN-based substrate recycled. This is accomplished using at least the following steps:

1. Epitaxial lateral overgrowth (ELO), growth of device layers, p-electrode deposition and ridge stripe processing.

This step is described in FIG. 1, which illustrates a GaN-based substrate 101 with an $SiO_2$-based growth restrict mask 102 formed thereon. Alternatively, as shown in FIG. 2, a GaN-based intermediate layer 103 may be deposited first on the GaN-based substrate 101 with the $SiO_2$-based growth restrict mask 102 formed on the GaN-based intermediate layer 103.

The growth restrict mask 102 is patterned into stripes 104, and includes opening areas 105 between the stripes 104 for epitaxial lateral overgrowth of GaN-based layers 106. Each of the stripes 104 of the growth restrict mask 102 has a width of about 50 μm with each of the opening areas 105 having a width of about 5 μm separating adjacent ones of the stripes 104.

The growth of the ELO GaN-based layers 106 occurs first in the opening areas 105, on either the GaN-based substrate 101 as shown in FIG. 1 or the GaN-based intermediate layer 103 as shown in FIG. 2, and then laterally from the opening areas 105 over the stripes 104 of the growth restrict mask 102. The growth of the ELO GaN-based layers 106 is stopped or interrupted before the ELO GaN-based layers 106 at adjacent opening areas 105 can coalesce on top of the growth restrict mask 102. Preferably, the ELO GaN-based layers 106 have a lateral width of about 20 μm in a wing region of the stripe 104 of the growth restrict mask 102. This interrupted growth results in no-growth regions 107 between adjacent ELO GaN-based layers 106.

Thereafter, semiconductor device layers 108 are grown on or above the ELO GaN-based layers 106. In one embodiment, the semiconductor device layers 108 may include an AlGaN cladding layer 109, n-GaN guiding layer 110, InGaN/GaN multiple quantum well (MQW) active region 111, and p-GaN guiding layer 112. A Transparent

Conductive Oxide (TCO) cladding layer 113 is deposited on the p-GaN guiding layer 112, followed by the deposition of a current limiting layer 114. Finally, a p-pad 115 is deposited on the TCO cladding layer 113.

The combined thickness of the ELO GaN-based layers 106 and the semiconductor device layers 108 may range from 1 to 20 μm, for example, but is not limited to these values. The combined thickness of the ELO GaN-based layers 106 and semiconductor device layers 108 is measured from the surface of growth restrict mask 102 to the upper surface of the semiconductor device layers 108.

The semiconductor device layers 108 include one or more flat surface regions 116 separated by etching regions 117, which are bounded on both sides by layer bending regions 118 at the edges thereof adjacent the no-growth regions 107. The width of the flat surface region 116 is preferably at least 5 μm, and more preferably is 10 μm or more. There is a high uniformity to the thickness of each of the semiconductor device layers 108 in the flat surface region 116.

The semiconductor device layers 108 separated by etching regions 117 and/or no-growth regions 107 are referred to as island-like semiconductor layers 119. Each of the island-like semiconductor layers 119 may be processed into a separate device. For example, ridge stripe processing may be carried out on each of the island-like semiconductor layers 119 to form separate laser devices.

These elements are further shown and described in more detail in conjunction with FIGS. 3(a)-3(b), 4(a)-4(b), 5(a)-5(b), 6(a)-6(c), 7 and 8 below.

2. Dry etching below the surface of the GaN-based substrate.

This step is described in FIG. 9. Dry etching is performed on the etching region 117, through the device layers 108 and the ELO GaN-based layers 106, to expose the growth restrict mask 102. This etching results in the creation of the island-like semiconductor layers 119, including the flat region 116 and the layer bending region 118,

and initiates the step to separate the island-like semiconductor layers 119 from the GaN-based substrate 101.

It is not always necessary to etch the surface of the GaN-based substrate 101, as long as the growth restrict mask 102 is exposed. More preferably, etching is performed up to the surface of the GaN-based substrate 101, so that the GaN-based substrate 101 can be easily removed.

3. Bonding a support substrate.

This step is shown in FIG. 10. The island-like semiconductor layers 119 are flip-chip bonded to a support substrate 1001 with metal or solder bonding pads 1002 deposited thereon, using metal-metal bonding or soldering techniques.

4. Dissolving the growth restrict mask by wet etching.

This step is shown in FIG. 11. The $SiO_2$ of the growth restrict mask 102 (shown in FIG. 10) is removed using a chemical solution, such as hydrofluoric (HF) or buffered hydrofluoric (BHF) acid, which lifts off the GaN-based substrate 101 from the island-like semiconductor layers 119.

5. N-electrode deposition.

This step is shown in FIG. 12. N-electrodes 1201 are deposited on the back side of the island-like semiconductor layers 119 following lift-off of the GaN-based substrate 101.

6. Chip scribing.

This step is shown in FIGS. 13(a)-13(b) and 14(a)-14(b). Chip scribing is performed using solid or dashed lines.

These and other aspects of the present invention are described in more detail below.

Definitions of Terms

*GaN-based substrate*

Any GaN-based substrate 101 that is sliced on a {0001}, {1-100}, {11-20}, {20-21}, {20-2-1}, {11-22} plane, or other plane, from a bulk GaN crystal can be used. The GaN-based substrate 101 may include Al, In, B, etc.

*GaN-based semiconductor layers*

The GaN-based semiconductor layers include the ELO GaN-based layers 106, device layers 108 such as AlGaN cladding layer 109, n-GaN guiding layer 110, InGaN/GaN multiple quantum well (MQW) active region 111 and p-GaN guiding layer 112, as well as intermediate layers 103.

These GaN-based semiconductor layers can include In, Al and/or B, as well as other dopants and impurities, such as Mg, Si, Zn, O, C, H, etc. The GaN-based semiconductor layers specifically may comprise GaN layers, AlGaN layers, AlGaInN layers, InGaN layers, etc.

As noted above, the device layers 108 such as AlGaN cladding layer 109, n-GaN guiding layer 110, InGaN/GaN multiple quantum well (MQW) active region 111 and p-GaN guiding layer 112, typically include at least one layer among an n-type layer, an undoped layer and a p-type layer.

Using the GaN-based semiconductor layers, the resulting device may comprise, for example, a light-emitting diode (LED), laser diode (LD), Schottky barrier diode (SBD), photodiode, metal-oxide-semiconductor field-effect-transistor (MOSFET), etc., but is not limited to these devices. This invention is particularly useful for micro-LEDs and laser diodes, such as edge-emitting lasers and vertical cavity surface-emitting lasers (VCSELs).

*Growth restrict mask*

The growth restrict mask 102 comprises a dielectric layer, such as $SiO_2$, SiN, SiON, $Al_2O_3$, AlN, AlON, or a refractory metal, such as W, Mo, Ta, Nb, etc. The growth restrict mask 102 may be a laminate or stacking layer structure selected from the above materials.

In one embodiment, the thickness of the growth restrict mask 102 is about 0.05 - 3 μm. The width of each of the stripes 104 of the growth restrict mask 102 is preferably larger than 20 μm, more preferably larger than 40 μm, and most preferably about 50 μm.

As noted above, the growth restrict mask 102 is patterned into stripes 104 and includes opening areas 105 between the stripes 104. In one embodiment shown in FIG. 3(a), the opening areas 105 are striped having a length a and a width b. The length a of each of the opening areas 105 is in a first direction parallel to the 1-100 direction of the (0001) c-plane-oriented GaN-based substrate 101 and the width b of each of the opening areas 105 is in a second direction parallel to the 11-20 direction of the (0001) c-plane-oriented GaN-based substrate 101, periodically at a first interval p1, extending in the second direction. The width b of each of the opening areas 105 is typically constant, but may be changed as necessary. The width L of each of the stripes 104 of the growth restrict mask 102 is L = p1 - b.

In another embodiment shown in FIG. 3(b), the length and width of each of the opening areas 105 are arranged in similar directions as FIG. 3(a), but the lengths a may be different and adjacent opening areas 105 are offset in the first direction by a second interval p2 and are shifted in the second direction by a half of the first interval p1, in a manner such that end portions of adjacent opening areas 105 overlap lengthwise for a predetermined distance q in the first direction. This arrangement prevents embossment of both end portions of the opening areas 105 in the 1-100 direction of the GaN-based substrate 101.

In both of these embodiments, the interval p1 may be about 5 to 120 μm; the interval p2 may be about 500 to 1050 μm; the length a may be about 200 to 2000 μm; the width b may be about 2 to 20 μm; and the distance q may be about 35 to 40 μm. In FIG. 3(a), for example, the interval p1 may be about 55 μm; the interval p2 may be about 810 μm; the length a may be about 1200 μm; the width b may be about 5 μm; and the width L is 50 μm.

*ELO GaN-based layers*

FIGS. 4(a) and 4(b) illustrate the ELO GaN-based layers 106 grown using the growth restrict masks 102 of FIGS. 3(a) and 3(b), respectively.

Using the growth restrict mask 102, the ELO GaN-based layers 106 are grown in an island-like shape in the (0001) plane orientation by a vapor-phase deposition method, for example, a metalorganic chemical vapor deposition (MOCVD) method.

The surface of the GaN-based substrate 101 or the GaN-based intermediate layer 103 is exposed in the opening areas 105 of the growth restrict mask 102, and the ELO GaN-based layers 106 are selectively grown thereon, continuously in both vertical and lateral directions relative to the growth restrict mask 102. The growth is stopped before the ELO GaN-based layers 106 coalesce with adjacent ELO GaN-based layers 106 on the growth restrict mask 102.

For (0001) plane growth of a GaN-based semiconductor, the lateral growth rate parallel to the plane is the largest in the 11-20 direction and is the smallest in the 1-100 direction. In the growth restrict mask 102 shown in FIGS. 3(a) and 3(b), as the longitudinal direction of the opening area 105 is the 1-100 direction, the growth rate of the GaN-based semiconductor is small at both ends of the opening area 105, the ELO GaN-based layers 106 opposing each other in the 1-100 direction do not coalesce and remain separated from each other. The length of the ELO GaN-based layers 106 in the 1-100 direction becomes nearly equal with the length a of the opening area 105.

The thickness of the ELO GaN-based layers 106 is important, because it determines the width of the flat surface region 116. Preferably, the width of the flat surface region 116 is 20 μm or more. The thickness of the ELO GaN-based layers 106 is preferably as thin as possible, to reduce processing time and to facilitate etching the opening areas 105.

The growth ratio of the ELO GaN-based layers 106 is the ratio of the growth rate of the lateral direction parallel to the 11-20 axis of the GaN-based substrate 101 to the growth rate of the vertical direction parallel to the 0001 axis of the GaN-based substrate 101. Preferably, the growth ratio of the ELO GaN-based layers 106 is high, wherein, by optimizing the growth conditions, the growth ratio of the ELO GaN-based layers 106 can be controlled from 1 to 4.

In the case where the ratio of the ELO GaN-based layers 106 is 4, the ELO GaN-based layers 106 are only about 5 μm in thickness, but obtain a width of the flat surface region 116 of 20 μm. In this case, it is very easy to etch the opening areas 105.

In order to obtain a high ratio for the ELO GaN-based layers 106, the growth temperature of the ELO GaN-based layers 106 is preferably higher than about 950 °C and the pressure in the MOCVD chamber is preferably lower than about 100 Torr. Also, in order to promote the migration of Ga atoms, the V/III ratio is preferably high.

When the distance between the ELO GaN-based layers 106 on opposing planes with lowest growth rates is large, the following disadvantages occur. In the mask portion of the growth restrict mask 102 at the regions between the ELO GaN-based layers 106 in the 1-100 direction of which the growth rate is the lowest, raw gas is not consumed, and therefore, the gas concentration increases, and a concentration gradient in the 1-100 direction is generated, and by diffusion according to the concentration gradient, a large amount of the gas is supplied at the edge portions in the 1-100 direction of the ELO GaN-based layers 106. As the result, the thickness of the edge portions in the 1-100 direction of the ELO GaN-based layers 106 increases in comparison with other portions, and

results in a raised shape. The raised shape causes not only structural inconveniences in the devices, but also creates problems in the following manufacturing processes of photolithography, etc.

To prevent the raised shape, the ELO GaN-based layers 106 come as close as possible, and thus it is necessary not to create in-plane uniformity of the raw gas from the beginning of the growth. In the growth restrict mask 102 shown in FIG. 3(b), the opening areas 105 adjacent to each other in the 11-20 direction are formed in a manner such that the opening areas 105 overlap at opposing end portions for the length q.

As a result, the in-plane uniformity of gas concentration is obtained by consumption of the raw gas caused by growing the ELO GaN-based layers 106. Finally, this results in a uniformity in the thickness of the island-like semiconductor layers 119.

*Etching of opening areas*

FIGS. 5 and 6 illustrate the details of the etching process of the opening areas 105.

FIG. 5(a) shows the no-growth regions 107, the ELO GaN-based layers 106, the flat surface regions 116, the layer bending regions 118, and the etching regions 117, based on the growth restrict mask 102 of FIG. 3(a), and FIG. 5(b) shows the ELO GaN-based layers 106 and the etching regions 117, where etching 501 has been performed to remove the layer bending regions 118 (not shown).

FIG. 6(a) shows the opening areas 105, the no-growth regions 107, the ELO GaN-based layers 106, the flat surface regions 116, and the layer bending regions 118, based on the growth restrict mask 102 of FIG. 3(b), and FIG. 6(b) shows the opening areas 105 and the ELO GaN-based layers 106, where etching 501 has been performed to remove the layer bending regions 118 (not shown).

As shown by 601 and 602 in FIG. 6(a), the etching 501 may be larger than the opening areas 105. In this example, the island-like semiconductor layers 119 do not have

an interface with the GaN-based substrate 101 and other island-like semiconductor layers 119. With the wider etching area, the island-like semiconductor layers 119 can be removed quickly and easily from the GaN-based substrate 101.

If the interface between the island-like semiconductor layers 119 and the GaN-based substrate 101 remains at least in part, it does provide some benefits. For example, FIG. 6(c) shows the case where the interface between the island-like semiconductor layers 119 and the GaN-based substrate 101 remains at both edges of the opening areas 105. In this case, it is easy to hold the island-like semiconductor layers 119 after the dry etching. However, it is best if the remaining area is as small as possible. After dry etching, the island-like semiconductor layers 119, which are on the growth restrict mask 102, can slide and be easily removed.

*Etching region*

FIGS. 5 and 6 also illustrate the details of the etching regions 117.

The etching regions 117 are the location that is etched by a dry etch and/or wet etch to expose the growth restrict mask 102. As shown in FIGS. 5(a) and 5(b), the etching regions 117 are mainly on the opening areas 105. However, in FIGS. 6(a) and 6(c), there is an etching region 601 that overwraps a first direction and/or an etching region 602 that overwraps a second direction to the growth restrict mask 102 (not shown). This is to expose the growth restrict mask 102.

The overwrap width typically ranges between about 0 and 10 μm, and more preferably ranges between about 1 and 6 μm in the first direction, because the process yield is kept high. The second direction is almost the same value. However, the overwrap width may be different without causing any problems.

The etching regions 117 may be wider than the opening areas 105, so that that there is nothing else present at the interface between the island-like semiconductor layers

119 and the GaN-based substrate 101. This makes the GaN-based substrate 101 easy to remove from the island-like semiconductor layers 119.

*Layer bending region*

FIG. 7 illustrates the details of the layer bending region 118, in conjunction with the growth restrict mask 102, the opening area 105, the flat surface region 116, and the etching region 117.

In one embodiment, the layer bending layer 118 may or may not be removed by etching. For example, simultaneous etching of both the etching region 117 and the layer bending region 118 may be performed in order to reduce the processing time and cost.

As shown in FIG. 7, the layer bending region 118 may include a bended active region 701. If the layer bending layer 118 is not removed by etching, and the bended active region 701 remains in the device, a portion of the light emitted from the active region 111 is reabsorbed. As a result, it may be preferable to remove the layer bending region 118.

Moreover, if the device is a laser diode, and the layer bending layer 118 is not removed by etching, so that the bended active region 701 remains in the device, the laser mode may be affected by the layer bending region 118 and the bended active region 701 due to a low refractive index (e.g., an InGaN layer) in the bended active region 701. As a result, it may be preferable to remove the layer bending region 118 and the bended active region 701.

*Island-like semiconductor layers*

FIG. 8 is a sectional view of the island-like semiconductor layers 119, which in this example comprise a laser diode.

Specifically, the III-nitride semiconductor laser diode is comprised of the following layers, laid one on top of another in the order mentioned, a 1.3 μm n-$Al_{0.06}GaN$

cladding layer 109, a 0.4 μm n-GaN guiding layer 110, an InGaN/GaN MQW active region 111, a p-GaN guiding layer 112, an TCO cladding layer 113, a current limiting layer 114, and a p-electrode 115. Note that, in this example, there is an optional AlGaN electron blocking layer (EBL) 801 positioned between the InGaN/GaN MQW active region 111 and the p-GaN guiding layer 112.

The sectional view of FIG. 8 shows the laser bar along a direction perpendicular to an optical resonator, which is comprised of a ridge stripe structure. The ridge stripe structure is comprised of the TCO cladding layer 113, current limiting layer 114, and p-electrode 115, and provides optical confinement in a horizontal direction. The width of the ridge stripe structure is of the order of 1.0 to 20 μm, and typically is 5 μm.

In one embodiment, the p-electrode 115 may be comprised of one or more of the following materials: Pd, Ni, Ti, Pt, Mo, W, Ag, Au, etc. For example, the p-electrode may comprise Pd-Ag-Ni-Au (with thicknesses of 3-50-30-300 nm). These materials may be deposited by electron beam evaporation, sputter, thermal heat evaporation, etc. In addition, the p-electrode is typically deposited on the TCO cladding layer 113.

*Etching region*

FIG. 9 shows the depth of etching region 117, which is at least below the surface of growth restrict mask 102 and, in this example, extends into the GaN-based substrate 101. In this case, it is easily to remove the growth restrict mask 102 using a wet etching method.

*Support substrate*

FIG. 10 illustrates a support substrate 1001, which is bonded to the island-like semiconductor layers 119 individually using patterned bonding pads 1002. Conventional bonding techniques can be used.

The support substrate 1001 may be comprised of elemental semiconductor, compound semiconductor, metal, alloy, nitride-based ceramics, oxide-based ceramics, diamond, carbon, plastic, etc., and may comprise a single layer structure, or a multilayer structure made of these materials. A metal, such as solder, etc., or an organic adhesive, may be used for the patterned bonding pads 1002, and is selected as required.

In general, the most common types of flip-chip bonding are thermal compression bonding and wafer fusion/bonding. Wafer fusion has been popularly employed in InP-based devices. However, thermal compression bonding is generally much simpler than wafer fusion, as it uses metal-to-metal bonding, and has the benefit of also greatly improving thermal conductivity.

An Au-Au compression bond is by far the simplest bond and results in a fairly strong bond. An Au-Sn eutectic bond offers a much greater bond strength.

In one embodiment, a Cu substrate 1001 is used as the support substrate. The patterned Ti/Au bonding pads 1002 are fabricated on the Cu substrate 1001 by electron beam evaporation or sputter. The bonding pads 1002 are comprised of, in one example, Ti (10 nm) and Au (500 nm).

An activation of the exposed surface of the island-like semiconductor layers 119 may be performed before compression bonding. The activation is achieved using a plasma process of Ar and/or $O_2$.

Thereafter, the island-like semiconductor layers 119 are bonded to the bonding pads 1002 of the support substrate 1001 at about 150-300°C under pressure.

*Removing the substrate*

There are two techniques that can be used to remove the GaN-based substrate 101 from the island-like semiconductor layers 119.

One technique is to use just the support substrate 1001. The interface between the growth restrict mask 102 and the ELO GaN-based layers 106 has a weak bonding

strength. Thus, it is easy to peel the island-like semiconductor layers 119 from the GaN-based substrate 101 using the support substrate 1001.

Another technique is to etch the growth restrict mask 102 using a hydrofluoric acid (HF), buffered HF (BHF), or other etchant, before removing the GaN-based substrate 101, to at least partially dissolve the growth restrict mask 102. This technique requires that the opening areas 105 and/or the etching regions 117 be etched until the growth restrict mask 102 is exposed. Once the growth restrict mask 102 is exposed, wet etching can partially or wholly dissolve the growth restrict mask 102, and then the GaN-based substrate 101 can be removed from the island-like semiconductor layers 119. This is illustrated in FIG. 11.

Specifically, after the support substrate 1001 has been bonded to the island-like semiconductor layers 119, the entire structure is dipped into a solvent for wet etching to dissolve the growth restrict mask 102. In one embodiment, the growth restrict mask 102, shown in FIG. 10, is $SiO_2$, which is dissolved by an HF or BHF solvent. The merit of this technique is that a wide area of $SiO_2$ is dissolved by the HF very easily and quickly, and there is no mechanical damage when the GaN-based substrate 101 is removed (very gently) from the island-like semiconductor layers 119.

The removed GaN-based substrate 101 shown in FIG. 11 then can be recycled. For example, the surface of the GaN-based substrate 101 may be re-polished by a polisher. The recycling process can be done repeatedly, which lowers the cost of fabricating GaN-based semiconductor devices.

*First and second support substrates*

In another example, first and second support substrates may be used in the removal of the GaN-based substrate 101 from the island-like semiconductor layers 119. This method comprises the steps of bonding a first support substrate 1001 to the exposed surface of the island-like semiconductor layers 119, and bonding a second support

substrate (not shown) to an exposed surface of the GaN-based substrate 101, before or after removing the GaN-based substrate 101 from the island-like semiconductor layers 119. Typically, the second support substrate bonded to the GaN-based substrate 101 later can be removed by dissolving low-temperature melted metal and/or solder bonding layers between the second support substrate bonded and the GaN-based substrate 101 using an appropriate etchant.

*N-electrodes*

FIG. 12 illustrates the deposition of n-electrodes 1201 on the back side of the island-like semiconductor layers 119, which is exposed following the removal of the GaN-based substrate 101.

Typically, the n-electrodes 1201 may be comprised of the following materials: Ti, Hf, Cr, Al, Mo, W, Au, etc. For example, the n-electrode 1201 may be comprised of Ti-Al-Pt-Au (with a thickness of 30-100-30-500 nm), but is not limited to those materials. The deposition of these materials may be performed by electron beam evaporation, sputter, thermal heat evaporation, etc.

*Facets*

FIGS. 13(a)-13(b) and 14(a)-14(b) illustrate the method of making facets for a laser diode device.

FIG. 13(a) shows the no-growth region 107, the ELO GaN-based layer 106, and the etching region 117, based on the growth restrict mask 102 of FIG. 3(a). FIG. 13(b) is an enlarged view of the circled portion of FIG. 13(a), and shows a ridge stripe structure 1301, etched mirror region 1302 and chip scribe line 1303, on the ELO GaN-based layer 106 in FIG. 13(a). The etched mirror region 1302 is located based on optical resonance length, as is the chip scribe line 1303.

FIG. 14(a) shows the island-like semiconductor layers 119 bonded to the support substrate 1001. FIG. 14(b) is an enlarged view of the circled portion of FIG. 14(a), and shows a ridge stripe structure 1301, etched mirror region 1302 and chip scribe line 1303, on the island-like semiconductor layers 119 in FIG. 14(b). The etched mirror region 1302 is located based on optical resonance length, as is the chip scribe line 1303.

The etching process for GaN etching uses an Ar ion beam and $Cl_2$ ambient gas. The etching depth is from about 1 μm to about 4 μm. The etched mirror facet may be coated by a dielectric film selected from the group of the following: $SiO_2$, $Al_2O_3$, AlN, AlON, SiN, SiON, $TiO_2$, $Ta_2O_5$, $Nb_2O_5$, $Zr_2O$, etc.

*Chip division*

FIGS. 13(a)-13(b) and 14(a)-14(b) also illustrate the chip division method.

The chip division method has two steps. The first step is to scribe the island-like semiconductor layers 119. The second step is to divide the support substrate 1001 using a laser scribe, etc.

As shown in both FIGS. 13(b) and 14(b), the chip scribe line 1303 is fabricated by a diamond scribing machine or laser scribe machine. The chip scribe line 1303 is fabricated on the back side of the island-like semiconductor layers 119. The chip scribe line 1303 may be a solid line or a dashed line.

Next, the support substrate 1001 is divided by laser scribing as well to obtain a laser diode device. It is better to avoid the ridge strip structure 1301 when the chip scribe line 1303 is fabricated.

*Process steps*

FIG. 15 is a flowchart that illustrates the method of removing GaN-based substrates from GaN-based semiconductor layers, after forming devices from the GaN-

based semiconductor layers, so that the GaN-based substrates can be recycled, according to one embodiment of the present invention.

Block 1501 represents the step of providing a base substrate 101. In one embodiment, the base substrate 101 is a III-nitride-based substrate 101, such as a GaN-based substrate 101.

Block 1502 represents an optional step of depositing an intermediate layer 103 on the substrate 101. In one embodiment, the intermediate layer 103 is a III-nitride-based layer 103, such as a GaN-based layer 103.

Block 1503 represents the step of forming a growth restrict mask 102 on or above the substrate 101, i.e., on the substrate 101 itself or on the intermediate layer 103. The growth restrict mask 102 is patterned to include a plurality of stripes 104 and opening areas 105.

Block 1504 represents the step of growing one or more semiconductor layers 106 on or above the growth restrict mask 102 using epitaxial lateral overgrowth (ELO), wherein the epitaxial lateral growth of the semiconductor layers 106 extends in a direction parallel to the opening areas 105 of the growth restrict mask 102, and the epitaxial lateral overgrowth is stopped before the semiconductor layers 106 coalesce on the stripes 104. In one embodiment, the ELO layer 106 is an ELO III-nitride-based layer 106, such as an ELO GaN-based layer 106.

Block 1505 represents the step of growing one or more semiconductor device layers 108 on the ELO layer 106. These device layers 108, along with the ELO layer 106, create one or more of the island-like semiconductor layers 119.

Block 1506 represents the step of etching at least a portion of the semiconductor device layers 108 in the etching region 117 to remove the etched portion of the semiconductor device layers 108 and expose at least a portion of the growth restrict mask 102. The etching may include etching at least a portion of the device layers 108 above an opening area 105 of the growth restrict mask 102, and may continue below the surface of

the substrate 101. The etching may also include removing a layer bending region 118 from the semiconductor layers 108.

Block 1507 represents the step of bonding the island-like semiconductor layers 119 to a support substrate 1001. The island-like semiconductor layers 119 are flip-chip bonded to a support substrate 1001 with metal or solder 1002 deposited thereon using metal-metal bonding or soldering techniques.

Block 1508 represents the step of at least partially dissolving the growth restrict mask 102 by etching to remove the substrate 101 from the island-like semiconductor layers 119. The growth restrict mask 102 is at least partially removed by the etching, which lifts off the substrate 101 from the island-like semiconductor layers 119. Further, the island-like semiconductor layers 119 may be peeled from the substrate 101.

Block 1509 represents the step of depositing n-electrodes on the back side of the island-like semiconductor layers 119, which is exposed by the lift-off of the substrate 101.

Block 1510 represents the step of chip scribing to separate the devices. This step may also include the etching of facets for laser diode devices.

Block 1511 represents the resulting product of the method, namely, one or more III-nitride-based semiconductor devices fabricated according to this method, as well as a substrate 101 that has been removed from the devices and is available for recycling and reuse.

Advantages and Benefits

The present invention provides a number of advantages and benefits:

- Expensive III-nitride-based substrates 101 can be reused after the substrates 101 are removed from the device layers 108.
- High quality device layers 108 may be obtained using a substrate 101 of the same or similar materials, with a very low defect density.

- Using the same or similar materials for both the substrate 101 and the device layers 108 can reduce the strain in the device layers 108.
- Using materials with the same or similar thermal expansion for both the substrate 101 and the device layers 108 can reduce bending of the substrate 101 during epitaxial growth.
- Slicing the substrate 101 from a bulk crystal with a mis-cut orientation maintains the uniformity of thickness between the device layers 108 and produces a higher yield.
- Layers 106 grown by ELO are of high quality.
- The ELO layers 106 do not coalesce with each other, and internal strain is released, which helps to avoid any occurrences of cracks. For device layers 108 that are AlGaN layers, this is very useful, especially in the case of high Al content layers.
- The island-like semiconductor layers 119 are formed in isolation, so tensile stress or compressive stress does not fall upon other island-like semiconductor layers 119.
- Also, the growth restrict mask 102 and the ELO layers 106 are not bonded chemically, so the stress in the ELO layers 106 and device layers 108 can be relaxed by a slide caused at the interface between the growth restrict mask 102 and the ELO layers 106.
- The existence of the no-growth regions 107 between each of the island-like semiconductor layers 119 provides flexibility, and the substrate 101 is easily deformed when external force is applied and can be bended. Therefore, even if there occurs a slight warpage, curvature, or deformation in the substrate 101, this can be easily corrected by a small external force, to avoid the occurrence of cracks. As a result, the handling of the

substrates 101 by vacuum chucking is possible, which makes the manufacturing process of the semiconductor devices more easily carried out.

- The no-growth region 107 makes it is easy to dissolve a large area of the growth restrict mask 102.
- Device layers 108 of high quality semiconductor crystal can be grown by suppressing the curvature of the substrate 101, and further, even when the device layers 108 are very thick, the occurrences of cracks, etc., can be suppressed, and thereby a large-area semiconductor device can be easily realized.
- Thermal management of the devices improve significantly due to the flip-chip bonding on the support substrate.
- The chip size is reduced by about 10 times when compared to the commercially available devices.
- The fabrication method can also be easily adopted to large size wafers (>2 inches).

Modifications and Alternatives

A number of modifications and alternatives can be made without departing from the scope of the present invention.

Specifically, the III-nitride-based substrates may be basal c-plane {0001}; nonpolar a-plane {1 1 -2 0} and m-plane {1 0 -1 0} families; and semipolar plane families that have at least two nonzero h, i, or k Miller indices and a nonzero l Miller index, such as the {2 0 -2 -1} planes. Semipolar substrates of (20-2-1) are especially useful, because of the wide area of flattened ELO growth, which is very difficult to obtain with sapphire substrates.

Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A method of removing a substrate, comprising:

forming a growth restrict mask on or above a III-nitride-based substrate;

growing one or more III-nitride-based semiconductor layers on or above the III-nitride-based substrate using the growth restrict mask to create one or more island-like semiconductor layers;

bonding the island-like semiconductor layers to a support substrate; and

removing the III-nitride-based substrate from the island-like semiconductor layers, using the support substrate.

2. The method of claim 1, wherein removing the III-nitride-based substrate from the island-like semiconductor layers comprises dissolving at least a portion of the growth restrict mask by etching to remove the III-nitride-based substrate from the island-like semiconductor layers.

3. The method of claim 1, wherein removing the the III-nitride-based substrate from the island-like semiconductor layers comprises peeling the island-like semiconductor layers from the III-nitride-based substrate, using the support substrate.

4. The method of claim 1, wherein the III-nitride-based substrate is bonded to a support substrate.

5. The method of claim 1, wherein the III-nitride-based substrate is recycled after the III-nitride-based substrate is removed from the island-like semiconductor layers.

6. The method of claim 1, wherein the growth restrict mask is patterned.

7. The method of claim 6, wherein the growth restrict mask is comprised of a plurality of stripes and opening areas.

8. The method of claim 7, wherein the growth of one or more of the III-nitride-based semiconductor layers extends in a direction parallel to the opening areas of the growth restrict mask.

9. The method of claim 1, wherein one or more of the III-nitride-based semiconductor layers are grown by epitaxial lateral overgrowth (ELO).

10. The method of claim 9, wherein the epitaxial lateral overgrowth is stopped before the one or more of the III-nitride-based semiconductor layers coalesce.

11. The method of claim 1, wherein at least a portion of the III-nitride-based semiconductor layers is removed by etching to expose at least a portion of the growth restrict mask.

12. The method of claim 1, wherein at least a portion of the growth restrict mask is removed by etching to expose at least a portion of the III-nitride-based substrate.

13. The method of claim 1, wherein at least a portion of the growth restrict mask is removed by etching at least a portion of the III-nitride-based semiconductor layers above an opening area of the growth restrict mask.

14. The method of claim 1, further comprising removing a layer bending region from the III-nitride-based semiconductor layers.

15. A device fabricated by the method of claim 1.

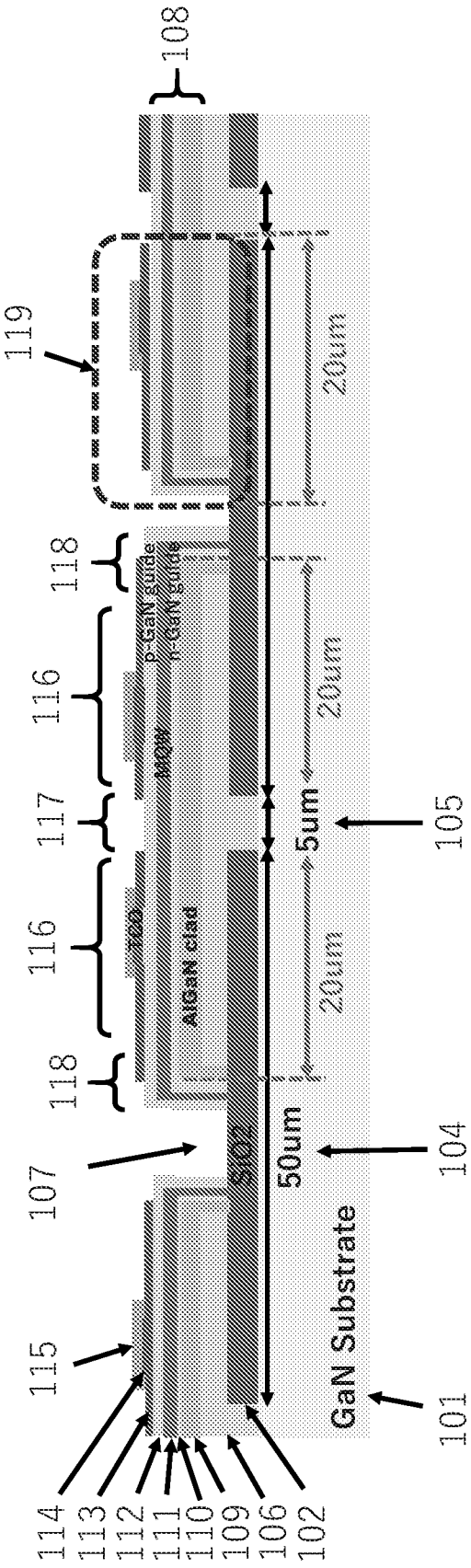

108
119
118
116
117
116
118
107
115
114
113
112
111
110
109
106
102
p-GaN guide
n-GaN guide
MQW
AlGaN clad
TCO
SiO2
GaN Substrate
20um
20um
20um
5um
50um
105
104
101

FIG. 1

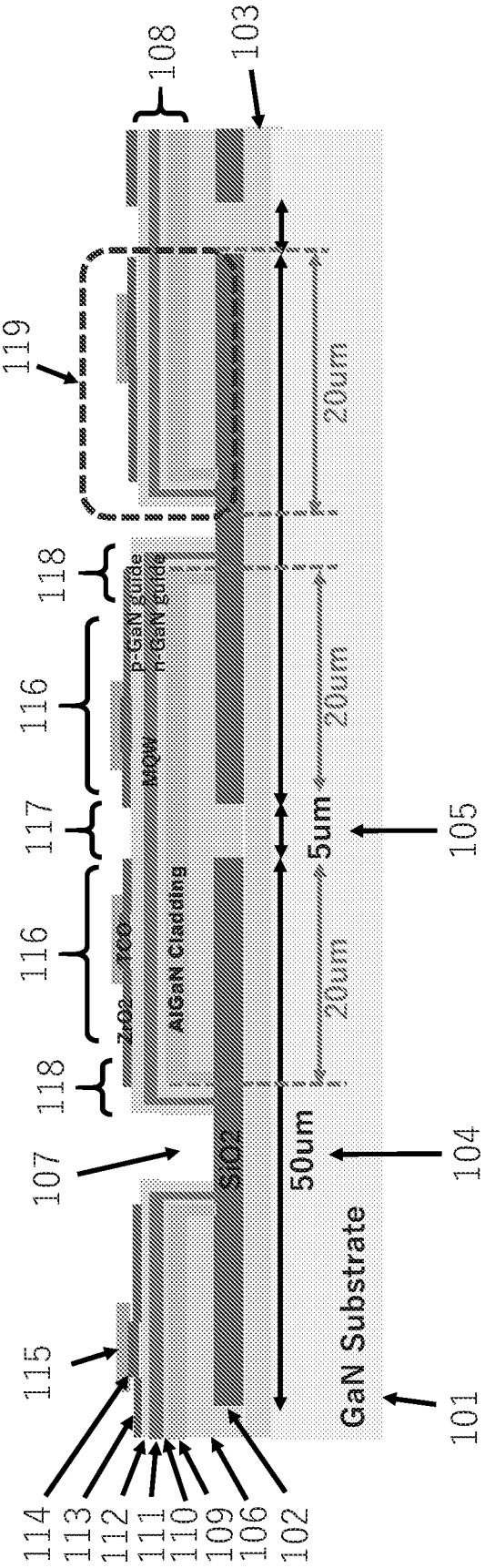

108
103
119
118
116
117
116
118
107
115
114
113
112
111
110
109
106
102
101
104
105
P-GaN guide
n-GaN guide
MQW
AlGaN Cladding
SiO2
GaN Substrate
50um
5um
20um
20um
20um
20um

FIG. 2

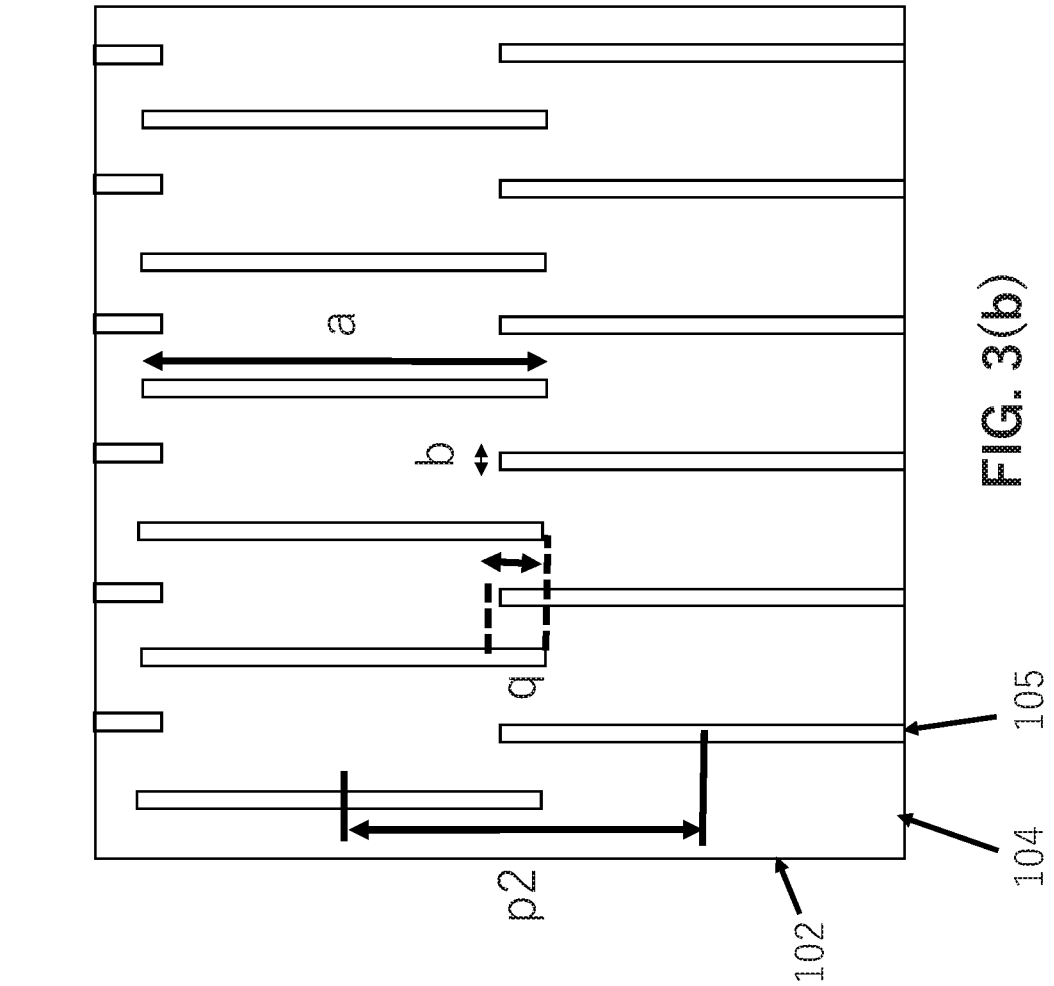



FIG. 3(b)

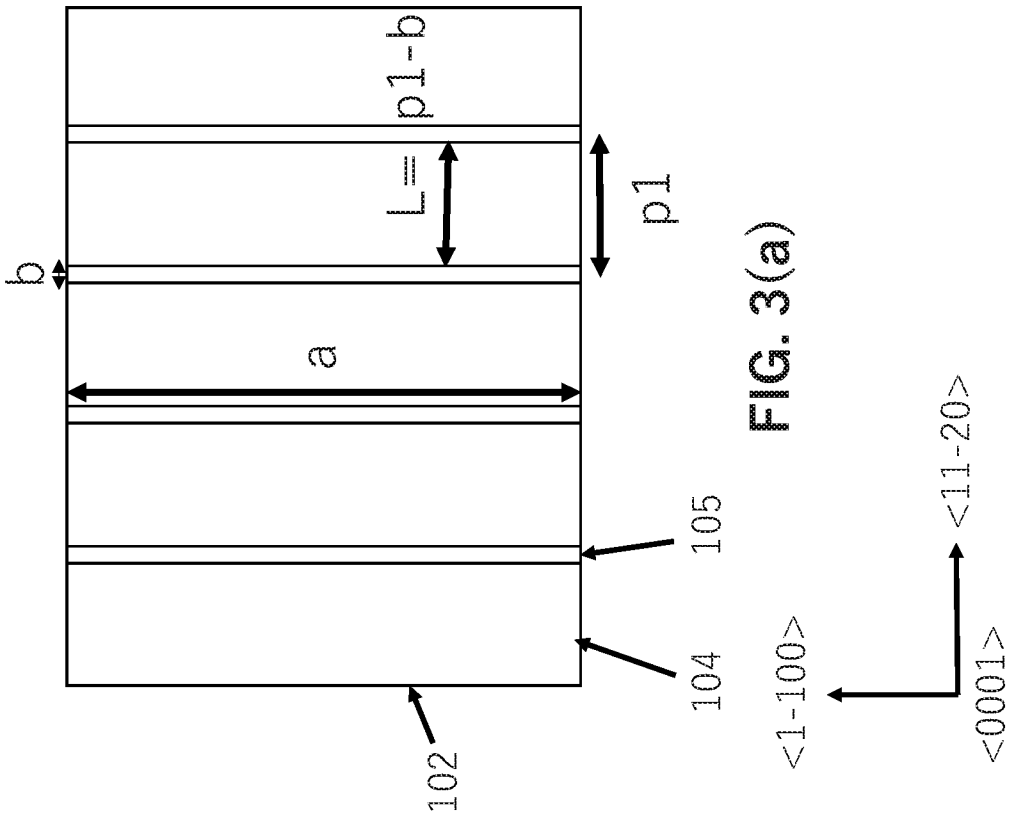



FIG. 3(a)

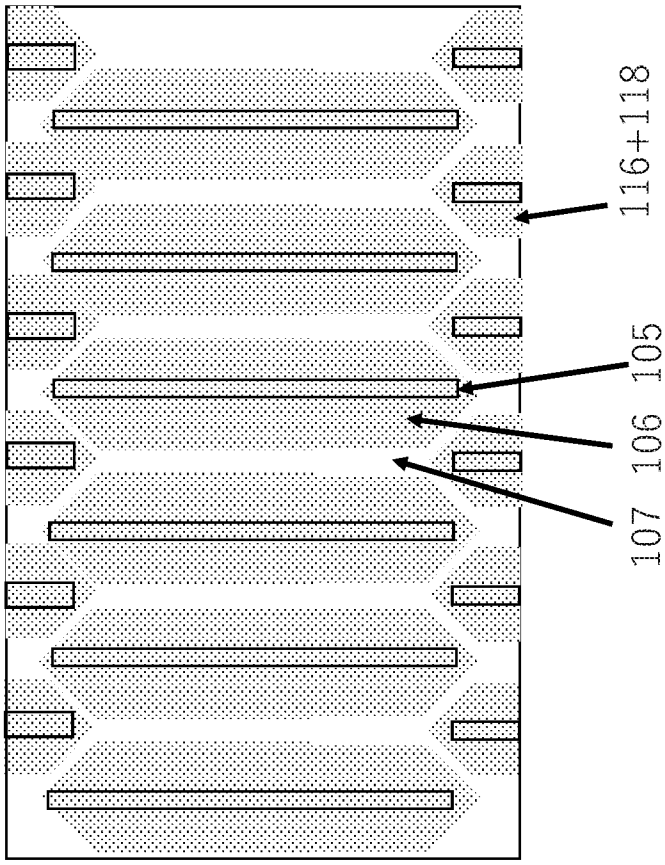



FIG. 4(b)

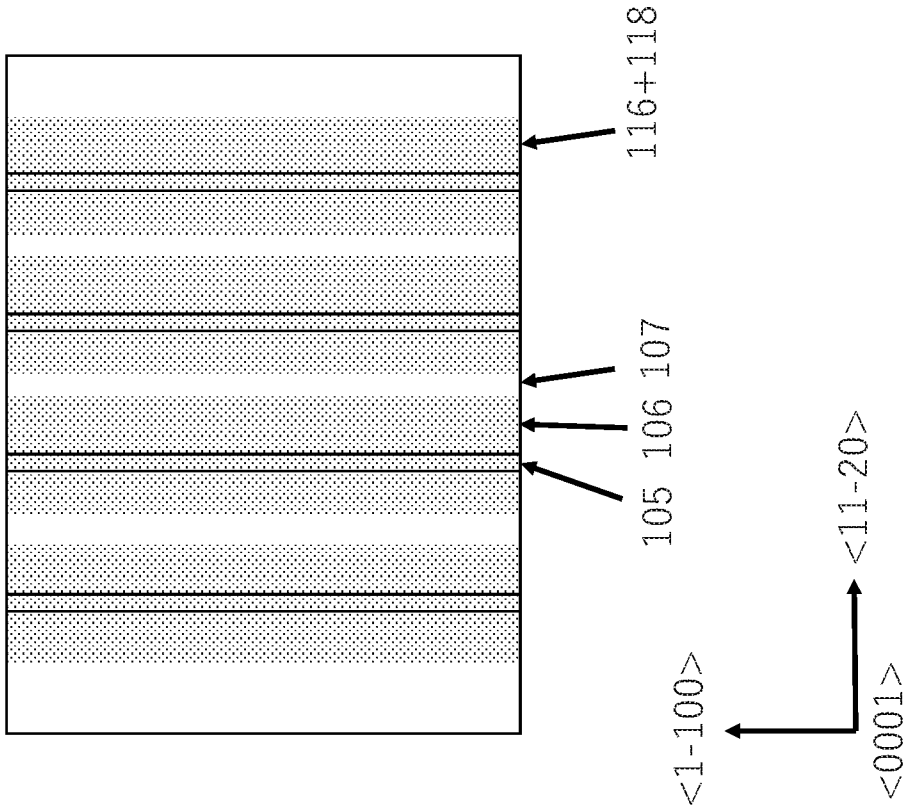



FIG. 4(a)

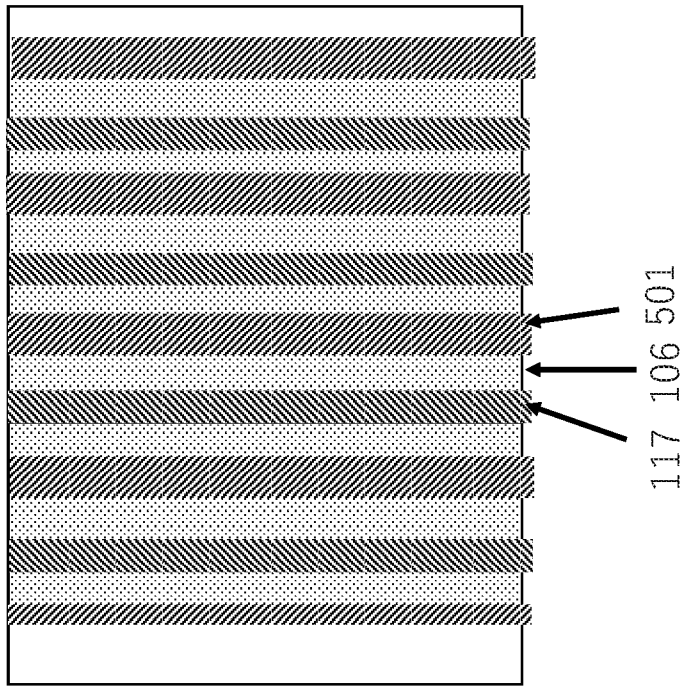



FIG. 5(b)

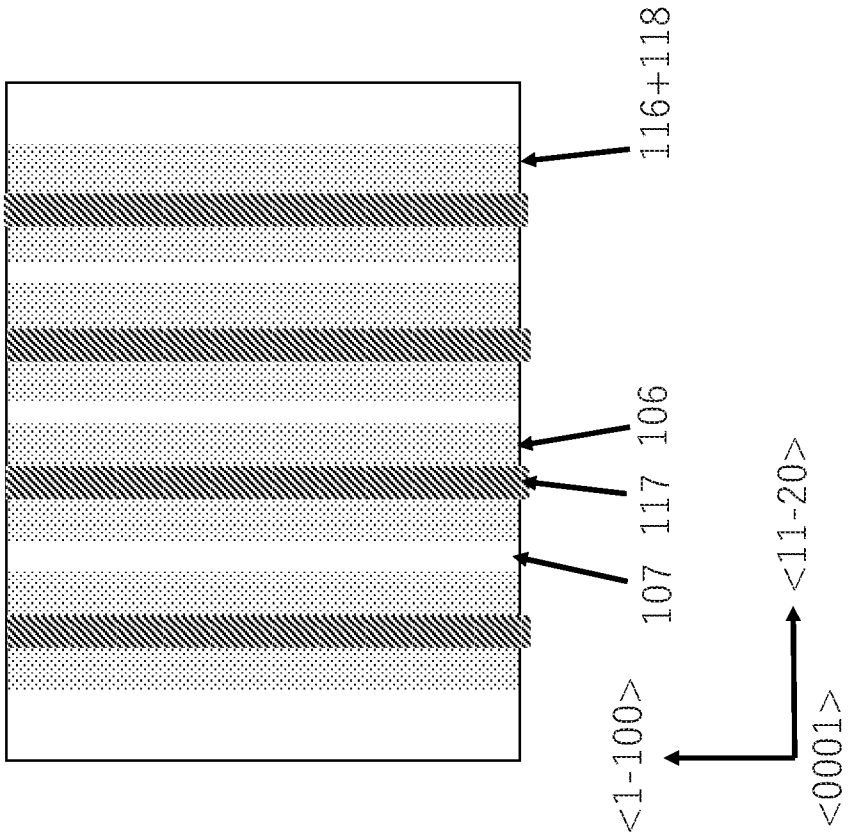



FIG. 5(a)

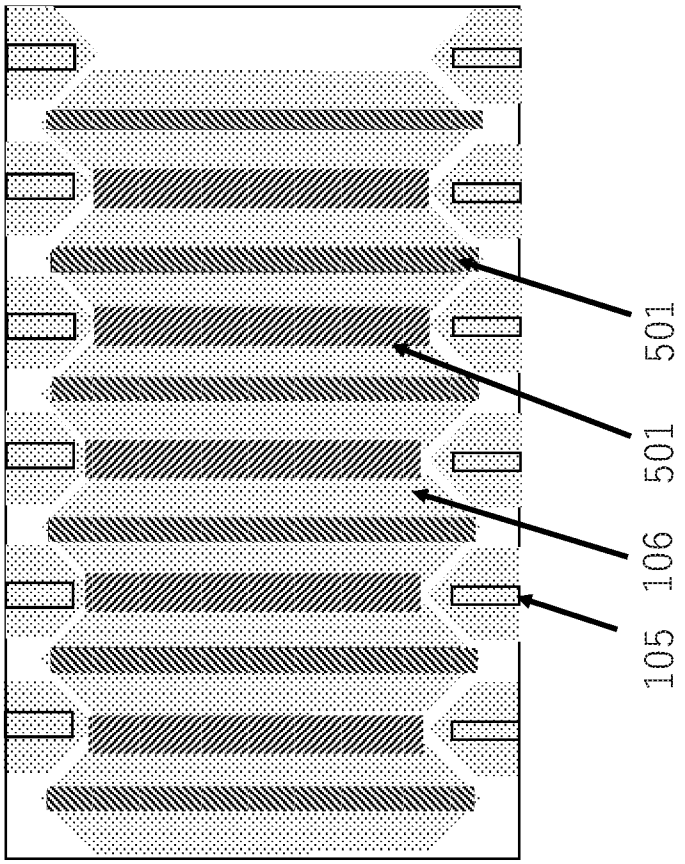



FIG. 6(b)

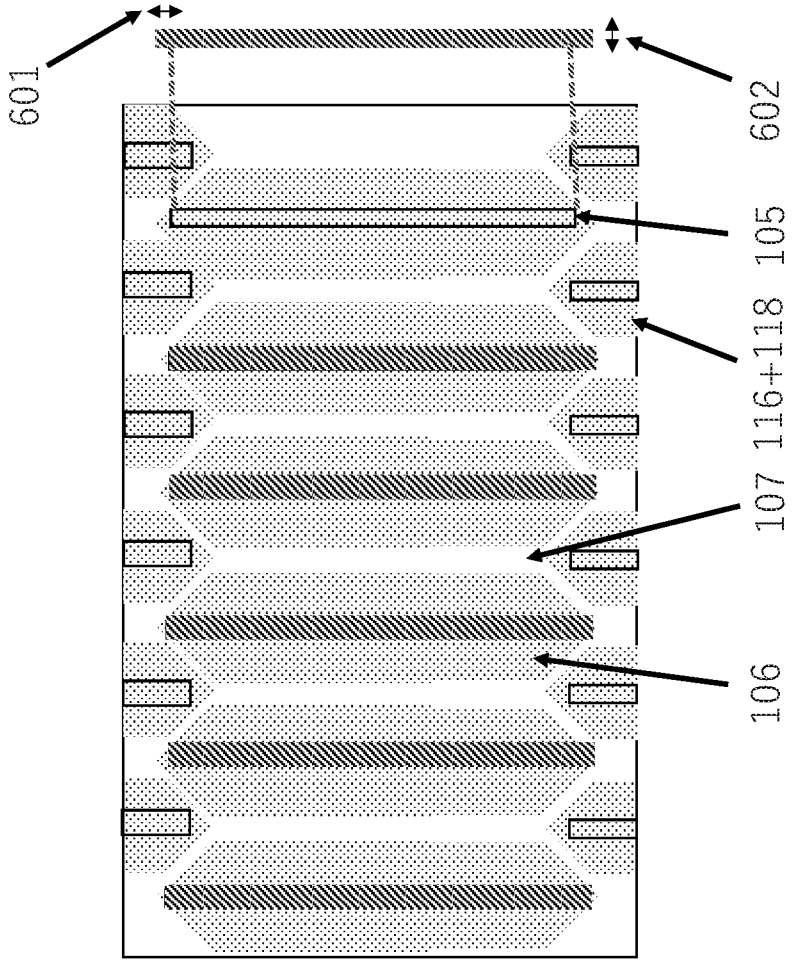



FIG. 6(a)

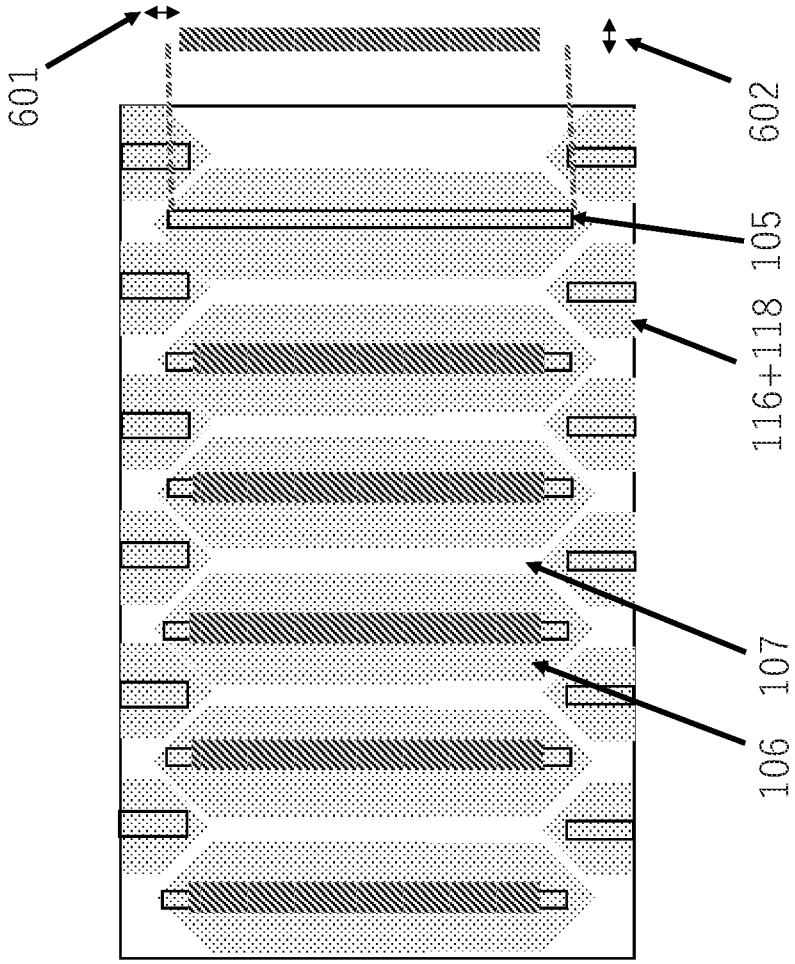



FIG. 6(c)

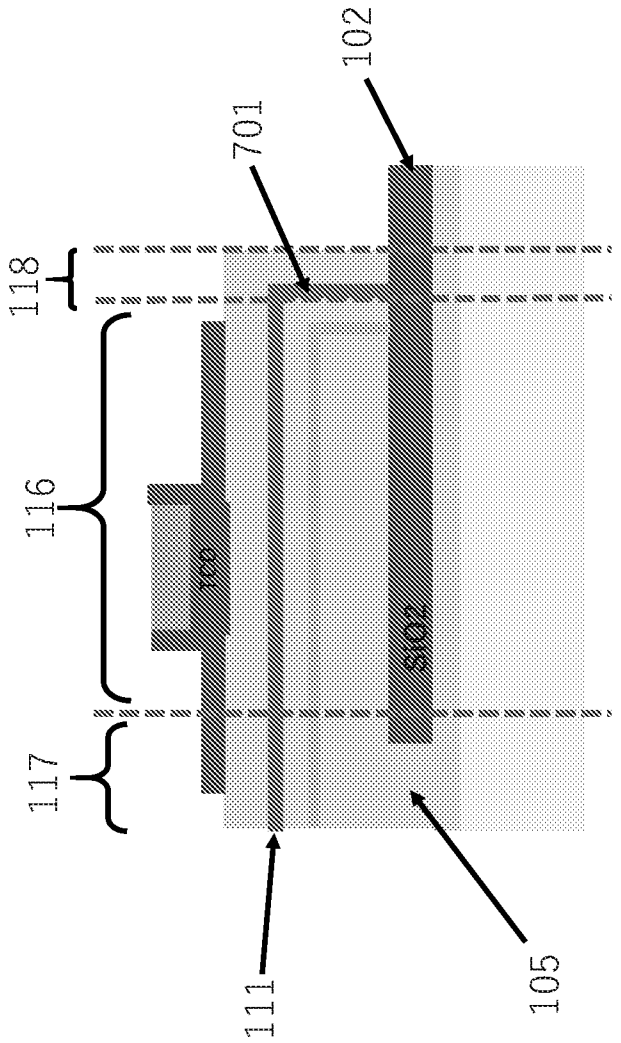



FIG. 7

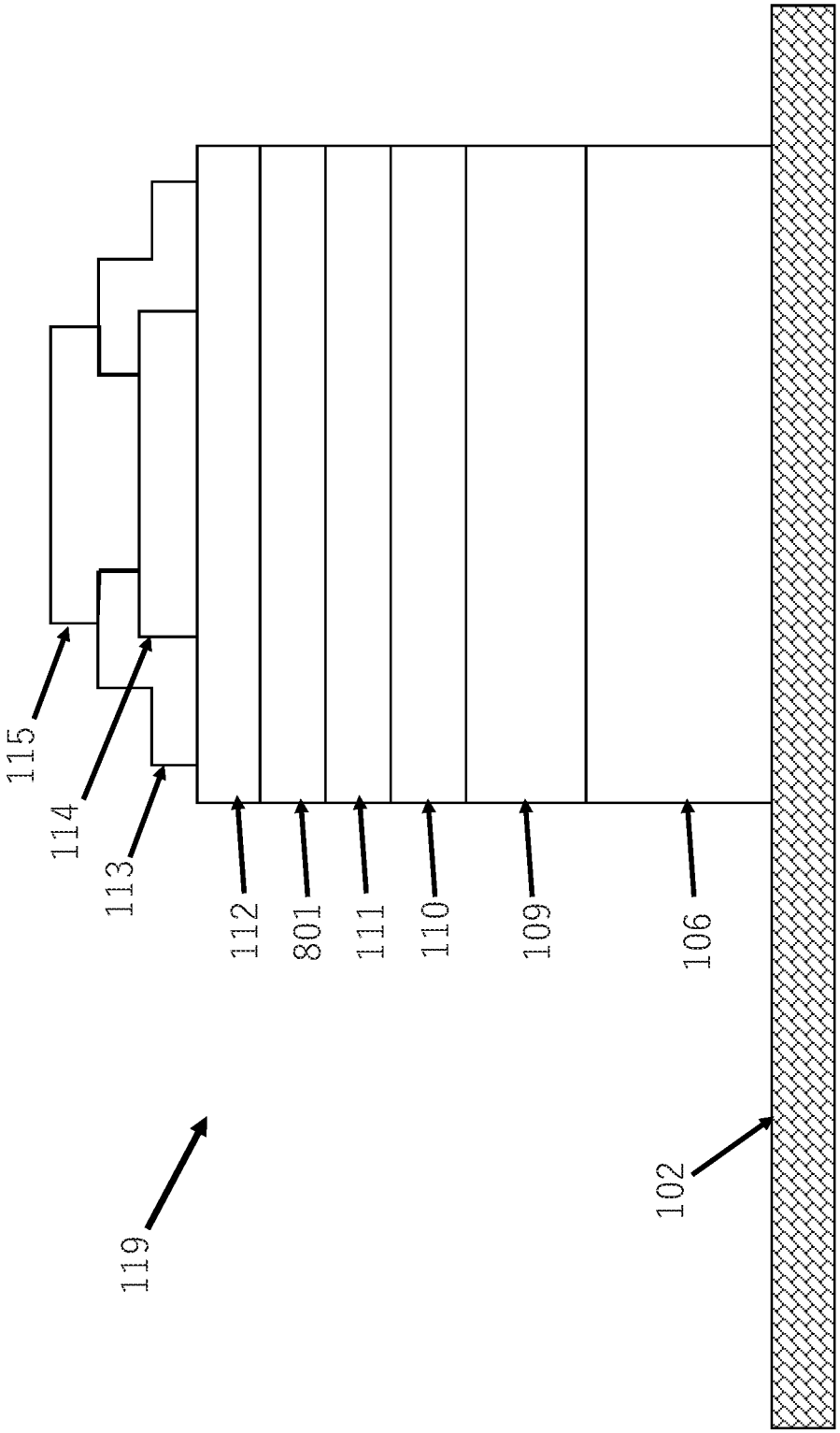



FIG. 8

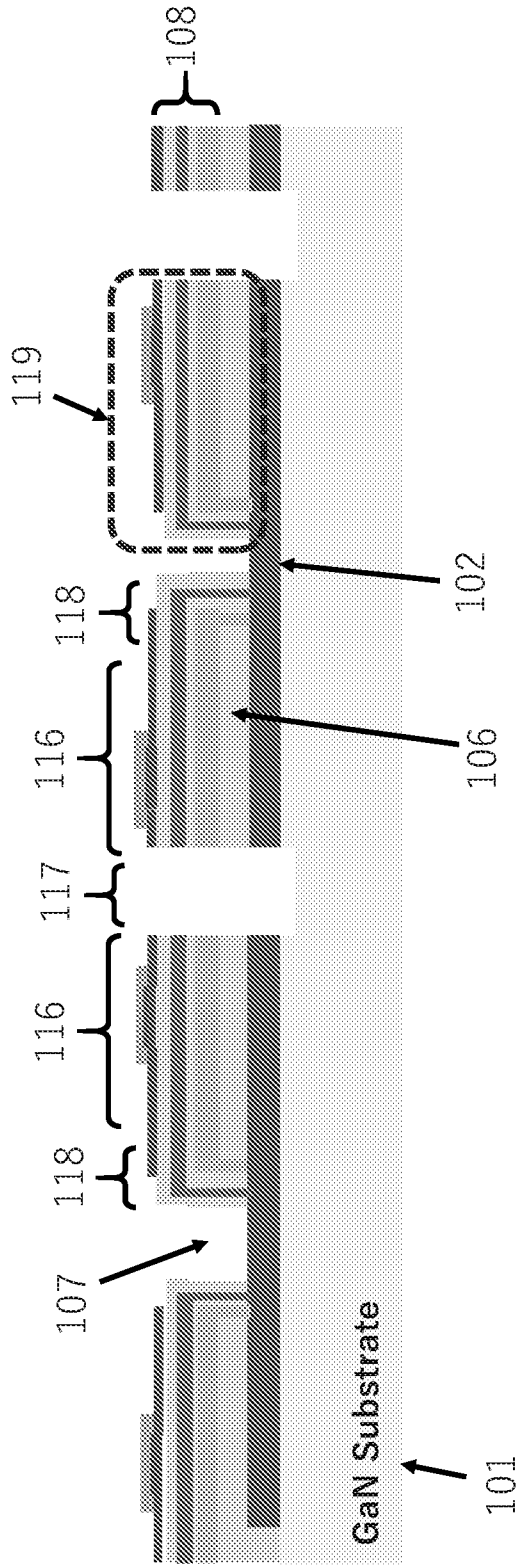



FIG. 9

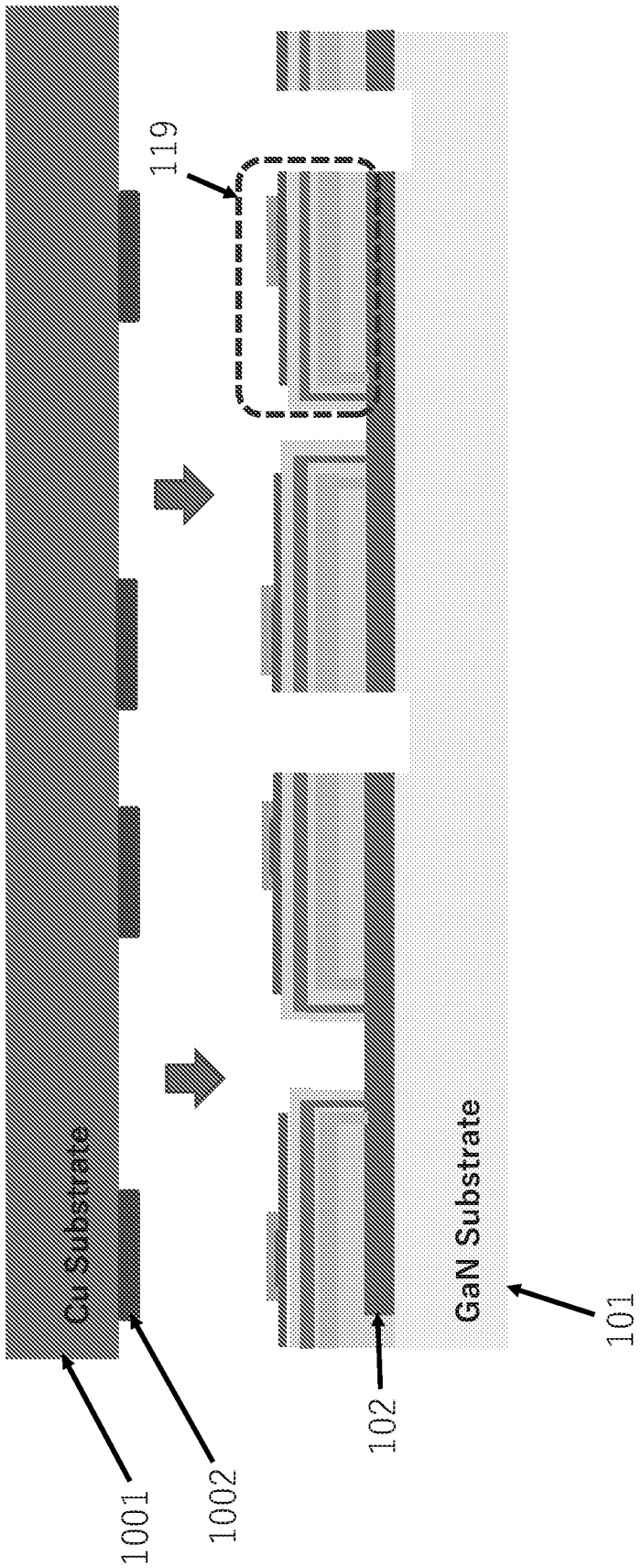



FIG. 10

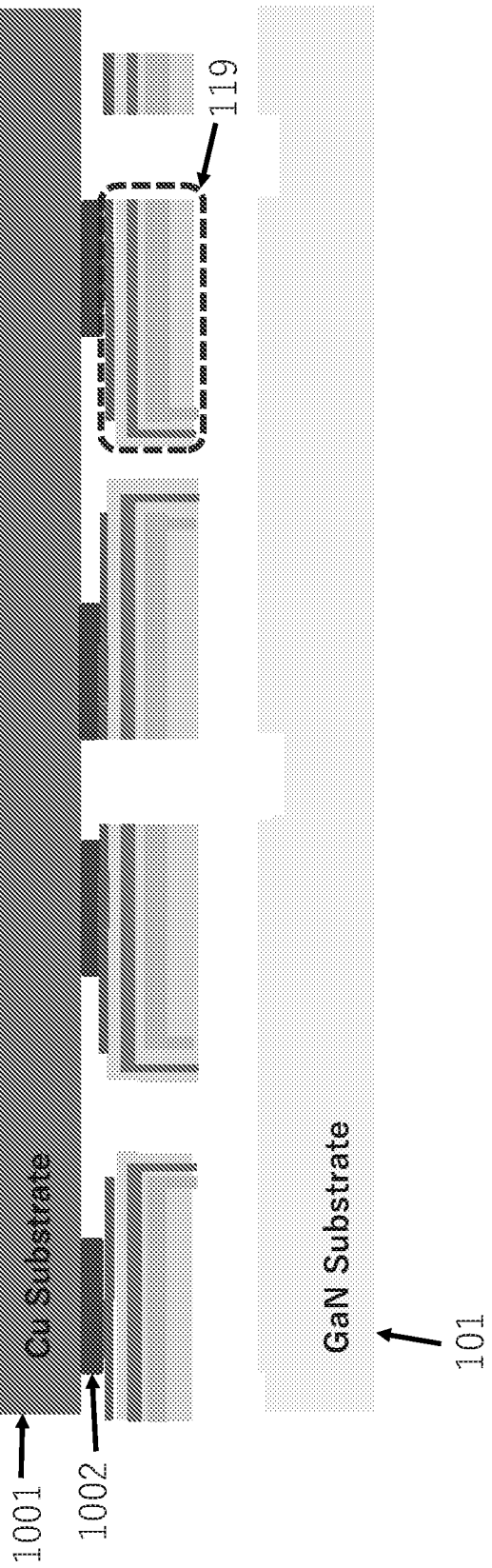



FIG. 11

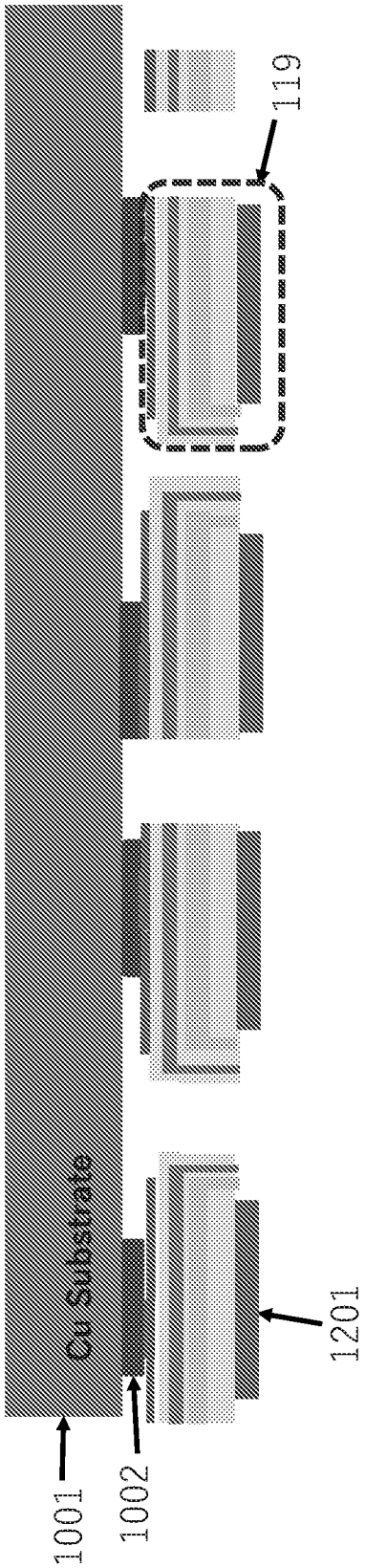



FIG. 12

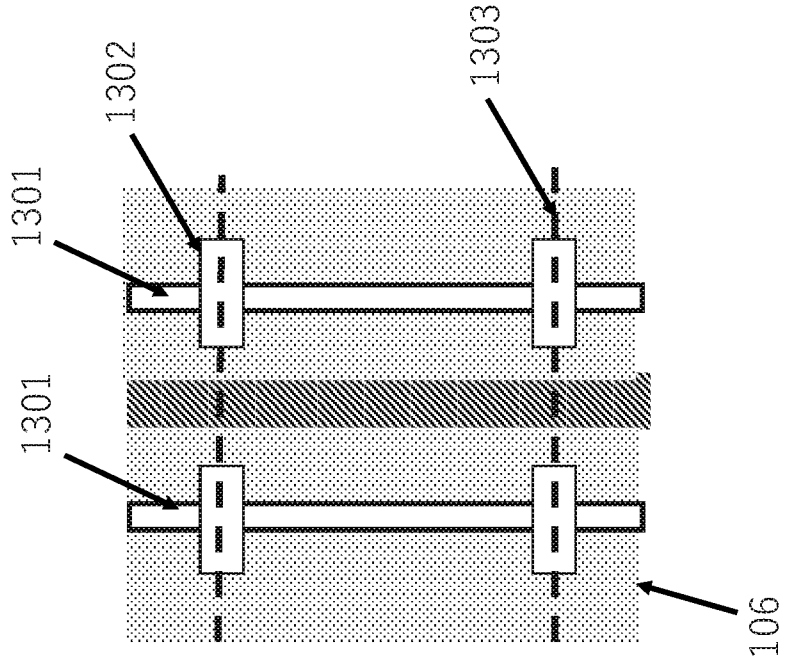



FIG. 13(b)

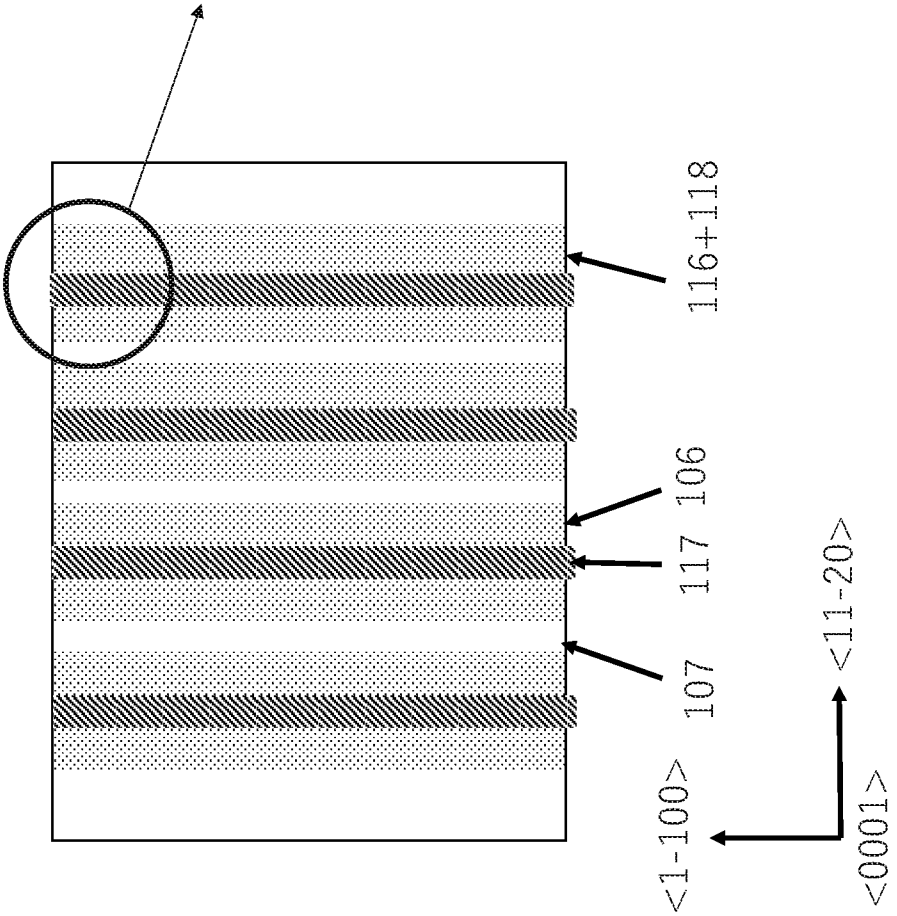



FIG. 13(a)

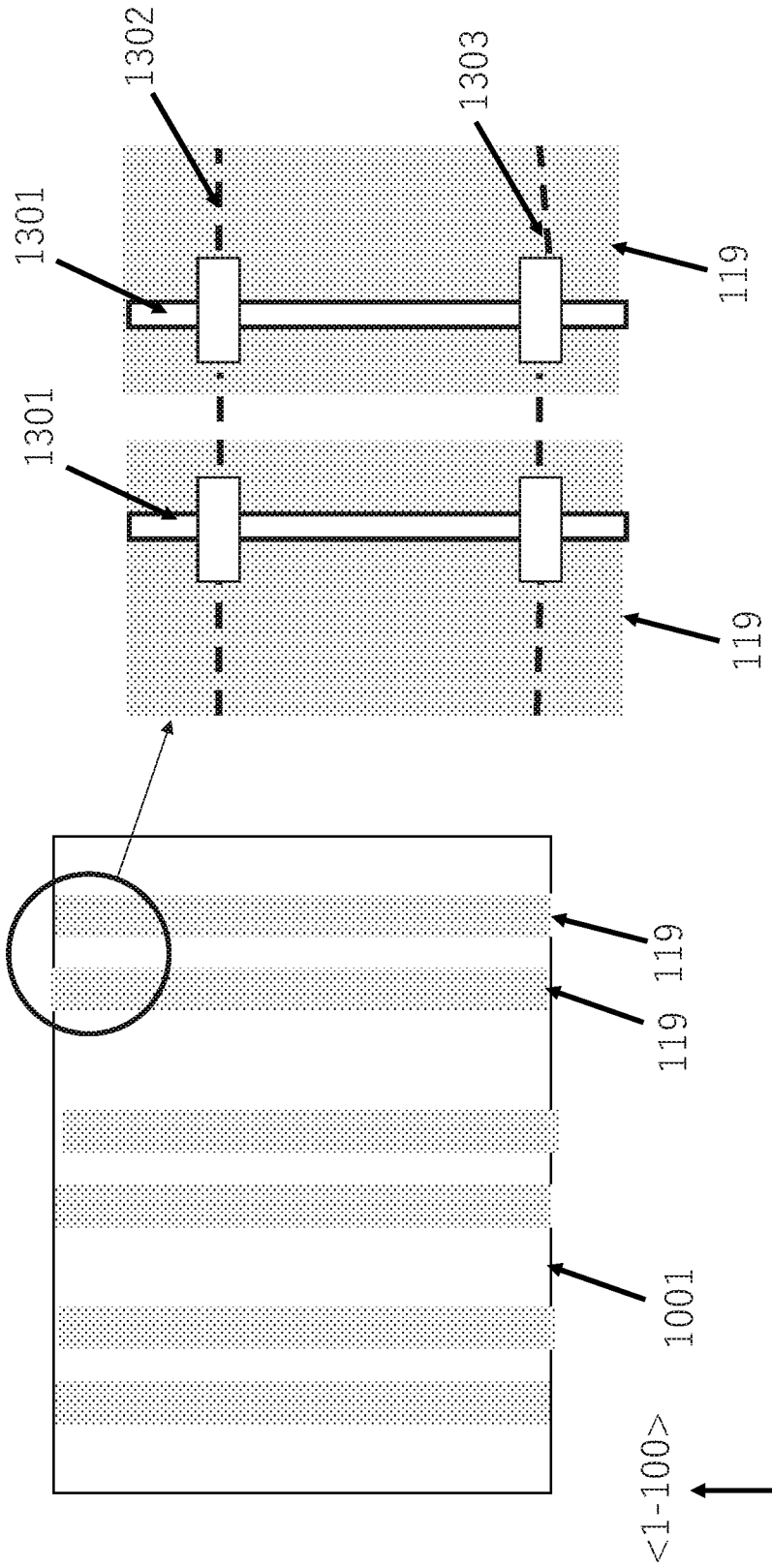



FIG. 14(b)

FIG. 14(a)

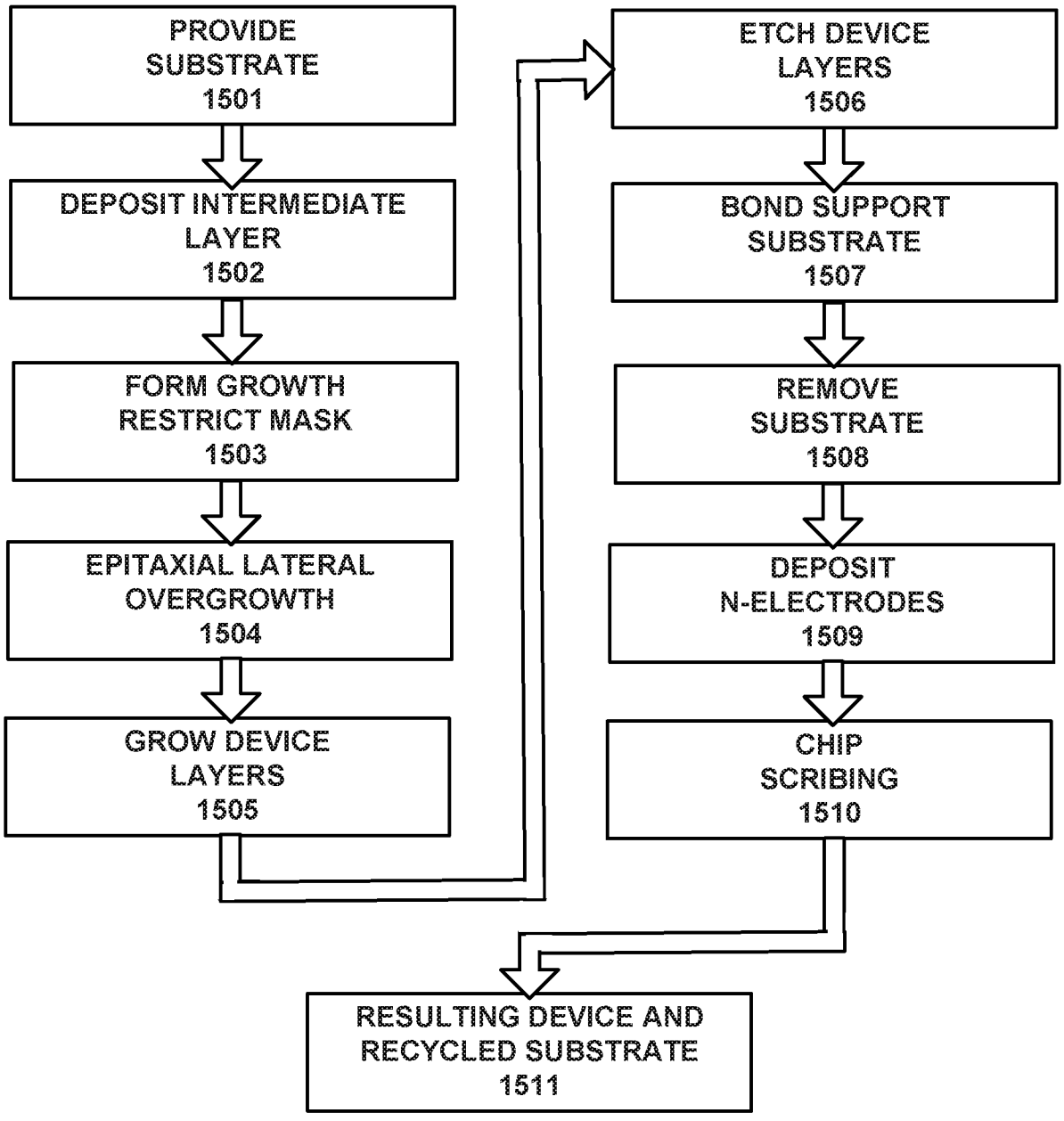

PROVIDE SUBSTRATE 1501
DEPOSIT INTERMEDIATE LAYER 1502
FORM GROWTH RESTRICT MASK 1503
EPITAXIAL LATERAL OVERGROWTH 1504
GROW DEVICE LAYERS 1505
ETCH DEVICE LAYERS 1506
BOND SUPPORT SUBSTRATE 1507
REMOVE SUBSTRATE 1508
DEPOSIT N-ELECTRODES 1509
CHIP SCRIBING 1510
RESULTING DEVICE AND RECYCLED SUBSTRATE 1511

*FIG. 15*

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 18/31393

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 33/00, H01L 33/20, H01L 33/32, H01L 33/46 (2018.01)
CPC - H01L 33/0075, H01L 33/0079, H01L 33/0095, H01L 33/20, H01L 33/32, H01L 33/46, H01L 2933/0025

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>---<br>Y<br>---<br>A | US 2015/0318436 A1 (SEOUL VIOSYS CO., LTD.) 05 November 2015 (05.11.2015), abstract; para [0011], [0018], [0019], [0062]-[0084], [0098], [0106]-[0108] | 1, 2, 4-13, 15<br>----------<br>3<br>----------<br>14 |
| Y | US 2012/0280363 A1 (SUMIDA et al.) 08 November 2012 (08.11.2012), para [0017], [0019], [0135] | 3 |
| A | US 2004/0057482 A1 (WANG) 25 March 2004 (25.03.2004), entire document | 1-15 |
| A | US 2006/0220042 A1 (YAEGASHI et al.) 05 October 2006 (05.10.2006), entire document | 1-15 |
| A | US 2006/0084245 A1 (KOHDA) 20 April 2006 (20.04.2006), entire document | 1-15 |
| A | US 2002/0152952 A1 (BEAUMONT et al.) 24 October 2002 (24.10.2002), entire document | 1-15 |
| A | US 2009/0098343 A1 (ARENA et al.) 16 April 2009 (16.04.2009), entire document | 1-15 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 15 July 2018 | 30 JUL 2018 |
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US, Commissioner for Patents<br>P.O. Box 1450, Alexandria, Virginia 22313-1450<br>Facsimile No. 571-273-8300 | Authorized officer:<br>Lee W. Young<br>PCT Helpdesk: 571-272-4300<br>PCT OSP: 571-272-7774 |