Abstract: A gate voltage boosting circuit provides a voltage boost to a gate of a select switching MOS transistor of a spin-torque MRAM cell to prevent a programming current reduction through an MTJ device of the spin-torque MRAM cell. A spin-torque MRAM cell array is composed of spin-torque MRAM cells that include a MTJ element and a select switching device. A local word line is associated with one row of the plurality of spin-torque MRAM cells and is connected to a gate terminal of the select switching devices of the row of MRAM cells to control activation and deactivation. One gate voltage boosting circuit is placed between an associated global word line and an associated local word line. The gate voltage boosting circuits boost a voltage of a gate of the selected switching device during writing of a logical "1" to the MTJ element of a selected spin-torque MRAM cell.
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Boosted Gate Voltage Programming for Spin-torque MRAM Array

Background of the Invention

Related Patent Applications

[0001] U.S. Patent Application Serial Number 11/789,324 filed on April 24, 2007, assigned to the same assignee as the present invention, and incorporated herein by reference in its entirety.

Field of the Invention

[0002] This invention relates generally to circuits and methods for programming memory array structures. More particularly, this invention relates circuits and methods for boosting a gate voltage of a select switching transistor of spin-torque magnetic random access memory (MRAM) cells for programming spin-torque magnetic random access memory (MRAM) cells in an array.

Description of Related Art

[0003] The term Spin-RAM or spin-torque MRAM refers to a spin torque transfer magnetization switching (STS) MRAM. In this context, the term "spin" refers to the angular momentum of electrons passing through an MTJ that will alter the magnetic moment of a free layer of an MTJ device. Electrons possess both electric charge and angular momentum (or spin). It is known in the art that a current of spin-polarized electrons can change the magnetic orientation of a free ferromagnetic layer of an MTJ via an exchange of spin angular momentum. The major difference between conventional MRAM and spin-torque MRAM is their programming mechanism. Programming is accomplished by bi-direction currents passing through the Spin-RAM magnetic layers, while conventional MRAM is programmed by fields generated by external current or currents.
Reading is similar for both types of the memories, namely detecting the resistance difference of magnetic tunnel junction depending on whether the free layer magnetic polarity is parallel or anti-parallel with the fixed layer. The programming currents required for spin-torque MRAM is much lower than the conventional MRAM and allows a more scalable with geometry reduction.

[0004] "A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-Ram", Hosomi, et al., IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest. Dec. 2005, pp.: 459-462, provides a nonvolatile memory utilizing spin torque transfer magnetization switching (STS), abbreviated Spin-RAM. The Spin-RAM is programmed by magnetization reversal through an interaction of a spin momentum-torque-transferred current and a magnetic moment of memory layers in magnetic tunnel junctions (MTJs), and therefore an external magnetic field is unnecessary as that for a conventional MRAM.

[0005] Refer now to Fig. 1 for a block diagram illustrating a spin-torque MRAM cell and its peripheral circuitry of the prior art. A spin-torque MRAM cell 100 consists of an MTJ element 105 and a select switching Metal Oxide Semiconductor (MOS) transistor 110. The MTJ element 105 is composed of a pinned ferromagnetic layer 102 and a free ferromagnetic layer 104, and a tunnel barrier layer 103. The drain of the MOS transistor 110 is connected through a nonmagnetic layer to the pinned ferromagnetic layer 102. The free ferromagnetic layer 104 is connected to a bit line 115 and the source of the MOS transistor 110 is connected the source select line 120. The bit line 115 and source select line 120 are connected to the bipolar write pulse/read bias generator 125. The bipolar write pulse/read bias generator 125 provides the necessary programming current to the MTJ element 105 through the bit line 115 and the source select line 120. The direction being determined by logic state being programmed to the MTJ element 105.
The gate of the select switching MOS transistor 110 is connected to a word line 130. The word line 130 transfers a word line select voltage to the gate of the select switching MOS transistor 110 to activate the select switching MOS transistor 110 for reading or writing the logic state of the MTJ element 105. A sense amplifier 135 has one input terminal connected to the bit line and a second input terminal connected to a voltage reference circuit 140. When the word line 115 has the word line select voltage activated to turn on the select switching MOS transistor 110, the bipolar write pulse/read bias generator 125 generates a bias current that passes through MTJ element 105. A voltage is developed across the MTJ element 105 that is sensed by the sense amplifier 135 and compared with the reference voltage generator to determine the logic state written to the MTJ element 105. This logic state is transferred to the output terminal of the sense amplifier 135 as to the data output signal 145.

Refer to Fig. 2 for a description of an array of spin-torque MRAM cells 100. The spin-torque MRAM cells 100 are arranged in rows and columns. The gate of the MOS transistor of each of the spin-torque MRAM cell 100 on a row of the spin-torque MRAM cells 100 is connected to a word line 200a, 200b, ..., 200n, 20On to receive the word line select signal to activate the MOS transistor for writing and reading of a selected spin-torque MRAM cell 100. One terminal of each of MTJ element of the spin-torque MRAM cells 100 on a column of spin-torque MRAM cells 100 is connected to a bit line 205a, 205b, ..., 205m. The source of each MOS transistor of each of the spin-torque MRAM cells 100 is connected to a source select line 210a, 210b, ..., 210m. During a write operation, a programming voltage is transferred either from a selected bit line 205a, 205b, ..., 205m through the selected spin-torque MRAM cell 100 to the selected source select line 210a, 210b, ..., 210m or from selected source select line 210a, 210b, ..., 210m through the selected spin-torque MRAM cell 100 to the a selected bit line 205a, 205b, ..., 205m, dependent upon the logic state to be written to the selected spin-torque MRAM cell 100.
U. S. Patent Application 2007/0279968 (Luo, et al.) provides a magnetic memory magnetic memory cells attached to local word lines that are in turn connected to global word lines. The magnetic memory further includes bit lines connected to the magnetic elements, and source lines connected to the selection device. Each magnetic memory cell includes a magnetic element and a selection device connected with the magnetic element. The magnetic element is programmed by first and second write currents driven through the magnetic element in first and second directions. The local word lines are connected with the selection device of and have a first resistivity. Each global word line corresponds to a portion of the local word lines and has a resistivity lower than the first resistivity.

U. S. Patent 6,816,405 (Lu, et al.) describes a segmented word line architecture for cross point magnetic RAM. The MRAM includes a plurality of magnetic memory cells, a plurality of local word lines. Each of the local word lines being operatively coupled to at least one memory cell for assisting in writing a logical state of the at least one memory cell. Each of the local word lines are connected to a global word lines. The global word lines are isolated from the memory cells and are coupled by write circuits to the global word lines. Bit lines are operatively coupled to the memory cells for selectively writing a logical state of one or more of the memory cells. Each of the write circuits is configurable as a current source and/or a current sink for supplying and/or returning, respectively, at least a portion of a write current for assisting in writing one or more memory cells. The write circuits are configured to selectively distribute the write current across the global word lines so that stray magnetic field interaction between selected memory cells and half-selected and/or unselected memory cells is reduced.

U. S. Patent 7,345,945 (Jeon, et al.) teaches a line driver circuit for a semiconductor memory device. The semiconductor memory device has a word line driver circuit configured in stages. A plurality of sub word line driver circuits are connected, in parallel, to each main word line, and provide a sub word line enable signal to a selected sub word line in
response to a main word line enable signal provided through a main word line. A plurality of (local) word line driver circuits are connected in parallel, to each sub word line and provide a local word line enable signal to a selected local word line in response to the (main/sub) word line enable signal so as to operate a plurality of memory cells connected to the selected local word line.

[0011] U. S. Patent 6,424,563 (Honigschmid) describes an MRAM memory cell that includes a magnetoresistive resistor and a switching transistor. The magnetoresistive resistor is located between a central metallization plane and an upper metallization plane. The central metallization plane serves for the word line stitch and also for writing. A word line boost circuit is provided in the stitch region of each cell, with the result that the critical voltage is not achieved in the magnetoresistive resistor but the switching transistor can be turned on.

Summary of the Invention

[0012] An object of this invention is to provide voltage boost to a gate of a select switching MOS transistor of the spin-torque MRAM cell to prevent a programming current reduction through an MTJ device of a spin-torque MRAM cell.

[0013] To accomplish at least this object, various embodiments include a spin-torque MRAM cell array that has a plurality of spin-torque MRAM cells arranged in rows and columns. Each of the spin-torque MRAM cells includes a magnetic tunnel junction element and a select switching device. The select switching device has a drain terminal connected to a first terminal of the magnetic tunnel junction element. The spin-torque MRAM cell array has a plurality of local word lines. Each local word line is associated with one row of the plurality of spin-torque MRAM cells and connected to a gate terminal of the select switching device of each spin-torque MRAM cell on each row to control activation and deactivation of the select switching device. The spin-torque MRAM cell array has
plurality of gate voltage boosting circuits where each gate voltage boosting circuit is placed between an associated global word line of a plurality of global word lines and an associated local word line of the plurality of local word lines. The gate voltage boosting circuits boost a local word line voltage applied to a gate of the selected switching device during writing of a first level (a logical "1") to the magnetic tunnel junction element of a selected spin-torque MRAM cell when activated by a local word line control signal.

[0014] Each of the plurality of gate voltage boosting circuits incorporates a high voltage switching transistor having a drain terminal connected to the global word line associated with the gate voltage boosting circuit. A source of the high voltage switching transistor is connected to the gate of the select switching device and a gate of the high voltage switching transistor is connected to receive the local word line control signal to activate and deactivate the high voltage switch transistor for boosting the local word line voltage. In some embodiments, each of the plurality of gate voltage boosting circuits further includes a clamping device to prevent an over boost condition.

[0015] The spin-torque MRAM cell array further includes a plurality of bit lines. Each bit line is associated with one column of the columns of the plurality of spin-torque MRAM cells and is connected to a second terminal of the magnetic tunnel junction element. A common source line is connected to a source of each of the select switching devices of the plurality of spin-torque MRAM cells to provide a source or sink for a write current for programming the spin-torque MRAM cell. The common source line is connected to a common source select circuit connected to the common source line for selecting the source or sink for the write current.

[0016] The common source line select circuit includes a first transistor having a drain terminal connected to a first voltage source and a source terminal connected to the common source line. A second transistor has a drain terminal connected to the common source line and a source
terminal connected to a ground reference point. The common source line control signals are connected to gates of the first and second transistors to turn on and turn off the first and second transistors to provide a source or sink for the write current through the selected spin-torque MRAM cell during a program operation.

[0017] The spin-torque MRAM cell array includes a plurality of bit line precharge circuits. Each bit line precharge circuit is associated with one column of the plurality of spin-torque MRAM cells and has a third transistor having a drain terminal connected to a first voltage source and a source terminal connected to an associated bit line. A fourth transistor incorporated in the bit line precharge circuit has a drain terminal connected to the associated bit line and a source terminal connected to a ground reference point. The bit line control signals are connected to gates of the third and fourth transistors to turn on and turn off the third and fourth transistors to control directionality of the write current flow through a selected spin-torque MRAM cell during a program operation.

[0018] In various embodiments of the spin-torque MRAM cell array, a selected spin-torque MRAM cell is written to the first level by activating the global word line associated with the selected spin-torque MRAM cell at a first time. The local word line control signal is activated at the first time to effectively connect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell. A data input signal is applied as the first level to a bit line associated with the selected spin-torque MRAM cell to generate a current to program the magnetic tunnel junction element of the selected spin-torque MRAM cell to the first level at the first time. At a second time, the local word line control signal is deactivated to effectively disconnect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell. The local word line associated with the selected spin-torque MRAM cell is thus boosted to a higher voltage level to compensate
for a rise of a voltage at a source of the select switching device of the selected spin-torque MRAM cell.

[0019] In other embodiments, a spin-torque magnetic random access memory device incorporates a plurality of spin-torque MRAM cell arrays arranged in a plurality of groups. Each spin-torque MRAM array has a plurality of spin-torque MRAM cells arranged in rows and columns. Each spin-torque MRAM cell includes a magnetic tunnel junction element and a select switching device. The select switching device has a drain terminal connected to a first terminal of the magnetic tunnel junction element. Each spin-torque MRAM cell array has a plurality of local word lines. Each local word line is associated with one row of the plurality of spin-torque MRAM cells and connected to a gate terminal of the select switching device of each spin-torque MRAM cell on each row to control activation and deactivation of the select switching device.

[0020] Each of the spin-torque MRAM cell arrays has a plurality of gate voltage boosting circuits. Each gate voltage boosting circuit is placed between an associated global word line of a plurality of global word lines and an associated local word line of the plurality of local word lines to boost a voltage of a gate of the selected switching device during writing of a first level to the magnetic tunnel junction element of a selected spin-torque MRAM cell when activated by a local word line control signal;

[0021] Each of the plurality of gate voltage boosting circuits has a high voltage switching transistor. The high voltage switching transistor has a drain terminal connected to the global word line associated with the gate voltage boosting circuit, a source connected to the associated local word line and thus to the gate of the select switching device of each of the spin-torque MRAM cells and a gate of the high voltage switching transistor is connected to receive the local word line control signal for selecting one of the plurality of spin-torque MRAM cells. In some embodiments of the spin-torque magnetic random access memory device, each of the plurality
of gate voltage boosting circuits includes a clamping device to prevent an over boost condition.

[0022] Each of the spin-torque MRAM cell arrays further includes a plurality of bit lines. Each bit line is associated with one column of the columns of the plurality of spin-torque MRAM cells and connected to a second terminal of the magnetic tunnel junction element.

[0023] In various embodiments of the spin-torque magnetic random access memory device, a common source line is connected to a source of each of the select switching devices of the plurality of spin-torque MRAM cells to provide a source or a sink for a write current for programming a selected spin-torque MRAM cell. The common source line of each of the spin-torque MRAM cell arrays is connected to a common source select circuit for selecting the source or sink for the write current. The common source line select circuit has a first transistor having a drain terminal connected to a first voltage source and a source terminal connected to the common source line. A second transistor has a drain terminal connected to the common source line and a source terminal connected to a ground reference point. Common source line control signals are connected to gates of the first and second transistors to turn on and turn off the first and second transistors to provide a source or sink for the write current through the selected spin-torque MRAM cell during a program operation.

[0024] In some embodiments of the spin-torque magnetic random access memory device, the spin-torque MRAM cell array further includes a plurality of bit line precharge circuits. Each bit line precharge circuit is associated with one column of the plurality of spin-torque MRAM cells. Each of the plurality of bit line precharge circuits has a third transistor. The third transistor has a drain terminal connected to a first voltage source and a source terminal connected to an associated bit line. A fourth transistor has a drain terminal connected to the associated bit line and a source terminal connected to a ground reference point. The bit line control signals are connected to gates of the third and fourth transistors to
turn on and turn off the third and fourth transistors to control directionality of the write current flow through a selected spin-torque MRAM cell during a program operation.

[0025] In various embodiments of the spin-torque magnetic random access memory device, a selected spin-torque MRAM cell is written to the first level by activating the global word line associated with the selected spin-torque MRAM cell at a first time. At the first time the local word line control signal is activated to effectively connect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell at the first time. A data input signal as the first level (a logical “1”) is applied to a bit line associated with the selected spin-torque MRAM cell to generate a current to program the magnetic tunnel junction element of the selected spin-torque MRAM cell to the first level at the first time. At a second time, the local word line control signal is deactivated to effectively disconnect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell to boost the local word line associated with the selected spin-torque MRAM cell to a higher voltage level to compensate for a rise of a voltage at a source of the select switching device of the selected spin-torque MRAM cell;

[0026] A method for writing a selected spin-torque MRAM cell in the embodiments of an array of spin-torque MRAM cells to a first level begins by providing a plurality of spin-torque MRAM cells arranged in rows and columns. Each spin-torque MRAM cell has a magnetic tunnel junction element and a select switching device. The select switching device has a drain terminal connected to a first terminal of the magnetic tunnel junction element. A plurality of local word lines is provided. Each local word line is associated with one row of the plurality of spin-torque MRAM cells and connected to a gate terminal of the select switching device of each spin-torque MRAM cell on each row to control activation and deactivation of the select switching device. A plurality of gate voltage boosting circuits is
provided such that each gate voltage boosting circuit is placed between an associated global word line of a plurality of global word lines and an associated local word line of the plurality of local word lines for boosting a voltage of a gate of the selected switching device during writing of a first level to the magnetic tunnel junction element of a selected spin-torque MRAM cell when activated by a local word line control signal.

[0027] To write the selected spin-torque MRAM cell, the global word line associated with the selected spin-torque MRAM cell is activated at a first time. Also at the first time, the local word line control signal is activated to effectively connect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell at the first time. A data input signal as the first level is applied to a bit line associated with the selected spin-torque MRAM cell to generate a current to program the magnetic tunnel junction element of the selected spin-torque MRAM cell to the first level at the first time. To boost the local word line associated with the selected spin-torque MRAM cell to a higher voltage level to compensate for a rise of a voltage at a source of the select switching device of the selected spin-torque MRAM cell, the local word line control signal is deactivated to effectively disconnect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell at a second time.

[0028] In various embodiments, a method for forming a spin-torque MRAM cell array includes the step of forming a plurality of spin-torque MRAM cells arranged in rows and columns. The forming of each spin-torque MRAM cell involves the forming a magnetic tunnel junction element and forming a select switching device. The select switching device is formed having a drain terminal connected to a first terminal of the magnetic tunnel junction element. A plurality of local word lines are formed by associating each local word line with one row of the plurality of spin-torque MRAM cells and connecting each word line to a gate terminal of the select switching device of each spin-torque MRAM cell on its
associated row to control activation and deactivation of the select switching device. A plurality of gate voltage boosting circuits is formed such that forming each gate voltage boosting circuit includes placing each gate voltage boosting circuit between an associated global word line of a plurality of global word lines and an associated local word line of the plurality of local word lines. Each of the gate voltage boosting circuits boosts a voltage of a gate of the selected switching device during writing of a first level to the magnetic tunnel junction element of a selected spin-torque MRAM cell when activated by a local word line control signal.

[0029] Forming each of the plurality of gate voltage boosting circuits includes forming a high voltage switching transistor and connecting a drain terminal to the global word line associated with the gate voltage boosting circuit. A source terminal is connected to the gate of the select switching device. A gate is connected to receive the local word line control signal for selecting one of the plurality of spin-torque MRAM cells. In some embodiments, forming each of the plurality of gate voltage boosting circuits further includes forming a clamping device to prevent an over boost condition.

[0030] The method for forming a spin-torque MRAM cell array further forming a plurality of bit lines. Forming each bit line is accomplished by associating each bit line with one column of the columns of the plurality of spin-torque MRAM cells and connecting to a second terminal of the magnetic tunnel junction element.

[0031] The method for forming a spin-torque MRAM cell array further includes forming a common source line and connecting the common source line to a source of each of the select switching devices of the plurality of spin-torque MRAM cells to provide a source or sink for a write current for programming the spin-torque MRAM cell. A common source select circuit is formed and connected to the common source line for selecting the source or sink for the write current. The common source line select circuit is formed by forming a first transistor having a drain terminal
connected to a first voltage source and a source terminal connected to the common source line. A second transistor is formed with a drain terminal connected to the common source line and a source terminal connected to a ground reference point. Common source line control signals are connected to the gates of the first and second transistors to turn on and turn off the first and second transistors to provide a source or sink for the write current through the selected spin-torque MRAM cell during a program operation.

[0032] A plurality of bit line precharge circuits is formed with each bit line precharge circuit connected with one column of the plurality of spin-torque MRAM cells. Each of the plurality of bit line precharge circuits is formed by forming a third and a fourth transistor. The third transistor has a drain terminal connected to a first voltage source and a source terminal connected to an associated bit line. The fourth transistor has a drain terminal connected to the associated bit line and a source terminal connected to a ground reference point. The bit line control signals are connected to gates of the third and fourth transistors to turn on and turn off the third and fourth transistors to control directionality of the write current flow through a selected spin-torque MRAM cell during a program operation.

**Brief Description of the Drawings**

[0033] Fig. 1 is a block diagram of a spin-torque magnetic tunnel junction memory cell and its peripheral circuitry of the prior art.

[0034] Fig. 2 is schematic diagram of a spin-torque magnetic tunnel junction memory cell array of the prior art.

[0035] Fig. 3 is schematic diagram of an embodiment of a spin-torque magnetic tunnel junction memory cell array of this invention.
Fig. 4 is a timing diagram for programming a logical "1" to a selected spin-torque MRAM cell in a spin-torque MRAM cell array of this invention.

Fig. 5 is a timing diagram for programming a logical "0" to a selected spin-torque MRAM cell in a spin-torque MRAM cell array of this invention.

Fig. 6 is block diagram of a spin-torque magnetic random access memory device of this invention.

**Detailed Description of the Invention**

Referring to Fig. 1, it is known that the gate drive of the select switching MOS transistor 110 of the spin-torque MRAM cell 100 and therefore the current drive capability, of the select switching MOS transistor 110 depends on the voltage between the gate and source (the lower voltage side in case of an NMOSFET) of the select switching MOS transistor 110. When the programming current is in the direction from transistor to MTJ 105, the voltage drop on the MTJ 105 caused the source (Node A) 112 of the select switching MOS transistor 110 to rise. With reasonable programming current and MTJ resistance values used for present state of technology, this voltage rise can be around 0.3V. This voltage rise could cause more than 30% programming current reduction in 1.2v supply voltage operating environment.

An additional effect due to the threshold voltage of the select switching MOS transistor 110 also increased slightly due to a physical phenomenon called body-effect that added reduces the voltage at the source 112 of the select switching MOS transistor 110. The programming current capability of the spin-torque MRAM cell 100 is not symmetric in two directions. Therefore, what is needed is a gate voltage boosting circuit to boost the voltage present on the word line 130 that provides the gate drive voltage of select switching MOS transistor 110 of the spin-torque MRAM cell 100 to compensate for the rise of source voltage at the
junction (Node A) 112 of the MTJ 105 and the select switching MOS transistor 110.

[0041] Fig. 3 is schematic diagram of an embodiment of a spin-torque magnetic tunnel junction memory cell array 300 of this invention. The MRAM cells 305 are arranged in rows and columns. The gate of the select switching MOS transistor 307 of each of the MRAM cells 305 on a row of the MRAM cells 305 is connected to a local word line 320a, 320b, ..., 320m to receive a word line select signal from an associated global word line 315a, 315b, ..., 315m to activate the MOS transistor for writing and reading of a selected MRAM cell 305. Each of the global word lines 315a, 315b, ..., 315m are respectively connected to the row decode drivers 313a, 313b, ..., 313m located within the row decode circuit 310. The row decode drivers 313a, 313b, ..., 313m transfer the word line select signal to the selected global word line 315a, 315b, ..., 315m as a result of a decode of an address signal that designates the location of the selected MRAM cell 305.

[0042] The spin-torque MRAM cell array 300 is shown with a single block or sub-array of MRAM cells 305 and is associated with one bit of the Data D0 (write data D0W 314 and read data D0R392). The data driver 312 is connected to receive the write data D0W and transfer it to the bit lines 335a, ..., 335n through the gating MOS transistor 375a, ..., 375n. The global word lines 315a, 315b, ..., 315m pass through the sub-array, as shown, to other sub-arrays of MRAM cells 305.

[0043] One terminal of each MTJ element 306 of the MRAM cells 305 on a column of MRAM cells 305 is connected to a bit line 335a, ..., 335n. The source of each MOS transistor 307 of each of the MRAM cells 305 present on a row is connected to a common source line 360. During a write, a programming current is transferred either from a selected bit line 335a, ..., 335n through the selected MRAM cell 305 to the common source line 360 or from common source line 360 through the selected
MRAM cell 305 to the a selected bit line 335a, ..., 335n, dependent upon the logic state to be written to the selected MRAM cell 305s.

[0044] The common source line 360 is connected to the common source line select circuit 365. The common source line select circuit 365 includes the MOS transistors 366 and 368. The source of the MOS transistor 366 and the drain of the MOS transistor 368 are connected together and to the common source line 360. The drain of the MOS transistor 366 is connected to the voltage source Vi and the source of the MOS transistor 368 is connected to the ground reference point. The common source control signals 370a and 370b are connected to the gates of the MOS transistors 366 and 368 to selectively activate and deactivate the MOS transistors 366 and 368 to connect the common source line 360 to either the voltage source Vi or the ground reference point, dependent on the logical level of the data being written to the selected MRAM cell 305. In the present embodiment, connecting voltage source Vi provides the voltage for writing a level representing a logical "1" and the ground reference point at the common source line 360 in conjunction with the write data D2W 314 provide the voltage for writing a level representing a logical "0".

[0045] Each of the bit lines 335a, ..., 335n and the reference bit line 335R is connected to the bit line precharge circuit 330. The bit line precharge circuit 330 includes the bit line precharge circuits 340a, ..., 340n, and 340R that are connected respectively to the bit lines 335a, ..., 335n and 335R. The bit line precharge circuits 340a, 340b, ..., 340n, and 340R each include the MOS transistors 341 and 342. The source of the MOS transistor 341 and the drain of the MOS transistor 342 are connected together and to their associated bit lines 335a, ..., 335n. The drain of the MOS transistor 341 is connected to the voltage source V2 and the source of the MOS transistor 342 is connected to the ground reference point.

The bit line control signals 350a and 350b are connected to the gates of all of the bit line precharge circuits 340a, ..., 340n, and 340R to selectively activate and deactivate the MOS transistors 341 and 342 to
connect the bit lines to either the voltage source \( V_2 \) or the ground reference point, dependent on the logical level of the data being written to the selected MRAM cell 305.

[0046] One end of each of the bit lines 335a, ..., 335n is connected to the source of a gating MOS transistor 375a, ..., 375n. The drain of each of the gating MOS transistors 375a, ..., 375n is connected to receive one bit of a data input signal \( D_{314} \) and the gate of each of the gating MOS transistors 375a, ..., 375n is connected to receive a column select signal \( y_0 380a, ..., y_n 380n \) and \( y_r 380R \). The column select signals \( y_0 380a, ..., y_n 380n \) and \( y_r 380R \) are generated by decoding the column address portion of an address signal in a column decoder circuit 355. A group of sense amplifiers 385 are connected to all the array of an MRAM device such the sense amplifier 390 is also connected to each of the bit lines 335a, ..., 335n through the gating MOS transistor 375a, ..., 375n for sensing the logic state (low resistance vs high resistance) of each of each of the MTJ devices 306 of the MRAM cell 305 to read data from a selected MRAM cell(s) 305s.

[0047] One column of the spin-torque MRAM cell array 300 includes the reference MRAM cells 305R1, 305R2, ..., 305Rm. The reference MRAM cells 305R1, 305R2, ..., 305Rm have one terminal of each MTJ element 306 of each of the reference MRAM cells 305R1, 305R2, ..., 305Rm 305 is connected to a reference bit line 335R. The source of each MOS transistor 307 of each of the reference MRAM cells 305R1, 305R2, ..., 305Rm is connected to a common source line 360. The gate of the select switching MOS transistor 307 of each of the reference MRAM cells 305R1, 305R2, ..., 305Rm on a row of the MRAM cells 305 is connected to a local word line 320a, 320b, ..., 320m to receive a word line select signal from an associated global word line 315a, 315b, ..., 315m to activate the MOS transistor of the reference MRAM cells 305R1, 305R2, ..., 305Rm during writing and reading of a selected MRAM cell 305s. The reference bit line 335R is connected through a reference signal averaging circuit 395 to a reference terminal of the sense amplifier 395 for reading
the pre-established program level for each of the reference MRAM cells 305R1, 305R2, ..., 305Rm. The reference read signal 398 is applied to the reference signal averaging circuit 395 during a read operation. The reference signal averaging circuit 395 averages the reference signal from the reference MRAM cells 305R1, 305R2, ..., 305Rm and the reference MRAM cells from an adjacent array 301 to create the averages of the two reference cells. The pre-established program level for each of the reference MRAM cells 305R1, 305R2, ..., 305Rm and the reference MRAM cells from an adjacent array 301 are such that one column is of the reference MRAM cells 305R1, 305R2, ..., 305Rm and the reference MRAM cells from an adjacent array 301 are programmed to a maximum resistance (RMAX) and the other to a minimum resistance (RMIN). These values of resistance provide the necessary reference signal values for the sense amplifier 390.

[0048] Each of the global word lines 315a, 315b, ..., 315m is connected to a gate voltage boosting circuit 325a, 325b, ..., 325m. Each of the gate voltage boosting circuits 325a, 325b, ..., 325m have a high voltage pass transistor 326 with a drain connected to the associated global word line 315a, 315b, ..., 315m and a source connected to the associated local word line 320a, 320b, ..., 320m and thus to the gate of the select switching MOS transistor 307 of each of the MRAM cells 305 of the row of the array 300 of MRAM cells 305. The gates of all of the high voltage pass transistors 326 of the gate voltage boosting circuits 325a, 325b, ..., 325m are commonly connected to the row decode circuit 310 to receive the local word line control signal 345 for activating and deactivating the gate voltage boosting circuits 325a, 325b, ..., 325m. An optional clamp diode 328 may be added to each of the gate voltage boosting circuit 325a, 325b, ..., 325m to further prevent an over boost condition, if necessary. The anode of the optional clamp diode 328 is shown connected to the source of the high voltage pass transistor 326 and the cathode connected to the ground reference point. In other embodiments, the cathode of the optional clamp diode 328 is connected to the source of the high voltage
pass transistor 326 and the anode connected to an appropriate biasing voltage.

[0049] In current semiconductor fabrication processes, the high voltage pass transistor 326 of each of the gate voltage boosting circuits 325a, 325b, ..., 325m may be a transistor type normally used for Input/Output function of an integrated circuit. The Input/Output type transistors operate at a higher voltage level than that select switching MOS transistor 307 of each of the MRAM cells 305.

[0050] Fig. 4 is a timing diagram for programming a logical "1" to a selected spin-torque MRAM cell in a spin-torque MRAM cell array of this invention. Refer now to Fig. 4 and Fig. 3 for an explanation for a method of the programming of a logical "1" to a selected MRAM cell 305s. A method for writing a selected spin-torque MRAM cell 305s in an array of spin-torque MRAM cells 300 to a first level (logical "1") begins at time τ₀ by setting the data input signal DᵦW 314 to a ground reference voltage level (OV) as shown in the plot 400. An inverse data input signal ̅DᵦW (Not shown in Fig. 3) is set at time τ₀ to the voltage level of the power supply voltage source VDD as shown in plot 405. The first common source control signal 370a is set at the ground reference voltage level (OV) prior to the time τ₀ as shown in the plot 410 to keep the MOS transistor 366 turned off. The second common source control signal 370b transits from the voltage level of the power supply voltage source VDD to the at the time τ₀ to the ground reference voltage level (OV), as shown in the plot 415 to turn off the MOS transistor 368. The first bit line control signal 350a is set at the ground reference voltage level (OV) prior to the time τ₀ as shown in the plot 420 to keep the MOS transistor 341 of the bit line precharge circuits 340a, ..., 34On, and 340R turned off. The second bit line control signal 350b transits from the voltage level of the power supply voltage source VDD to the at the time τ₀ to the ground reference voltage level (OV) to turn off the MOS transistor 342 of the bit line precharge circuits 340a, ..., 34On, and 340R, as shown in the plot 425. In the plot
430, the local word line control voltage 345 is set to a high voltage level (V_{HV}) that is greater than the voltage level of the power supply voltage source VDD at the time \( \tau_0 \). This voltage level turns on all the high voltage pass transistor 326 of each of the gate voltage boosting circuits 325a, 325b, ..., 325m to connect the global word lines 315a, 315b, ..., 315m the local word lines 320a, 320b, ..., 320m. The selected global word line 315a is activated to transit from the ground reference voltage level (OV) to the voltage level of the power supply voltage source VDD at the time \( \tau_0 \) as shown in plot 435. With the high voltage pass transistor 326 of the gate voltage boosting circuit 325a turned on, the local word line 320a follows the voltage level of the global word line 315a, as shown in plot 440 at the time \( \tau_0 \). At the time \( \tau_0 \), the selected bit line 335n, the unselected bit lines 335a, 335b, ... the voltage at the junction of the MTJ element 307 of each of the MRAM cells 305, and the common source line 360 are set to the ground reference voltage level (OV) as shown respectively in plots 445, 450, 455, and 460.

[0051] At the time \( \tau_i \), the first common source control signal 370a transits from the ground reference voltage level (OV), as shown in the plot 410 to the voltage level of the power supply voltage source VDD to turn on the MOS transistor 366. The second common source control signal 370b remains, at the time \( \tau_i \), to the ground reference voltage level (OV), as shown in the plot 415 to keep the MOS transistor 368 turned off. This begins the transition of the common source line select circuit 365 from the ground reference voltage level (OV) to the voltage level V-i, as shown in plot 460. The voltage level V_i is equal to or less than the voltage level of the power supply voltage source VDD. Also, at the time \( \tau_i \), the bit line control signal 350a transits from the ground reference voltage level (OV) to the voltage level of the power supply voltage source VDD to turn on the MOS transistor 341 to connect the selected bit line 335n to the voltage source V_2 as shown in plot 420. The voltage level V_2 is equal to or less than the voltage level of the power supply voltage source VDD. The second bit line control signal 350b remains at the ground reference...
voltage level (OV) to keep the MOS transistors 342 of the bit line
precharge circuits 340a, ..., 340n, and 340R turned off, as shown in the
plot 425. All the unselected bit lines 335a, 335b, ... and the one selected
bit line 335n are being charged up towards voltage level V2. Since the
selected bit line 335n also has the column select transistor yn 375n
turned on, it only reaches a transient intermediate level as shown in plot
445. The unselected bit lines 335a, ... and the common source line 460
voltage levels rise towards voltage level V2, as shown in plots 455 and
460. As the voltage levels rise, the gates of MOS transistor 307 of each
of the MRAM cells 305 of the unselected MRAM cells 305 on the selected
local word line 320a serve as boost capacitors for the local word line
320a, so the local word line 320a voltage rises.

[0052] At a time just prior to the time τi, the local word line control voltage
345 transits from the high voltage level (VHV) to the ground reference
voltage level (OV) to turn off the high voltage pass transistor 326 of each
of the gate voltage boosting circuits 325a, 325b, ..., 325m, as shown in
plot 430. The voltage level of the selected local word line 320a is
boosted, as shown in plot 440, and thus the gate drive of each MOS
transistor 307 of each of the MRAM cells 305 to compensate the rise of
source voltage to ensure that the program current through the MTJ
element 306 of the selected MRAM cell 305s.

[0053] At the time τ2, the first bit line control signal 350a is set at the
ground reference voltage level (OV) as shown in the plot 420 to turn off
the MOS transistor 341 of the circuits 340a, ..., 340n, and 340R. The
selected bit line 335n returns to ground reference voltage level (OV) as
shown in the plot 445. Since the unselected bit lines 335a, 335b, ... are
essentially floating and their capacitances are charge to the voltage level
Vi, the unselected bit lines 335a, 335b, ... remain at the voltage level Vi.

[0054] At the time τ3, the data input signal D0w 314 is set to a tri-state high
impedance as shown in the plot 400. The inverse data input signal D0w
(Not shown in Fig. 3) is set at time τ3 to a tri-state high impedance as
shown in plot 405. The first common source control signal 370a is set at the ground reference voltage level (OV) prior to the time τ₃ as shown in the plot 410 to turn off the MOS transistor 366. The second common source control signal 370b transits to the voltage level of the power supply voltage source VDD at the time τ₃ to the ground reference voltage level (OV), as shown in the plot 415 to turn on the MOS transistor 368. The first bit line control signal 350a remains at the ground reference voltage level (OV) as shown in the plot 420 to keep the MOS transistor 341 of the bit line precharge circuits 340a, ..., 34On, and 340Ras turned off. The second bit line control signal 350b transits from the voltage level of the ground reference voltage level (OV) at the time τ₃ to the power supply voltage source VDD to turn on the MOS transistor 342 of the bit line precharge circuits 340a, ..., 34On, and 340Ras shown in the plot 425. In the plot 430, the local word line control voltage 345 is set to a high voltage level (Vᵢₜ minded) that is greater than the voltage level of the power supply voltage source VDD at the time τ₃. This voltage level turns on all the high voltage pass transistor 326 of each of the gate voltage boosting circuits 325a, 325b, ..., 325m to connect the global word lines 315a, 315b, ..., 315m the local word lines 320a, 320b, ..., 320m. The selected global word line 315a is deactivated to transit from the voltage level of the power supply voltage source VDD to the ground reference voltage level (OV) at the time τ₃ as shown in plot 435. With the high voltage pass transistor 326 of the gate voltage boosting circuit 325a turned on, the local word line 320a follows the voltage level of the global word line 315a, as shown in plot 440 at the time τ₃ and is essentially at the ground reference voltage level (OV).

The selected bit line 335n, the unselected bit lines 335a, 335b, ... the voltage at the junction of the MTJ element 306 and the source of each MOS transistor 307 of each of the MRAM cells 305, and the common source line 360 are set or transit to the ground reference voltage level (OV) as shown respectively in plots 445, 450, 455, and 460.

[0055] The programming of the logical "0" is similar to the programming for a selected spin-torque MRAM cell of the prior art. Fig. 5
is a timing diagram for programming a logical "0" to a selected spin-torque MRAM cell in a spin-torque MRAM cell array of this invention. Refer now to Fig. 5 and Fig. 3 for an explanation for a method of the programming of a logical "0" to a selected MRAM cell 305s. A method for writing a selected spin-torque MRAM cell 305s in an array of spin-torque MRAM cells 300 to a first level (logical "0") begins at time τ₀ by setting the data input signal D₂₅₀ 314 from a tri-state intermediate level to a desired logical "0" program voltage level as shown in the plot 500. An inverse data input signal $\overline{D}_{250}$ (Not shown in Fig. 3) is set at time τ₀ to the voltage level of the ground reference voltage level (OV) as shown in plot 505. The first common source control signal 370a is set at the ground reference voltage level (OV) prior to the time τ₀ as shown in the plot 510 to keep the MOS transistor 366 turned off. The second common source control signal 370b is set at the voltage level of the power supply voltage source VDD, as shown in the plot 515 to keep the MOS transistor 368 turned on. The first bit line control signal 350a is set at the ground reference voltage level (OV) prior to the time τ₀ as shown in the plot 520 to keep the MOS transistor 341 of the bit line precharge circuits 340a, ..., 340n, and 340R turned off. The second bit line control signal 350b transits from the voltage level of the power supply voltage source VDD to the at the time τ₀ to the ground reference voltage level (OV) to keep the MOS transistor 342 of the bit line precharge circuits 340a, ..., 340n, and 340R turned off, as shown in the plot 525. In the plot 530, the local word line control signal 345 is set to a high voltage level ($V_H$) that is greater than the voltage level of the power supply voltage source VDD at the time τ₀. This voltage level turns on all the high voltage pass transistor 326 of each of the gate voltage boosting circuits 325a, 325b, ..., 325m to connect the global word lines 315a, 315b, ..., 315m the local word lines 320a, 320b, ..., 320m. The selected global word line 315a is activated to transit from the ground reference voltage level (OV) to the voltage level of the power supply voltage source VDD at the time τ₀ as shown in plot 535. With the high voltage pass transistor 326 of the gate voltage boosting circuit 325a turned on, the local word line 320a follows the voltage level of the global
word line 315a, as shown in plot 540 at the time τ₀. Since the selected bit line 335n also has the column select transistor yn 375n turned on, the read/write row decoder drivers 312 drives the selected bit line 335n to transit at the time τ₀, from the ground reference voltage level (OV) to approach the voltage level of the desired logical "0" program voltage level as shown in plot 545. Also at the time τ₀, the unselected bit lines 335a, 335b, ..., 335m, the voltage at the junction of the MTJ element 306 and the source of each MOS transistor 307 of each of the MRAM cells 305, and the common source line 360 are set to the ground reference voltage level (OV) as shown respectively in plots 550, 555, and 560.

[0056] At completion of the writing of the logical "0" to the selected MRAM cell 305s at the time τ₂, the data input signal D₀w 314 and inverse data input signal D₀w (Not shown in Fig. 3) are set to a tri-state high impedance as shown in the plot 500 and plot 505. The first common source control signal 370a remains set at the ground reference voltage level (OV) prior to the time τ₂ as shown in the plot 510 to turn off the MOS transistor 366. The second common source control signal 370b remains set to the voltage level of the power supply voltage source VDD, as shown in the plot 515 to keep the MOS transistor 368 turned on. The first bit line control signal 350a remains at the ground reference voltage level (OV) as shown in the plot 520 to keep the MOS transistor 341 of the bit line precharge circuits 340a, ..., 340n, and 340R turned off. The second bit line control signal 350b transits from the voltage level of the power supply voltage source VDD to the ground reference voltage level (OV) at the time τ₂ to turn off the MOS transistor 342 of the bit line precharge circuits 340a, ..., 340n, and 340Ras shown in the plot 525. In the plot 530, the local word line control voltage 345 remains set to a high voltage level (VₚV) that is greater than the voltage level of the power supply voltage source VDD at the time τ₂. This voltage level keeps all the high voltage pass transistors 326 of each of the gate voltage boosting circuits 325a, 325b, ..., 325m turned on to connect the global word lines 315a, 315b, ..., 315m the local word lines 320a, 320b, ..., 320m. The selected
global word line 315a is deactivated to transit from the voltage level of the power supply voltage source VDD to the ground reference voltage level (OV) at the time \( \tau_2 \) as shown in plot 535. With the high voltage pass transistor 326 of the gate voltage boosting circuit 325a turned on, the local word line 320a follows the voltage level of the global word line 315a, as shown in plot 540 at the time \( \tau_2 \) and is essentially at the ground reference voltage level (OV). Since the selected bit line 335n has the column select transistor \( y_n \) 375n turned off and the second bit line control signal 350b has turned on the MOS transistor 342 of the bit line precharge circuits 340a, ..., 34On, and 320R to cause the selected bit line 335n to transit to the ground reference voltage level (OV), as shown in the plot 545. The unselected bit lines 335a, 335b, ..., the voltage at the junction of the MTJ element 306, and the source of each MOS transistor 307 of each of the MRAM cells 305, and the common source line 360 are set or transit to the ground reference voltage level (OV) as shown respectively in plots 550, 555, and 560.

[0057] Refer now to Fig. 6 for a discussion of an embodiment of a spin-torque magnetic random access memory device. Each array of MRAM cells as described in Fig. 1 are formed into groups of arrays (Fig. 3 illustrating a single group) to construct a spin-torque MRAM device. Groups of the MRAM cell arrays 605 are organized into groups of arrays 600. The precharge circuit 610 is connected to each of the MRAM cell arrays 605 to precharge the appropriate bit lines of the MRAM cell arrays 605 dependent upon the state of the data signal 655 being written to the MRAM cell arrays 605. The column select circuit 650 provides the column select signal \( y_i \) 652a and \( y_2 \) 652b to activate the gating MOS transistors 375a, ..., 375n, and 375R of Fig. 3 for a selected column of the MRAM cell arrays 605. The bit line decode circuit 680 is connected to each of the groups of arrays 600 to for selecting the columns of the MRAM cell arrays 605 based on decoding the address 630.

[0058] A word line decode circuit 615 is connected to each of the global word lines 665 of each of the MRAM cell arrays 605. The global word
lines 665 are each connected to associated the local word lines 320a, 320b, ..., 320m of Fig. 3 as described above to receive a word line select signal through the gate voltage boosting circuit 325a, 325b, ..., 325m from associated global word line 665. The word line decode circuit 615 receives the address signal 630 defining which row of which of the MRAM cell arrays 605 is to be written to or read from. The common source select line decode circuit 620 is connected to source select lines 660 of all of the MRAM cell arrays 605 to provide the source select signal for writing and reading the selected MRAM cells of the MRAM cell arrays 605. The common source select line decode circuit 620 receives the address signal 630 and the read/write signal 635 and determines which of the MRAM cells is to be read or written.

The bipolar write/read generator 625 receive the data input signal 645 and a clock timing signal 640. With the read/write signal 635 and the address signal 630 provides the necessary biasing and control signals to the precharge circuit 610, the column select circuit 650, the bit line decode circuit 680, and the common source select line decode circuit 620 for reading data from and writing data to the MRAM cells of the MRAM cell arrays 605. During a read operation, the sense amplifier 670 receives the data sense signals from the selected MRAM cells, amplifies, and conditions the data sense signals to generate the output data signals 675 for transfer external circuitry.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

The invention claimed is:
1. A spin-torque MRAM cell array comprising:
   a plurality of spin-torque MRAM cells arranged in rows and columns, each spin-torque MRAM cell comprising:
   a magnetic tunnel junction element, and
   a select switching device having a drain terminal connected to a first terminal of the magnetic tunnel junction element;
   a plurality of local word lines, each local word line associated with one row of the plurality of spin-torque MRAM cells and connected to a gate terminal of the select switching device of each spin-torque MRAM cell on each row to control activation and deactivation of the select switching device; and
   a plurality of gate voltage boosting circuits, each gate voltage boosting circuit placed between an associated global word line of a plurality of global word lines and an associated local word line of the plurality of local word lines to boost a local word line voltage applied to a gate of the selected switching device during writing of a first level to the magnetic tunnel junction element of a selected spin-torque MRAM cell when activated by a local word line control signal.

2. The spin-torque MRAM cell array of claim 1 wherein each of the plurality of gate voltage boosting circuits comprises:
   a high voltage switching transistor having a drain terminal connected to the global word line associated with the gate voltage boosting circuit, a source connected to the gate of the gate of the select switching device and a gate connected to receive the local word line control signal to activate and deactivate the high voltage switch transistor for boosting the local word line voltage.
3. The spin-torque MRAM cell array of claim 2 wherein each of the plurality of gate voltage boosting circuits further comprises a clamping device to prevent an over boost condition.

4. The spin-torque MRAM cell array of claim 1 further comprising a plurality of bit lines, each bit line associated with one column of the columns of the plurality of spin-torque MRAM cells and connected to a second terminal of the magnetic tunnel junction element.

5. The spin-torque MRAM cell array of claim 1 further comprising a common source line connected to a source of each of the select switching devices of the plurality of spin-torque MRAM cells provide a source or sink for a write current for programming the spin-torque MRAM cell.

6. The spin-torque MRAM cell array of claim 5 further comprising a common source select circuit connected to the common source line for selecting the source or sink for the write current.

7. The spin-torque MRAM cell array of claim 6 wherein the common source line select circuit comprises;

   a first transistor having a drain terminal connected to a first voltage source and a source terminal connected to the common source line; and

   a second transistor having a drain terminal connected to the common source line and a source terminal connected to a ground reference point;

   wherein common source line control signals are connected to gates of the first and second transistors to turn on and turn off the first and second transistors to provide a source or sink for the write current through the selected spin-torque MRAM cell during a program operation.
8. The spin-torque MRAM cell array of claim 1 further comprising a plurality of bit line precharge circuits, each bit line precharge circuit associated with one column of the plurality of spin-torque MRAM cells for precharging the associated bit line dependent upon a datum to be written.

9. The spin-torque MRAM cell array of claim 8 wherein each of the plurality of bit line precharge circuits comprises:

   a third transistor having a drain terminal connected to a first voltage source and a source terminal connected to the associated bit line; and

   a fourth transistor having a drain terminal connected to the associated bit line and a source terminal connected to a ground reference point;

wherein bit line control signals are connected to gates of the third and fourth transistors to turn on and turn off the third and fourth transistors to control directionality of the write current flow through a selected spin-torque MRAM cell during a program operation.

10. The spin-torque MRAM cell array of claim 1 wherein a selected spin-torque MRAM cell is written to the first level during a first writing step by:

    activating the global word line associated with the selected spin-torque MRAM cell at a first time;

    activating the local word line control signal to effectively connect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell at the first time;

    applying a data input signal as the first level to a bit line associated with the selected spin-torque MRAM cell to generate a current
to program the magnetic tunnel junction element of the selected spin-torque MRAM cell to the first level at the first time; and
deactivating the local word line control signal to effectively disconnect the global word line associated with the selected spin-torque MRAM cell and the local word line associated with the selected spin-torque MRAM cell at a second time to float the local word line associated with the selected spin-torque MRAM cell for boosting the associated local word line to a higher voltage level to compensate for a rise of a voltage at a source of the select switching device of the selected spin-torque MRAM cell;

11. A spin-torque magnetic random access memory device comprising

a plurality of spin-torque MRAM cell arrays arranged in a plurality of groups, each spin-torque MRAM array comprising:

a plurality of spin-torque MRAM cells arranged in rows and columns, each spin-torque MRAM cell comprising:

a magnetic tunnel junction element, and

a select switching device having a drain terminal connected to a first terminal of the magnetic tunnel junction element;

a plurality of local word lines, each local word line associated with one row of the plurality of spin-torque MRAM cells and connected to a gate terminal of the select switching device of each spin-torque MRAM cell on each row to control activation and deactivation of the select switching device; and

a plurality of gate voltage boosting circuits, each gate voltage boosting circuit placed between an associated global word
The spin-torque magnetic random access memory device of claim 11
wherein each of the plurality of gate voltage boosting circuits comprises:

- a high voltage switching transistor having a drain terminal
  connected to the global word line associated with the gate
  voltage boosting circuit, a source connected to the gate of the
  gate of the select switching device and a gate connected to
  receive the local word line control signal to activate and
deactivate the high voltage switch transistor for boosting the
local word line voltage.

The spin-torque magnetic random access memory device of claim 12
wherein each of the plurality of gate voltage boosting circuits further
comprises a clamping device to prevent an over boost condition.

The spin-torque magnetic random access memory device of claim 11
wherein the spin-torque MRAM cell array further comprises a plurality of
bit lines, each bit line associated with one column of the columns of the
plurality of spin-torque MRAM cells and connected to a second terminal of
the magnetic tunnel junction element.

The spin-torque magnetic random access memory device of claim 11
further comprising a common source line connected to a source of each
of the select switching devices of the plurality of spin-torque MRAM cells
provide a source or sink for a write current for programming the spin-
torque MRAM cell.

line of a plurality of global word lines and an associated local
word line of the plurality of global word lines to boost a local
word line voltage applied to a gate of the selected switching
device during writing of a first level to the magnetic tunnel
junction element of a selected spin-torque MRAM cell when
activated by a local word line control signal;
16. The spin-torque magnetic random access memory device of claim 15 wherein the spin-torque MRAM cell array further comprises a common source select circuit connected to the common source line for selecting the source or sink for the write current.

17. The spin-torque magnetic random access memory device of claim 16 wherein the common source line select circuit comprises:

   a first transistor having a drain terminal connected to a first voltage source and a source terminal connected to the common source line; and

   a second transistor having a drain terminal connected to the common source line and a source terminal connected to a ground reference point;

   wherein common source line control signals are connected to gates of the first and second transistors to turn on and turn off the first and second transistors to provide a source or sink for the write current through the selected spin-torque MRAM cell during a program operation.

18. The spin-torque magnetic random access memory device of claim 11 wherein the spin-torque MRAM cell array further comprises a plurality of bit line precharge circuits, each bit line precharge circuit associated with one column of the plurality of spin-torque MRAM cells.

19. The spin-torque magnetic random access memory device of claim 18 wherein each of the plurality of bit line precharge circuits comprises:

   a third transistor having a drain terminal connected to a first voltage source and a source terminal connected to the associated bit line; and
a fourth transistor having a drain terminal connected to the
associated bit line and a source terminal connected to a ground
reference point;

wherein bit line control signals are connected to gates of the third
and fourth transistors to turn on and turn off the third and fourth
transistors to control directionality of the write current flow
through a selected spin-torque MRAM cell during a program
operation.

20. The spin-torque magnetic random access memory device of claim 11
wherein a selected spin-torque MRAM cell is written to the first level
during a first writing step by:

activating the global word line associated with the selected spin-
torque MRAM cell at a first time;

activating the local word line control signal to effectively connect
the global word line associated with the selected spin-torque
MRAM cell and the local word line associated with the selected
spin-torque MRAM cell at the first time;

applying a data input signal as the first level to a bit line associated
with the selected spin-torque MRAM cell to generate a current
to program the magnetic tunnel junction element of the selected
spin-torque MRAM cell to the first level at the first time; and

deactivating the local word line control signal to effectively
disconnect the global word line associated with the selected
spin-torque MRAM cell and the local word line associated with
the selected spin-torque MRAM cell at a second time to float
the local word line associated with the selected spin-torque
MRAM cell for boosting the associated local word line to a
higher voltage level to compensate for a rise of a voltage at a
source of the select switching device of the selected spin-torque
MRAM cell;

21. A method for writing a selected spin-torque MRAM cell in an array of spin-
torque MRAM cells to a first level comprising the steps of:

providing a plurality of spin-torque MRAM cells arranged in rows
and columns, each spin-torque MRAM cell comprising:

a magnetic tunnel junction element, and

a select switching device having a drain terminal connected
to a first terminal of the magnetic tunnel junction

providing a plurality of local word lines, each local word line
associated with one row of the plurality of spin-torque MRAM
cells and connected to a gate terminal of the select switching
device of each spin-torque MRAM cell on each row to control
activation and deactivation of the select switching device; and

providing a plurality of gate voltage boosting circuits, each gate
voltage boosting circuit placed between an associated global
word line of a plurality of global word lines and an associated
local word line of the plurality of local word lines to boost a local
word line voltage applied to a gate of the selected switching
device during writing of a first level to the magnetic tunnel
junction element of a selected spin-torque MRAM cell when
activated by a local word line control signal;

activating the global word line associated with the selected spin-
torque MRAM cell at a first time;

activating the local word line control signal to effectively connect
the global word line associated with the selected spin-torque
MRAM cell and the local word line associated with the selected
spin-torque MRAM cell at the first time;

applying a data input signal as the first level to a bit line associated
with the selected spin-torque MRAM cell to generate a current
to program the magnetic tunnel junction element of the selected
spin-torque MRAM cell to the first level at the first time; and

deactivating the local word line control signal to effectively
disconnect the global word line associated with the selected
spin-torque MRAM cell and the local word line associated with
the selected spin-torque MRAM cell at a second time to float
the local word line associated with the selected spin-torque
MRAM cell for boosting the associated local word line to a
higher voltage level to compensate for a rise of a voltage at a
source of the select switching device of the selected spin-torque
MRAM cell;

22. A method for forming a spin-torque MRAM cell array comprising the steps
of:

forming a plurality of spin-torque MRAM cells arranged in rows and
columns, wherein forming each spin-torque MRAM cell
comprises the steps of:

forming a magnetic tunnel junction element, and

forming a select switching device having a drain terminal
connected to a first terminal of the magnetic tunnel junction
element;

forming a plurality of local word lines, wherein forming each local
word line comprises the steps of

associating each local word line with one row of the plurality of
spin-torque MRAM cells, and

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connecting each word line to a gate terminal of the select
switching device of each spin-torque MRAM cell on its
associated row to control activation and deactivation of the
select switching device; and

forming a plurality of gate voltage boosting circuits, wherein
forming each gate voltage boosting circuit comprises the steps
of:

placing each gate voltage boosting circuit between an
associated global word line of a plurality of global word lines
and an associated local word line of the plurality of local
word lines to boost a local word line voltage applied to a
gate of the selected switching device during writing of a first
level to the magnetic tunnel junction element of a selected
spin-torque MRAM cell when activated by a local word line
control signal.

23. The method for forming a spin-torque MRAM cell array of claim 22
wherein forming each of the plurality of gate voltage boosting circuits
comprises the steps of:

forming a high voltage switching transistor;

connecting a drain terminal of the high voltage switching transistor
to the global word line associated with the gate voltage boosting
circuit;

connecting a source terminal of the high voltage switching
transistor to the gate of the select switching device; and

connecting a gate of the high voltage switching transistor to receive
the local word line control signal to activate and deactivate the
high voltage switch transistor for boosting the local word line
voltage.
24. The method for forming a spin-torque MRAM cell array of claim 23 wherein forming each of the plurality of gate voltage boosting circuits further comprises the steps of:

- forming a clamping device to prevent an over boost condition;
- connecting a first terminal of the clamping device to the source of the high voltage switching transistor and the associated word line; and
- connecting a second terminal of the clamping device to the ground reference point.

25. The method for forming a spin-torque MRAM cell array of claim 22 further comprising the step of forming a plurality of bit lines, wherein forming each bit line comprises the steps of:

- associating each bit line with one column of the columns of the plurality of spin-torque MRAM cells; and
- connecting each bit line to a second terminal of the magnetic tunnel junction element.

26. The method for forming a spin-torque MRAM cell array of claim 22 further comprising the steps of:

- forming a common source line; and
- connecting the common source line to a source of each of the select switching devices of the plurality of spin-torque MRAM cells to provide a source or sink for a write current for programming the spin-torque MRAM cell.

27. The method for forming a spin-torque MRAM cell array of claim 26 further comprising the steps of:

- forming a common source select circuit; and
28. The method for forming a spin-torque MRAM cell array of claim 27 wherein forming the common source line select circuit comprises steps of:

- forming a first transistor having a drain terminal connected to a first voltage source and a source terminal connected to the common source line;
- forming a second transistor having a drain terminal connected to the common source line and a source terminal connected to a ground reference point; and
- connecting common source line control signals to gates of the first and second transistors to turn on and turn off the first and second transistors to provide a source or sink for the write current through the selected spin-torque MRAM cell during a program operation.

29. The method for forming a spin-torque MRAM cell array of claim 22 further comprising the steps of:

- forming a plurality of bit line precharge circuits; and
- connecting each bit line precharge circuit with one column of the plurality of spin-torque MRAM cells.

30. The method for forming a spin-torque MRAM cell array of claim 29 wherein forming each of the plurality of bit line precharge circuits comprises the steps of:

- forming a third transistor having a drain terminal connected to a first voltage source and a source terminal connected to an associated bit line;
forming a fourth transistor having a drain terminal connected to the
associated bit line and a source terminal connected to a ground
reference point; and

connecting the bit line control signals to gates of the third and
fourth transistors to turn on and turn off the third and fourth
transistors to control directionality of the write current flow
through a selected spin-torque MRAM cell during a program
operation.
FIG. 2 - Prior Art
FIG. 3
FIG. 4
INTERNATIONAL SEARCH REPORT

A CLASSIFICATION OF SUBJECT MATTER

IPC G11C 11/14 (2006 01),7/00( 2006 01),HOIS 4/00( 2006 01)

USPC 365/1 71,189,203. 189 16,029/592 1

According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

US 365/171.1 89,203,1 89 16,48,029/5921

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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Continuation of B. FIELDS SEARCHED Item 3:
Search Text US-PGPUB, USPAT, USOCR, EPO, JPO, DERWENT
Search Terms spin near torque, MRAN magnet, common, source, circuit, transistor, clamp, diode