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(54) Title: MULTI-LAYER CHIP CARRIER AND PROCESS FOR MAKING

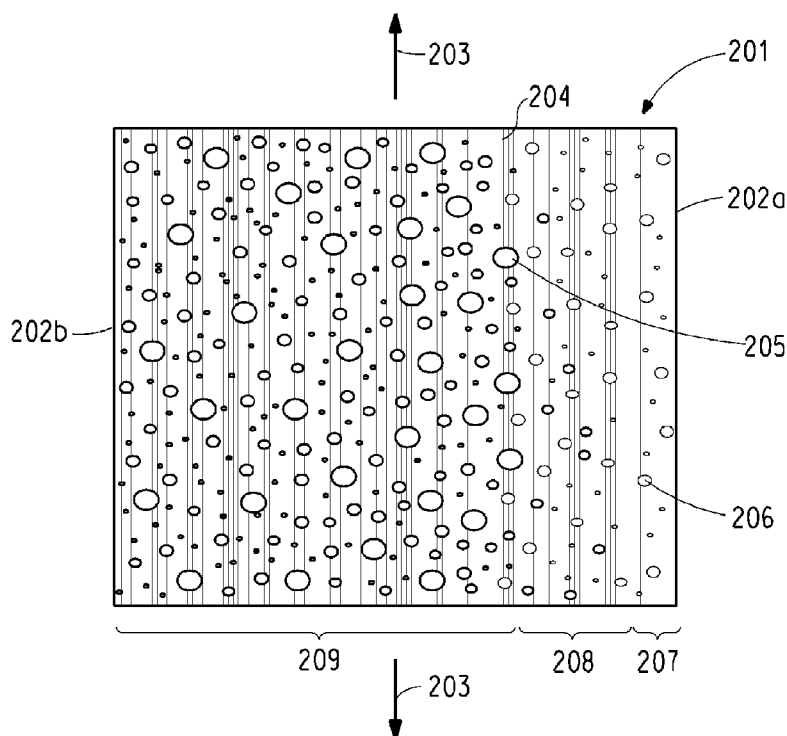


FIG. 2

(57) Abstract: Provided, are multi-layer chip carriers comprising an asymmetric cross-linked polymeric dielectric film, and processes for making the chip carriers.

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European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/204733 A1 (MURAI MAKOTO [JP] ET AL) 14 September 2006 (2006-09-14) paragraphs [0046] - [0048], [0054], [0061], [0067]; figures 2,3	1-11
X	DE 101 61 101 A1 (INFINEON TECHNOLOGIES AG [DE]) 13 March 2003 (2003-03-13) paragraphs [0041], [0042]; figure 1	1-11
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A	US 5 834 101 A (HAYASHI SATORU [JP]) 10 November 1998 (1998-11-10) figures 2-4	5

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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