(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 February 2022 (10.02.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/029501 A1

(51) International Patent Classification:
H01L 31/101 (2006.01) *G01J 1/44* (2006.01)

(21) International Application Number:
PCT/IB2021/000575

(22) International Filing Date:
06 August 2021 (06.08.2021)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/060,187 03 August 2020 (03.08.2020) US
17/347,822 15 June 2021 (15.06.2021) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 17/347,822 (CON)
Filed on 15 June 2021 (15.06.2021)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P. O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(72) Inventors: **SCHUPPENER, Gerd**; 703 Beaumont Drive, Allen, TX 75013 (US). **ALIROTEH, Miaad**; 1933 Grand Teton Dr., Milpitas, CA 95035 (US). **RAMASWAMY, Srinath**; 624 Sundown Way, Murphy, TX 75094 (US). **HAROUN, Baher**; 906 Pampa Drive, Allen, TX 75013 (US).

(74) Agent: **ABRAHAM, Ebby** et al.; Texas Instruments Incorporated, P. O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN,

(54) Title: AVALANCHE PHOTODIODE GAIN CONTROL

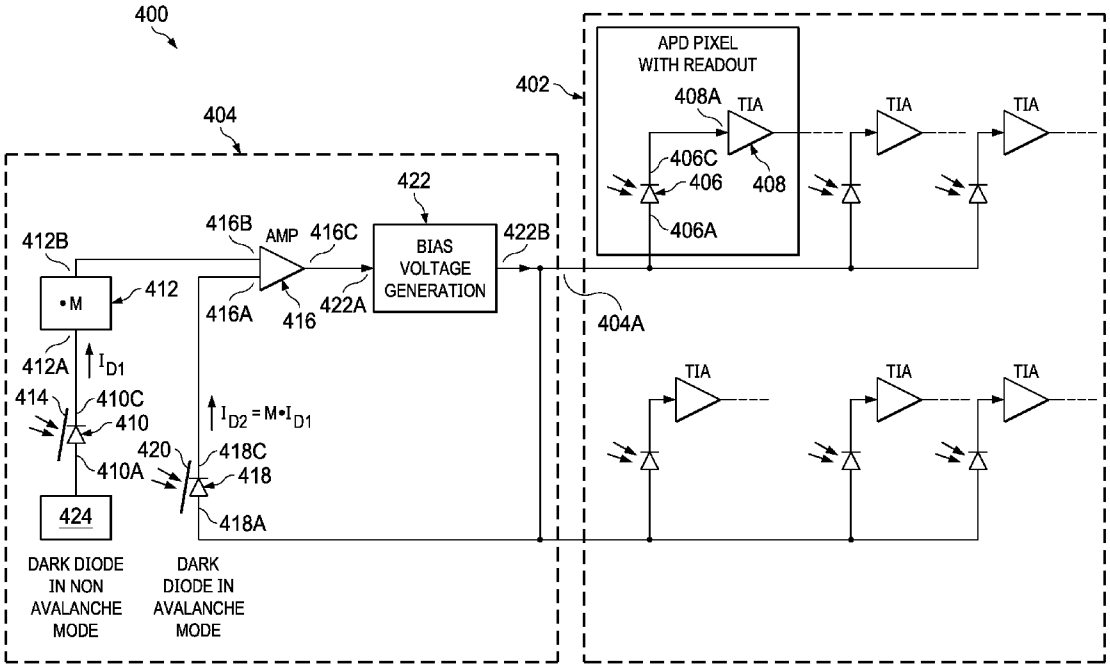


FIG. 4

(57) Abstract: An avalanche photo-diode (APD) circuit includes a first APD (406) and a bias circuit (404). The first APD (406) is configured to detect light. The bias circuit (404) is configured to control a gain of the first APD (406). The bias circuit (404) includes a second APD (410), a reference voltage source (424), a bias voltage generation circuit (422), and a metal layer (414) configured to shield the second APD (410) from the light. The reference voltage source is configured to bias the second APD (410). The bias voltage generation circuit (422) is configured to generate a bias voltage for biasing the first APD (406) based on dark current output by the second APD (410).

WO 2022/029501 A1

[Continued on next page]

KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

— *with information concerning request for restoration of the right of priority in respect of one or more priority claims; the decision of the receiving Office regarding the request for restoration is pending and will be published separately once available (Rules 26bis.3 and 48.2(j))*

AVALANCHE PHOTODIODE GAIN CONTROL

BACKGROUND

[0001] Photodiodes are semiconductor devices that generate an electrical current when illuminated. Photodiodes are used as light-detection elements in a variety of applications. A photodiode includes a p-n junction formed in a semiconductor material. A reverse bias is applied to the p-n junction to widen the depletion layer, and an electric field is applied. Electron-hole pairs are generated in the depletion layer by the absorbed light. Under the attraction of the electric field, electrons move to the n-type semiconductor region, while holes move to the p-type semiconductor region, thereby causing a current to flow. Types of photodiodes include PIN photodiodes and avalanche photodiodes.

SUMMARY

[0002] In one example, an avalanche photo-diode (APD) circuit includes a first APD, a reference voltage source, and a bias circuit. The first APD includes an anode. The bias circuit includes a bias output, a second APD, and a layer of metal that covers the second APD. The bias output is coupled to the anode of the first APD. The second APD includes a cathode and an anode. The cathode of the second APD is coupled to the bias output. The anode of the second APD is coupled to the reference voltage source.

[0003] In another example, an APD circuit includes a first APD and a bias circuit. The first APD is configured to detect light. The bias circuit is configured to control a gain of the first APD. The bias circuit includes a second APD, a reference voltage source, a bias voltage generation circuit, and a metal layer configured to shield the second APD from the light. The reference voltage source is configured to bias the second APD. The bias voltage generation circuit is configured to generate a bias voltage for biasing the first APD based on dark current output by the second APD.

[0004] In a further example, a light detection circuit includes an APD array and a bias circuit. The APD array is configured to detect light, and includes a first APD, and a transimpedance amplifier. The transimpedance amplifier is coupled to first APD. The bias circuit is coupled to the APD array, and is configured to control a gain of the first APD. The bias circuit includes a second APD, a reference voltage source, a current multiplier circuit, a bias voltage generation circuit, and a metal

layer that is configured to shield the second APD from the light. The reference voltage source is configured to bias the second APD. The current multiplier circuit is coupled to the second APD, and is configured to provide an output current that is a predetermined multiple of the dark current output by the second APD. The bias voltage generation circuit is configured to generate a bias voltage for biasing the first APD based on the output current of the current multiplier circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1A is a schematic diagram of a positive-intrinsic-negative (PIN) photodiode.

[0006] FIG. 1B is a graph of the electric field distribution in the reverse biased PIN photodiode of FIG. 1A.

[0007] FIG. 2A is a schematic diagram of an avalanche photodiode (APD).

[0008] FIG. 2B is a graph of the electric field distribution in the various layers of the reverse biased APD of FIG. 2A.

[0009] FIG. 3A is a graph of dark current in an APD.

[0010] FIG. 3B is a graph of photocurrent in an APD.

[0011] FIG. 3C is a graph of avalanche gain in an APD.

[0012] FIG. 4 is a block diagram of an example APD circuit that uses dark current to bias an APD.

[0013] FIG. 5 is a schematic diagram for an example bias voltage generation circuit suitable for use in the APD circuit of FIG. 4.

[0014] FIG. 6 is a block diagram of an example second APD circuit that uses dark current to bias an APD.

[0015] FIG. 7 is a block diagram of an example third APD circuit that uses dark current to bias an APD.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0016] In a photodiode, photocurrent (I_p) is proportional to the incident optical power (P_{in}). Responsivity is the ratio of photocurrent generated from incident light, to the incident light, and may be expressed as current over power.

$$R = \frac{I_p}{P_{in}}$$

where:

I_p is in units of amperes (A); and

P_{in} is in units of watts (W).

[0017] The quantum efficiency of the photodiode may be defined as:

$$\eta = \frac{electron\ generation\ rate}{photon\ incidence\ rate} = \frac{I_p/q}{P_{in}/hv}$$

[0018] Responsivity may be expressed based on quantum efficiency as:

$$R = \frac{\eta q}{hv} \approx \frac{\eta \lambda}{1.24}$$

[0019] Positive-intrinsic-negative (PIN) photodiodes and avalanche photodiodes (APD) are commonly used to detect light. FIG. 1A is a schematic diagram of a PIN photodiode. FIG. 1B is a graph of the electric field distribution in the reverse biased PIN photodiode. The PIN photodiode includes an intrinsic (or lightly doped) region sandwiched between a p-type region and an n-type region. The intrinsic region increases depletion region width, where photo-generated carriers (electrons and holes) travel by drift, rather than by diffusion as in the p-type and n-type regions. The depletion region creates capacitance that is inversely proportional to the width of the depletion region. Because response time of the photodiode is a function of the capacitance, increasing depletion region width decreases response time. PIN photodiodes are reverse biased well below the breakdown voltage. Table 1 lists various characteristics of typical PIN photodiodes.

Parameter	Symbol	Unit	Si	Ge	InGaAs
Wavelength	λ	μm	0.4-1.1	0.8-1.8	1.0-1.7
Responsivity	R	A/W	0.4-0.6	0.5-0.7	0.6-0.9
Quantum Efficiency	η	%	75-90	50-55	60-70
Dark current	I_d	nA	1-10	50-500	1-20
Rise time	T_r	ns	0.5-1	0.1-0.5	0.02-0.5
Bandwidth	Δf	GHz	0.3-0.6	0.5-3	1-10
Bias Voltage	V_b	V	10-100	6-10	3-6

Table 1

[0020] FIG. 2A is a schematic diagram of an APD. FIG. 2B is a graph of the electric field distribution in the various layers of the reverse biased APD. The APD is similar to the PIN photodiode, and includes an additional p-type region that operates as a multiplication layer. Secondary carriers are generated in the multiplication layer via impact ionization. The responsivity of the APD is expressed as:

$$R_{APD} = MR$$

where:

M is the multiplication factor provided by addition of the multiplication layer; and

R is responsivity of the photodetector without the multiplication layer.

[0021] The multiplication factor M may be expressed as:

$$M = \frac{1 - kA}{\exp\left[-(1 - kA)\alpha_e d\right] - kA}$$

where:

α_h is a hole impact ionization constant;

α_e is an electron impact ionization constant;

d is thickness of the multiplication layer; and

$$kA = \frac{\alpha_h}{\alpha_e}$$

[0022] The APD is reverse biased at a higher voltage than the PIN photodiode to enable impact ionization ($M>>1$). With low reverse bias voltage, the APD behaves like a PIN photodiode ($M=1$). Table 2 lists characteristics of typical APDs.

Parameter	Symbol	Unit	Si	Ge	InGaAs
Wavelength	λ	μm	0.4-1.1	0.8-1.8	1.0-1.7
Responsivity	R_{APD}	A/W	80-130	3-30	5-20
APD gain	M		100-500	50-200	10-40
k-factor	k_A		0.02-0.05	0.7-1.0	0.5-0.7
Dark current	I_d	nA	0.1-1	50-500	1-5
Rise time	T_r	ns	0.1-2	0.5-0.8	0.1-0.5
Bandwidth	Δf	GHz	0.2-.1	0.4-0.7	1-10
Bias Voltage	V_b	V	30-300	20-40	20-30

Table 2

[0023] APD gain is dependent on temperature and reverse bias voltage. Gain should be controlled to meet system performance metrics, such as sensitivity, signal-to-noise ratio, linearity, etc. In an array of APDs, the different APDs may receive different incident optical power, and control of the APD gain should be independent of incident light. The effects of ambient or stray

light should be compensated.

[0024] FIGS. 3A, 3B, and 3C are graphs of dark current, photocurrent, and avalanche gain in an APD respectively. Dark current is the small current flowing in an APD when no light is incident on the APD. FIG. 3A shows that for a dark APD avalanche breakdown is dependent on temperature, with higher temperature requiring a higher reverse bias voltage. The slope in the breakdown region is steep. FIG. 3B shows that photocurrent behavior of the APD is similar to the dark current behavior of the APD (e.g., higher temperature requiring higher reverse bias voltage). FIG. 3C shows that for different temperatures the reverse bias voltage must be adjusted to maintain a desired gain. The APD bias control circuits described herein take advantage of this similarity in dark current and photocurrent behavior, and apply dark current to bias the APD and control the gain thereof.

[0025] FIG. 4 is a block diagram of an APD circuit 400 that uses dark current to bias an APD. The APD circuit 400 may be a light detection circuit, a light detection and ranging (LIDAR) receiver circuit, or other optical transduction circuit. The APD circuit 400 includes an APD array 402 and a bias circuit 404. The APD array 402 may include one or more APDs. Some implementations of the APD array 402 may include hundreds or thousands of APDs. The APD array 402 includes an APD 406 and a transimpedance amplifier (TIA) 408. The APD 406 and the TIA 408 are coupled to form pixel circuitry of the APD array 402. The APD 406, and other APDs of the APD array 402, may be fabricated in silicon, germanium, silicon-germanium, or other semiconductor materials. The APD 406 is exposed to and detects incident light, and produces a photocurrent that is proportional to the incident light. The TIA 408 converts the photocurrent to voltage. An input 408A of the TIA 408 is coupled to the cathode 406C of the APD 406. The anode 406A of the APD 406 is coupled to the bias circuit 404 for receipt of a bias voltage that controls the gain of the APD 406. In practice, the anode of each APD of the APD array 402 is coupled to the bias circuit 404 for receipt of the bias voltage.

[0026] The bias circuit 404 generates the bias voltage based on dark current, and is therefore insensitive to ambient light and differences in optical power across the APD array 402. The bias circuit 404 includes a bias output 404A, an APD 410, a current multiplier circuit 412, an amplifier 416, an APD 418, a bias voltage generation circuit 422, and a reference voltage source 424. The bias output 404A is coupled to the anode 406A of the APD 406. The APD 410 and the APD 418 may be instances of the APD 406. The APD 410 and the APD 418 may be located near the APD array 402 (on an integrated circuit) for process and temperature tracking. A layer of metal 414 (or

other opaque material) covers the APD 410, and a layer of metal 420 (or other opaque material) covers the APD 418. For example, the metal 414 and the metal 420 may be same metal layer of an integrated circuit that isolates the APD 410 and APD 418 from light. Thus, the APD 410 and the APD 418 generate dark current and do not generate photocurrent.

[0027] An anode 410A of the APD 410 is coupled to the reference voltage source 424. The reference voltage source 424 provides a bias voltage that biases the APD 410 for non-avalanche operation. The bias voltage applied to the APD 410 may relatively low (e.g., 0 to -20 volts). The dark current (I_{D1}) generated by the APD 410 is multiplied by a predetermined multiplier value in the current multiplier circuit 412. The predetermined multiplier value is determined based on the desired gain of the APD 406. For example, the predetermined multiplier value may be in a range of 10-500. A cathode 410C of the APD 410 is coupled to an input 412A of the current multiplier circuit 412. The current multiplier circuit 412 may be implemented as a current mirror circuit to provide the desired multiplication of the dark current received from the current multiplier circuit 412. The multiplied dark current (MI_{D1}) produced by the current multiplier circuit 412 is provided to the amplifier 416. An input 416B of the amplifier 416 is coupled to the output 412B of the current multiplier circuit 412.

[0028] The anode 418A of the APD 418 is coupled to the bias output 404A. Thus, the same bias voltage is applied to the APD 418 and the APD 406, to bias the APD 418 and the APD 406 for avalanche mode operation. The dark current (I_{D2}) generated by the APD 418 is provided to the amplifier 416. A cathode 418C of the APD 418 is coupled to the input 416A of the amplifier 416.

[0029] The amplifier 416 compares the dark currents generated by the APD 410 and the APD 418 to produce a difference voltage (the difference of the two currents (MI_{D1} and I_{D2}). The difference voltage output by the amplifier 416 is provided to the bias voltage generation circuit 422.

[0030] The bias voltage generation circuit 422 applies the difference voltage received from the amplifier 416 to generate the bias voltage applied to the APD 406 and the APD 418. An input 422A of the bias voltage generation circuit 422 is coupled to an output 416C of the amplifier 416. The bias voltage generated by the bias voltage generation circuit 422 biases the APD 418 to produce dark current I_{D2}, where $I_{D2}=MI_{D1}$. If $I_{D2}<MI_{D1}$, the APD reverse bias is increased. If $I_{D2}>MI_{D1}$, the APD reverse bias is decreased. If $I_{D2}=MI_{D1}$, the APD reverse bias is not changed. Thus, the bias voltage applied to the APD 406, and other APDs of the APD array 402, is based on the dark current output by the APD 410 and the APD 418 as function of temperature and process.

[0031] FIG. 5 is a schematic diagram for an example bias voltage generation circuit 422. The amplifier 416 is also shown in FIG. 5 for reference. The bias voltage generation circuit 422 includes a transistor 502 and a capacitor 504. The transistor 502 may be a p-type field effect transistor (FET). A gate 502G of the transistor 502 is coupled to the input 422A of the bias voltage generation circuit 422 and the output 416C of the amplifier 416. A drain 502D of the transistor 502 is coupled to a negative voltage source 506. The negative voltage source 506 may provide voltage in a range of -20 to -250 volts for biasing the APD array 402. A source 502S of the transistor 502 is coupled to the output 422B and to terminal 504A of the capacitor 504. A terminal 504B of the capacitor 504 is coupled to ground. The difference voltage received at the gate 502G of the transistor 502 controls the transistor 502, and the bias voltage generated at the source 502S of the transistor 502.

[0032] FIG. 6 is a block diagram of a second APD circuit 600 that uses dark current to bias an APD. The APD circuit 600 may be a light detection circuit, a light detection and ranging (LIDAR) receiver circuit, or other optical transduction circuit. The APD circuit 600 includes the APD array 402 and a bias circuit 604. The bias circuit 604 includes the bias output 404A, the APD 410, the current multiplier circuit 412, the APD 418, a transimpedance amplifier 602, a unity gain buffer 606 (a buffer circuit), and a variable current source 608. As explained with regard to the bias circuit 404, the metal 414 and the metal 420 prevent light from reaching the APD 410 and the APD 418.

[0033] The APD 410 is biased at a low reverse bias by the reference voltage source 424. The dark current generated by the APD 410 is multiplied by M in the current multiplier circuit 412. The multiplied dark current is provided to the variable current source 608.

[0034] In the APD circuit 600, the transimpedance amplifier 602, the unity gain buffer 606, the variable current source 608, and the APD 418 are part of a bias voltage generation circuit. A control input 608A of the variable current source 608 is coupled to the output 412B of the current multiplier circuit 412. The multiplied dark current received at the variable current source 608 controls the current output by the variable current source 608. An input 608C of the variable current source 608 is coupled to a negative voltage source 610. Current MI_{D1} output by the variable current source 608 is forced into the APD 418 to generate the bias voltage for the APD 406. An output 608B of the variable current source 608 is coupled to the anode 418A of the APD 418 and the input 606A of the unity gain buffer 606. The cathode 418C of the APD 418 is coupled to an input 602A of the transimpedance amplifier 602 to provide the same cathode voltage as the APD 406.

[0035] The unity gain buffer 606 buffers the voltage at the anode 418A of the APD 418. An

output 606B of the unity gain buffer 606 is coupled to the bias output 404A to provide bias voltage to the APD 406, and other APDs of the APD array 402.

[0036] FIG. 7 is a block diagram of a third APD circuit 700 that uses dark current to bias an APD. The APD circuit 700 may be a light detection circuit, a light detection and ranging (LIDAR) receiver circuit, or other optical transduction circuit. The APD circuit 700 includes the APD array 402 and a bias circuit 704. The bias circuit 704 includes the bias output 404A, the APD 410, the current multiplier circuit 412, and a variable current source 708. As explained with regard to the bias circuit 404, the metal 414 prevent lights from reaching the APD 410.

[0037] The APD 410 is biased at a low reverse bias by the reference voltage source 424. The dark current generated by the APD 410 is multiplied by M in the current multiplier circuit 412. The multiplied dark current is provided to the variable current source 708.

[0038] In the APD circuit 700, the variable current source 702 is part of a bias voltage generation circuit. A control input 708A of the variable current source 708 is coupled to the output 412B of the current multiplier circuit 412. The multiplied dark current received at the variable current source 708 controls the current at output 708B of the variable current source 708. An input 708C of the variable current source 708 is coupled to a negative voltage source 710. Current MI_{D1} output by the variable current source 708 is forced into the APD 406 to generate the desired bias voltage. An instance of the variable current source 708 is coupled to each APD of the APD array 402 with a control input coupled to the output 412B of the current multiplier circuit 412 and an input coupled to the negative voltage source 710.

[0039] In this description, the term "couple" may cover connections, communications, or signal paths that enable a functional relationship consistent with this description. For example, if device A generates a signal to control device B to perform an action: (a) in a first example, device A is coupled to device B by direct connection; or (b) in a second example, device A is coupled to device B through intervening component C if intervening component C does not alter the functional relationship between device A and device B, such that device B is controlled by device A via the control signal generated by device A.

[0040] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An avalanche photo-diode (APD) circuit, comprising:
   a first APD including an anode;
   a reference voltage source; and
   a bias circuit including:
      a bias output coupled to the anode of the APD;
      a second APD including:
         a cathode coupled to the bias output; and
         an anode coupled to the reference voltage source; and
      a layer of metal covering the second APD.
2. The APD circuit of claim 1, wherein the bias circuit further includes:
   a current multiplier circuit including:
      an input coupled to the cathode of the second APD; and
      an output coupled to the bias output.
3. The APD circuit of claim 2, wherein the bias circuit further includes:
   a variable current source including:
      a control input coupled to the output of the current multiplier circuit; and
      an output coupled to the bias output.
4. The APD circuit of claim 3, wherein:
   the bias circuit further includes:
      a third APD including:
         an anode coupled to the output of the variable current source; and
   the layer of metal covers the third APD.
5. The APD circuit of claim 3, wherein the bias circuit further includes:
   a buffer circuit including:
      an input coupled to the output of the variable current source; and
      an output coupled to the bias output.
6. The APD circuit of claim 2, wherein:
   the bias circuit further includes:
      a third APD including:

an anode coupled to the bias output; and

the layer of metal covers the third APD.

7. The APD circuit of claim 6, wherein:

the third APD includes a cathode; and

the bias circuit further includes:

an amplifier including:

a first input coupled to the output of the current multiplier circuit;

a second input coupled to the cathode of the third APD; and

an output coupled to the bias output.

8. The APD circuit of claim 7, wherein the bias circuit further includes:

a bias voltage generation circuit including:

an input coupled to the output of the amplifier; and

an output coupled to the bias output.

9. An avalanche photo-diode (APD) circuit, comprising:

a first APD configured to detect light;

a bias circuit configured to control a gain of the first APD, and includes:

a second APD;

a reference voltage source configured to bias the second APD;

a metal layer configured to shield the second APD from the light; and

a bias voltage generation circuit configured to generate a bias voltage for biasing the first APD based on dark current output by the second APD.

10. The APD circuit of claim 9, wherein the bias circuit further includes:

a current multiplier circuit coupled to the second APD, and configured to provide, to the bias voltage generation circuit, an output current that is a predetermined multiple of the current output by the second APD.

11. The APD circuit of claim 10, wherein:

the first APD includes an anode; and

the bias voltage generation circuit further includes:

a variable current source including a current output coupled to the anode of the first APD, the variable current source configured to generate, at the current output, a bias current based on the output current of the current multiplier circuit.

12. The APD circuit of claim 11, wherein:

the bias voltage generation circuit further includes:

a third APD including:

an anode coupled to the current output of the variable current source;

the metal layer is configured to shield the third APD from the light.

13. The APD circuit of claim 11, wherein the bias voltage generation circuit further includes:

a buffer circuit coupled to the current output of the variable current source, configured to provide the bias voltage to the first APD.

14. The APD circuit of claim 10, wherein:

the bias circuit further includes:

a third APD biased by the bias voltage; and

an amplifier configured to generate a difference voltage as a difference of current output by the second APD and a current output by the third APD; and

the metal layer is configured to shield the third APD from the light.

15. The APD circuit of claim 14, wherein the bias voltage generation circuit is configured to generate the bias voltage based on the difference voltage.

16. A light detection circuit, comprising:

an avalanche photo-diode (APD) array configured to detect light, and including:

a first APD; and

a transimpedance amplifier coupled to first APD; and

a bias circuit coupled to the APD array, and configured to control a gain of the first APD, the bias circuit including:

a second APD;

a reference voltage source configured to bias the second APD;

a metal layer configured to shield the second APD from the light;

a current multiplier circuit coupled to the second APD, and configured to provide an output current that is a predetermined multiple of a dark current output by the second APD; and

a bias voltage generation circuit configured to generate a bias voltage for biasing the first APD based on the output current of the current multiplier circuit.

17. The light detection circuit of claim 16, wherein:

the first APD includes an anode; and

the bias voltage generation circuit further includes:

a variable current source including a current output coupled to the anode of the first APD, the variable current source configured to generate, at the current output, a bias current based on the output current of the current multiplier circuit.

18. The light detection circuit of claim 17, wherein:

the transimpedance amplifier is a first transimpedance amplifier;

the bias voltage generation circuit further includes:

a third APD including:

an anode coupled to the current output of the variable current source; and

a cathode;

a second transimpedance amplifier coupled to the cathode of the third APD;

a buffer circuit coupled to the current output of the variable current source, and configured to provide the bias voltage to the first APD; and

the metal layer is configured to shield the third APD from the light.

19. The light detection circuit of claim 16, wherein:

the bias circuit further includes:

a third APD biased by the bias voltage; and

an amplifier configured to generate a difference voltage as a difference of current output by the second APD and a current output by the third APD; and

the metal layer is configured to shield the third APD from the light.

20. The light detection circuit of claim 19, wherein the bias voltage generation circuit is configured to generate the bias voltage based on the difference voltage.

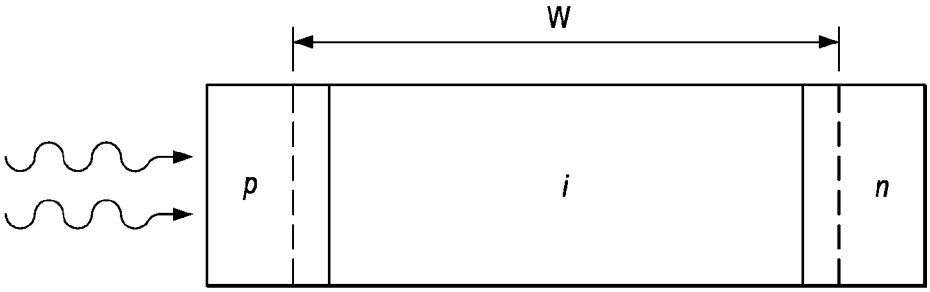


FIG. 1A

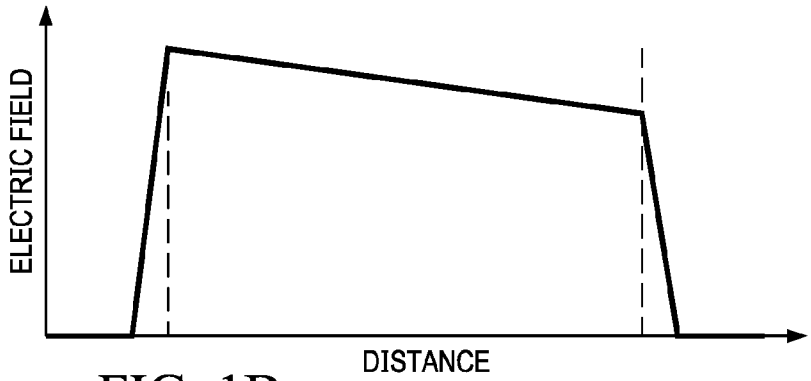


FIG. 1B

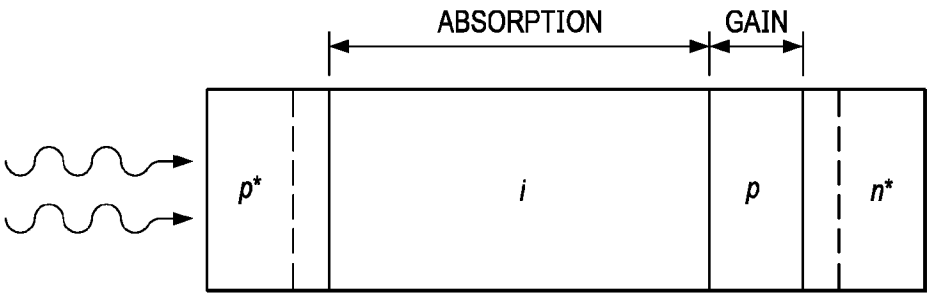


FIG. 2A

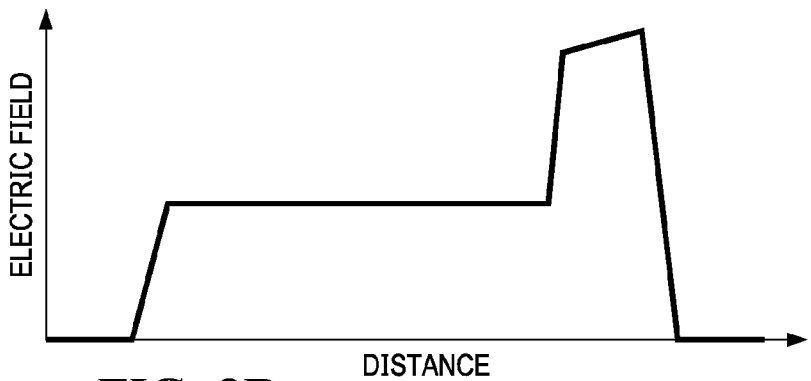


FIG. 2B

FIG. 3A

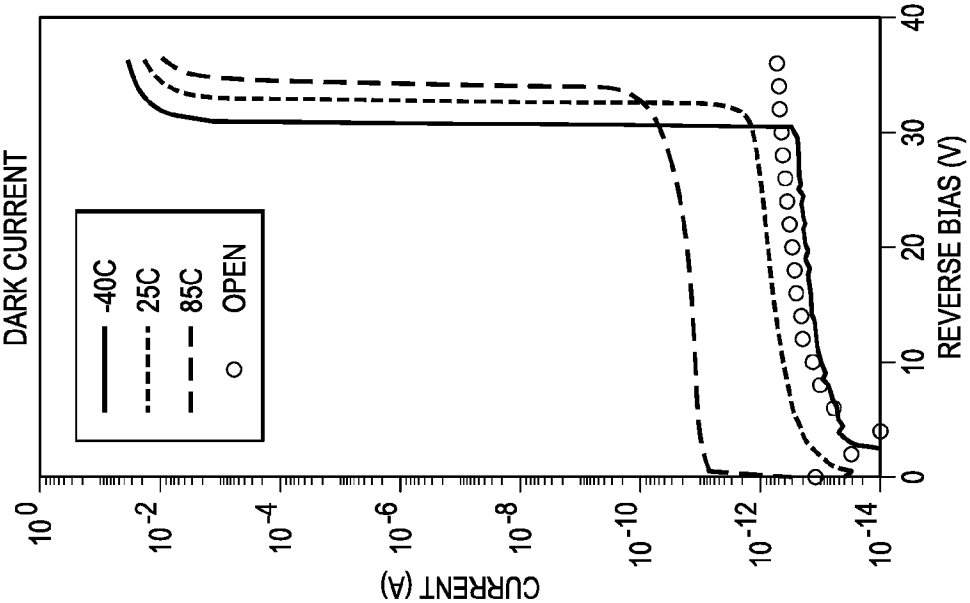


FIG. 3B

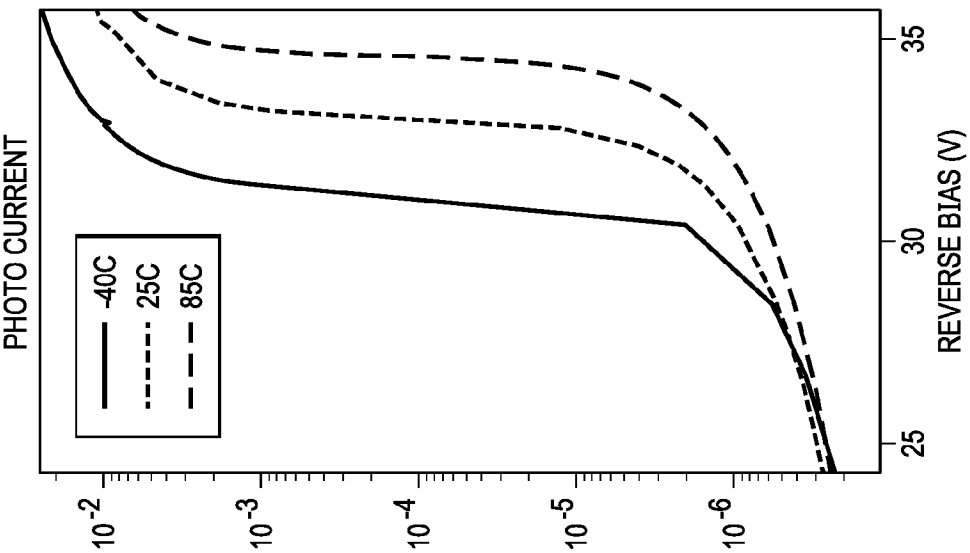
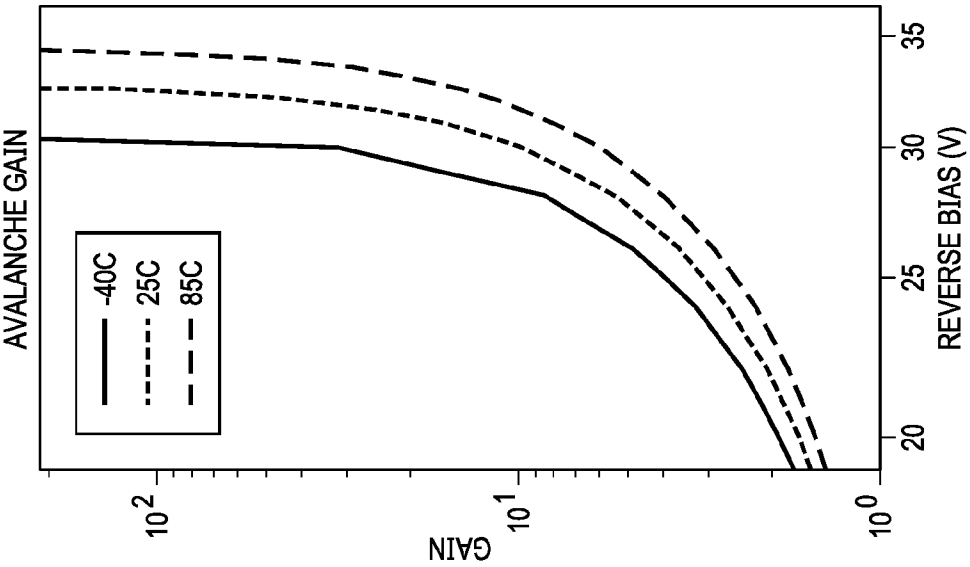


FIG. 3C



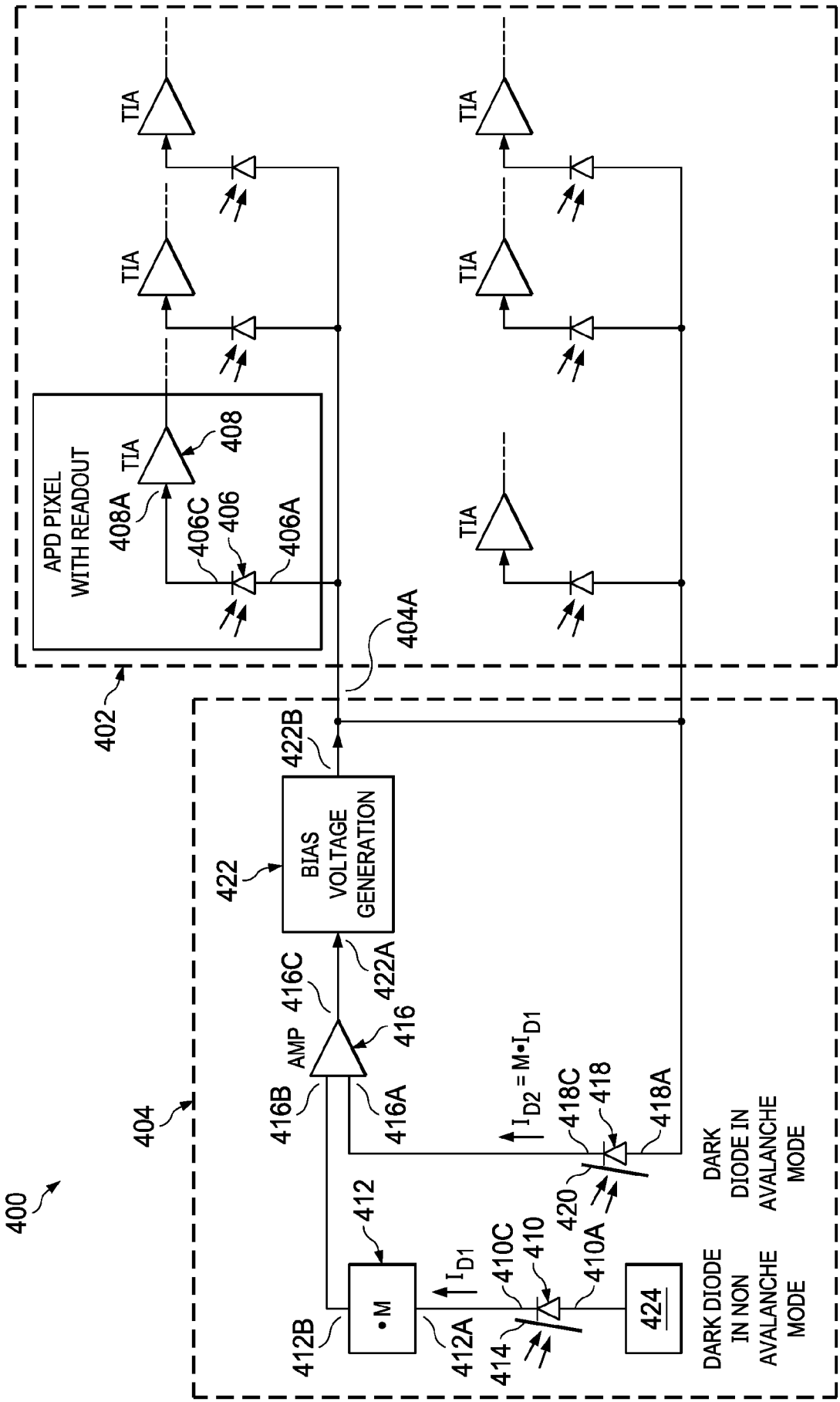

400
402
404
404A
APD PIXEL WITH READOUT
TIA
408
408A
406
406A
406C
422
BIAS VOLTAGE GENERATION
422A
422B
416
416A
416B
416C
AMP
$I_{D2} = M \cdot I_{D1}$
418
418A
418C
420
410
410A
410C
412
412A
412B
I_{D1}
• M
414
424
DARK DIODE IN NON AVALANCHE MODE
DARK DIODE IN AVALANCHE MODE

FIG. 4

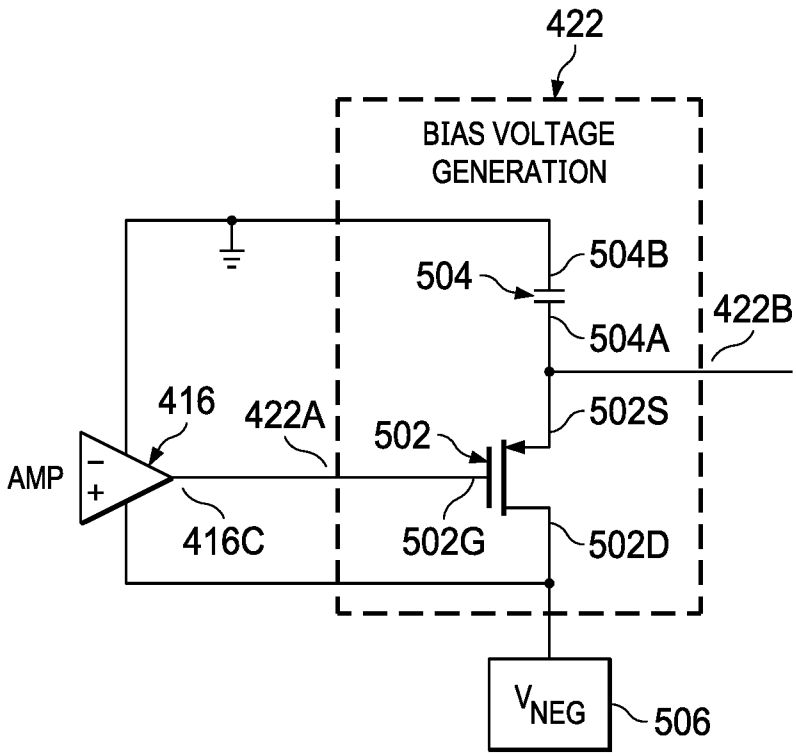

422
BIAS VOLTAGE
GENERATION
504
504B
504A
422B
416
422A
502
502S
AMP
416C
502G
502D
V_{NEG}
506

FIG. 5

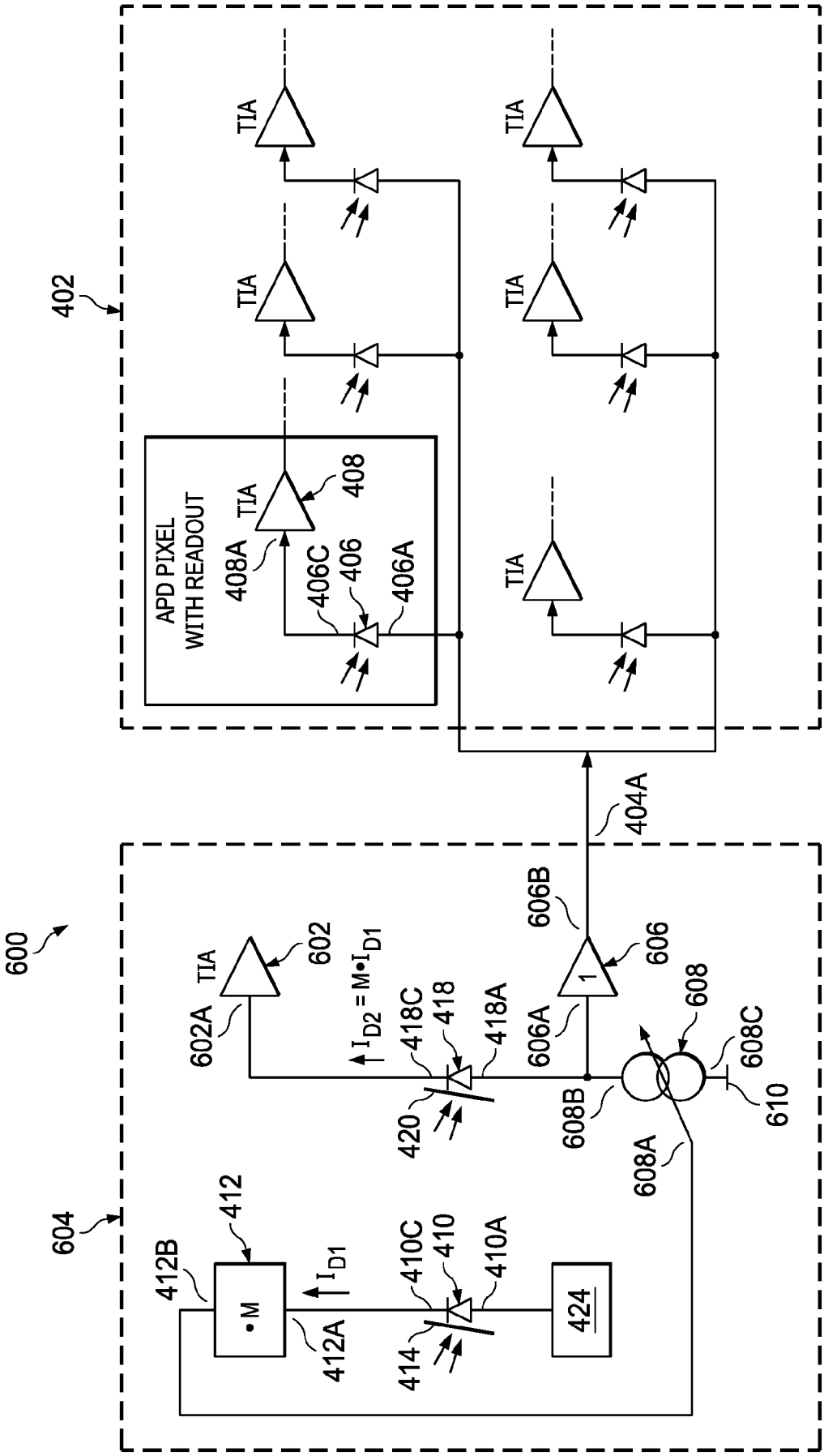

600
604
402
404A
TIA
602
602A
$I_{D2} = M \bullet I_{D1}$
418C
418
418A
420
606B
606
606A
608
608C
608B
608A
610
412
412B
• M
412A
I_{D1}
410C
410
410A
414
424
APD PIXEL WITH READOUT
408
408A
406C
406
406A
1

FIG. 6

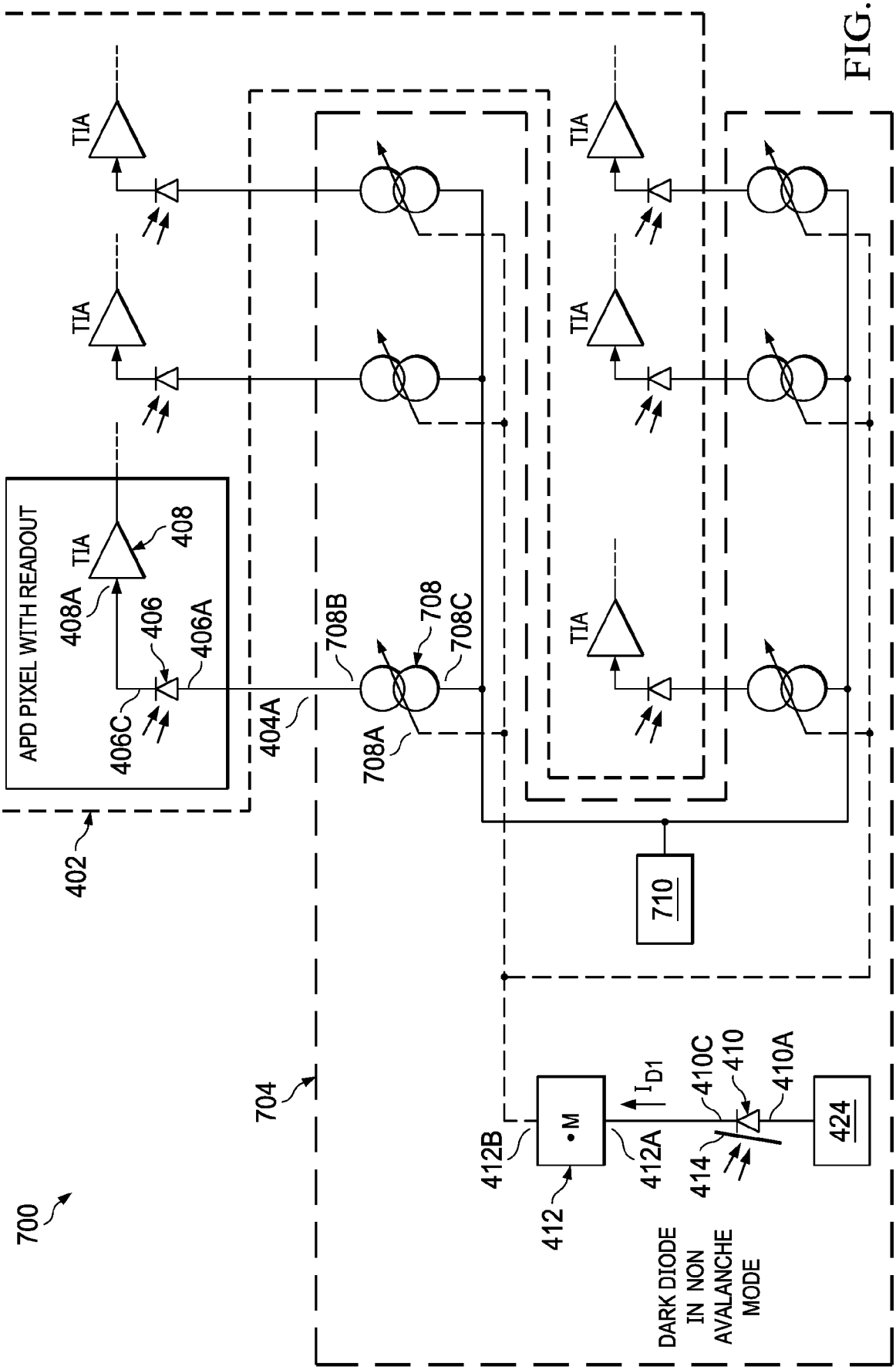

700
704
402
APD PIXEL WITH READOUT
TIA
408
408A
406
406A
406C
404A
708B
708
708C
708A
710
412B
412
412A
M
I_{D1}
410C
410
410A
414
424
DARK DIODE IN NON AVALANCHE MODE

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB 2021/000575

A. CLASSIFICATION OF SUBJECT MATTER

H01L 31/101 *(2006.01)*
G01J 1/44 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 31/101, G01J 1/42, 1/44,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5578815 A (HAMAMATSU PHOTONICS KK) 26.11.1996	1-20
A	WO 2019/199796 A (INNOVUSION IRELAND LIMITED) 17.10.2019	1-20
A	US 2015/0034808 A1 (KABUSHIKI KAISHA TOSHIBA) 05.02.2015	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 December 2021 (07.12.2021)	09 December 2021 (09.12.2021)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer N. Listvina Telephone No. (499) 240-25-91