# United States Patent

[11] 3,594,643


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[21] Appl. No. **826,999**
[22] Filed **May 22, 1969**
[45] Patented **July 20, 1971**
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[54] **ELECTRICAL TIMING APPARATUS WITH INTERRUPTIBLE TIME PRESENTATION**
**3 Claims, 5 Drawing Figs.**


[52] **U.S. Cl.** ..... **324/186,** 235/92 T
[51] **Int. Cl.** ..... **G04f 9/00,** G04f 11/06
[50] **Field of Search** ..... 324/68 C, 70 B; 235/92-29



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UNITED STATES PATENTS

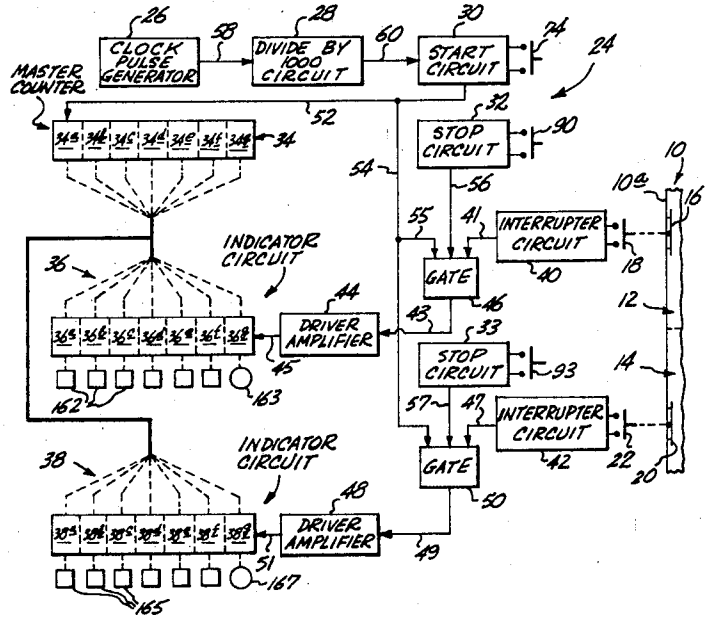
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**ABSTRACT:** Electronic timing apparatus which, upon being started, maintains and normally presents for observation a running indication of the elapsed time of an event. The apparatus includes circuitry which may be triggered in response to some selected occurrence during the event to produce a short term interruption in the running time presentation, whereby the particular time presentation marking the occurrence is sustained for observation. After such an interruption, the time presentation automatically updates and continues to run.

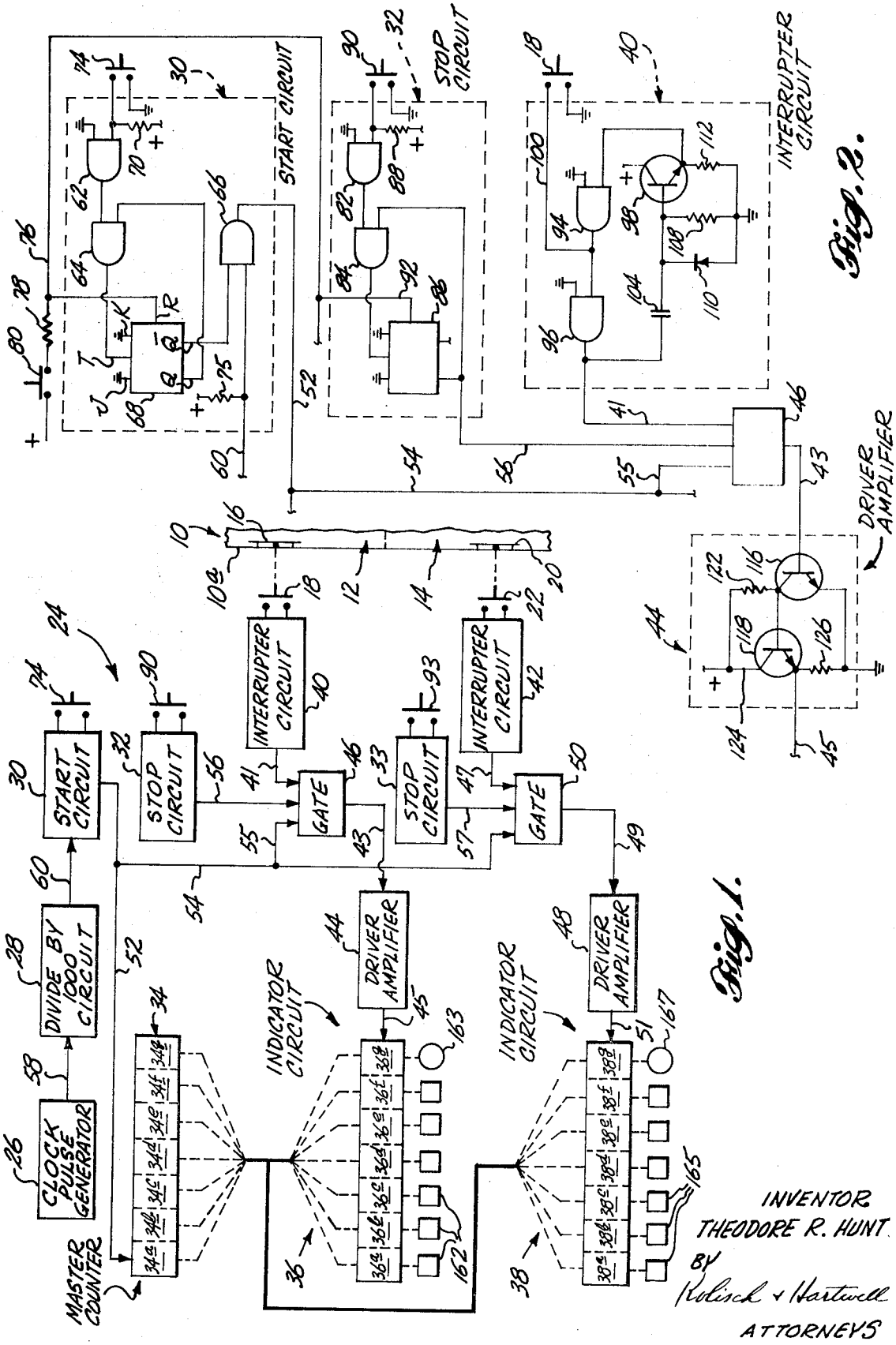



Fig. 1.

Fig. 2.

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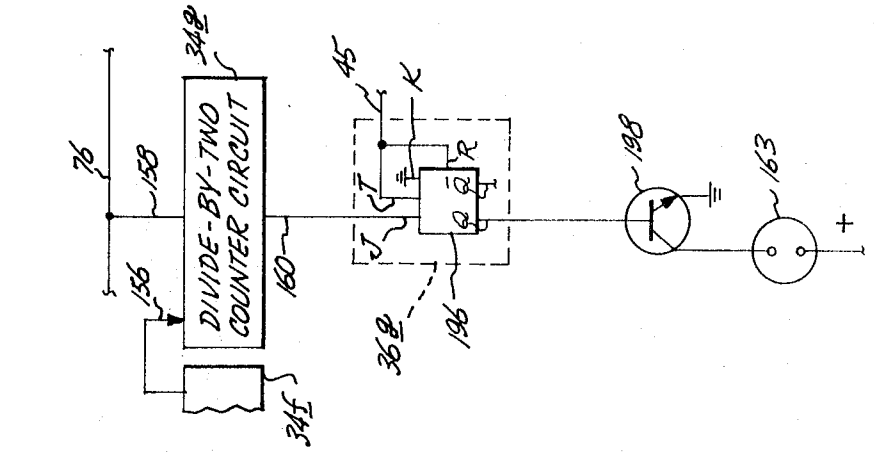



Fig. 5.

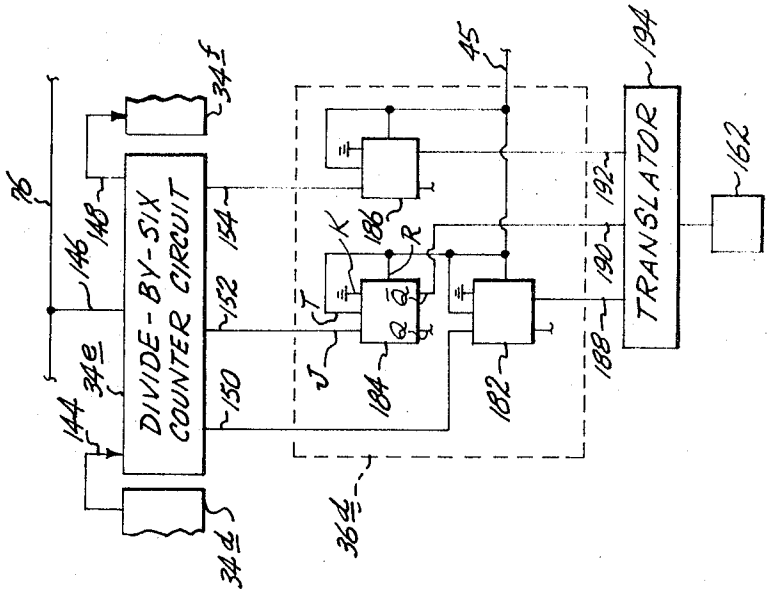



Fig. 4.

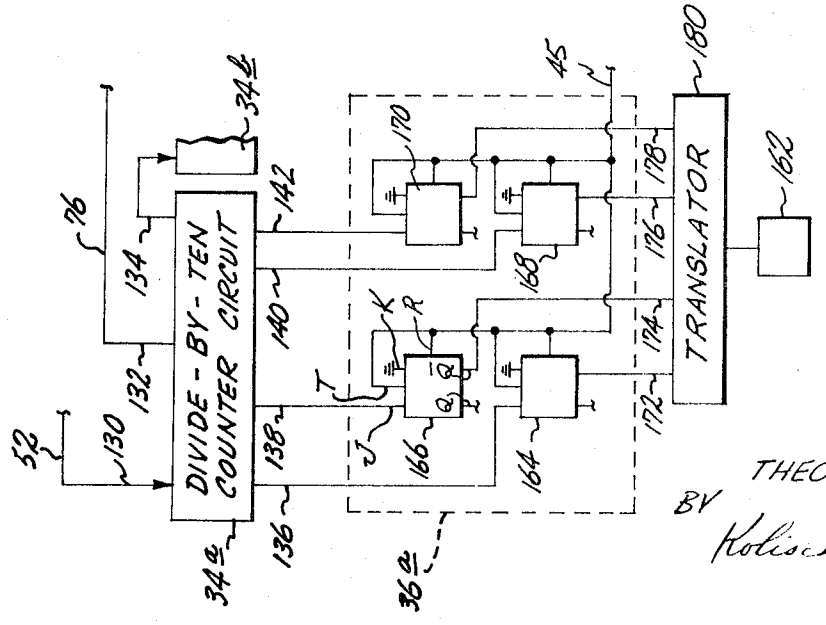



Fig. 3.

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# ELECTRICAL TIMING APPARATUS WITH INTERRUPTIBLE TIME PRESENTATION

This invention pertains to electronic timing apparatus. For the purpose of illustration, a preferred embodiment of the invention is described herein in conjunction with competitive swimming.

In competitive swimming, both during practice and in a meet, it is often desired to record the so-called split and finish times of a swimmer. A split time, generally speaking, is the time which has elapsed from the beginning of a multiple lap event to the completion of a particular lap, and a finish time is the total time required to complete the event. These selected times, if measured accurately, are useful in judging the performance of a swimmer, and in comparing his performance with that of a competitor.

In the past, however, such split and finish times have, for a number of reasons, been difficult to obtain with accuracy. Frequently, for example, a particular swimmer's split and finish times are obtained by an observer employing one or more manually operated stop watches. Such a practice, which relies on the reactions of the observer, clearly opens the door to inaccuracies. Further, conventional timing apparatus generally is not equipped to present, for comparison during an event, the different split and finish times for the various individual competitors. Such a comparison normally can be made only after the event when the different persons who have been observing and recording times have had an opportunity to combine their notes.

A general object of the present invention, therefore, is to provide novel electronic timing apparatus which takes care of the above-mentioned difficulties in a practical and satisfactory manner.

More specifically, an object of the invention is to provide such apparatus which not only is capable of indicating accurately The total elapsed time of an event (such as a swimming race), but also is capable of providing, during the event, an accurate sustained indication marking the time of some selected occurrence (such as the completion of a particular lap) in the race.

A further object is to provide such timing apparatus which further is capable of following and timing the action of more than one participant in an event, whereby comparisons such as those mentioned above may be made during the event.

According to a preferred embodiment of the invention, the proposed timing apparatus includes a pair of supplies of periodic electrical pulses interconnected in such a fashion (to a common source) that the pulses of one supply alternate with the pulses of the other. The pulses of the one supply feed a counting circuit which maintains a running stored count of the number of pulses received. The pulses of the other supply feed an indicator circuit which operates, on receiving such a pulse, to produce an indication reflecting the count then stored in the counting circuit. The indicator circuit sustains such an indication over the interval between successive pulses received from the other supply. An interrupter circuit is provided which is connected to the indicator circuit and which may be actuated to cut off for a short period of time the flow of pulses from the other supply to the indicator circuit.

These and other objects and advantages attained by the invention will become more fully apparent as the description which follows is read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a simplified circuit diagram in block form illustrating timing apparatus constructed according to the invention, and showing how the same may be employed in conjunction with competitive swimming;

FIG. 2 is a circuit diagram, partly in block form, illustrating in somewhat greater detail a start circuit, a stop circuit, and an interrupter circuit employed in the apparatus of FIG. 1;

FIGS. 3—5 inclusive, are circuit diagrams in block form illustrating certain portions of a counting circuit and of an indicating circuit employed in the apparatus of FIG. 1.



## APPARATUS GENERALLY

Turning now to the drawings, and referring first to FIG. 1, indicated at **10***a* is a portion of one end of a competition swimming pool **10**. The pool includes a plurality of the usual side-by-side lanes, such as lanes **12**, **14**, that extend between opposite ends of the pool. End **10***a* is the end at which different swimming races start and finish.

Suitably mounted adjacent pool end **10***a* and in lane **12** is a switch actuator **16** which is ganged to a normally open switch **18**. Actuator **16** may be constructed in any suitable fashion, and is positioned whereby it is engaged by a swimmer when he completes a lap in lane **12**. The actuator, on being engaged, momentarily closed switch **18**. An actuator **20**, similar to actuator **16**, is mounted in lane **14** adjacent pool end **10***a*. Actuator **20** is ganged to a normally open switch **22** which corresponds to switch **18**.

Indicated generally at **24** in FIG. **1** is electronic timing apparatus as contemplated herein. In general terms, apparatus **24** includes a clock pulse generator, or source, **26**, a divide-by-1000 circuit **28**, a start circuit **30**, and a master counter, or counting circuit, **34**. Apparatus **24** further includes a pair of stop circuits **32**, **33**, a pair of indicator circuits **36**, **38**, and a pair of interrupter circuits **40**, **42**. Circuits **32**, **36**, **40** are substantially the same in construction as circuits **33**, **38**, **42**, respectively. The combination of an indicator circuit, such as circuit **36**, and counter **34** comprises a timer means herein. In addition, circuits **40**, **42** each constitutes a change-condition circuit means.

Circuits **36**, **40** are interconnected through a driver amplifier **44**, a gate **46**, and conductors **41**, **43**, **45**. Conductor **41** connects circuit **40** to an input terminal of gate **46**; conductor **43** connects the output terminal of the gate to amplifier **44**; and conductor **45** connects the amplifier and circuit **36**. Circuit **40** is connected to the terminals of switch **18**. In like fashion, circuits **38**, **42** are interconnected through a driver amplifier **48**, a gate **50**, and conductors **47**, **49**, **51**. Amplifier **48** and gate **50** correspond to amplifier **44** and gate **46**, respectively; and conductors **47**, **49**, **51** correspond to conductors **41**, **43**, **45**, respectively. Circuit **42** is connected to the terminals of switch **22**.

Start circuit **30** is connected to counter **34** through a conductor **52** and is connected to inputs of gates **46**, **50** as shown through conductor **52** and conductors **54**, **55**. Conductor **52** is also referred to herein as a means for supplying electrical pulses. Stop circuit **32** is connected to an input of gate **46** through a conductor **56**. Stop circuit **33** is connected to an input of gate **50** through a conductor **57**. Counter **34** is connected to indicator circuits **36**, **38** in a manner which will be more fully described later.

## EXPLANATION OF TERMINOLOGY

Explaining briefly certain terminology which will be used herein, various components in apparatus **24** operate in response to a pair of voltage levels. More specifically, one of these levels corresponds to a certain positive voltage (typically +3 volts) which will be referred to hereinafter as a "**O**" state. The other level corresponds to ground, and will be called hereinafter a "1" state. A terminal, or conductor, having one of these voltage levels on it will be referred to as being in, or having on it, either a "1" or a "**O**" state.

## CLOCK PULSE GENERATOR 26

Clock pulse generator or oscillator means, **26** is a conventional circuit which, when operated, supplies a train of square wave pulses to circuit **28** through a conductor **58**. In the absence of a pulse on conductor **58**, the same is normally in a "1" state. Each clock pulse supplied to conductor **58** places the conductor in a "**O**" state, with the conductor returning to a "1" state after the pulse. Generator **26** produces pulses at a controlled rate which is held as close as possible to one million pulses per second.

DIVIDE-BY-1000 CIRCUIT 28

Circuit 28 is also conventional in construction. For each one thousand pulses received over conductor 58, circuit 28 produces a change in the voltage state on a conductor 60 through which it is connected to start circuit 30. Prior to operation of generator 26 circuit 28 holds conductor 60 in a "1" state. With the generator operating, after the first one thousand pulses thereof are received by circuit 28, the latter places conductor 60 in a "O" state. After the next one thousand pulses are received, it returns conductor 60 to a "1" state, and so on.

Such operation results in a flow of square wave pulses over conductor 60 at a rate of 1,000 pulses per second. With the pulse rate of generator 26 controlled as mentioned above, and with circuit 28 employed in conjunction with the generator, an extremely precise pulse rate (1,000 pulses per second) is maintained in the pulses supplied over conductor 60.

START CIRCUIT 30

Referring to FIG. 2, start circuit 30 includes three conventional two-input NAND gates 62, 64, 66 and a conventional flip-flop 68. Flip-flop 68 includes the usual trigger and reset terminals, T, R, respectively, J and K input terminals, and Q and $\bar{Q}$ output terminals, as indicated.

The upper input terminal of gate 62 in FIG. 2 is connected to ground, and thus is held in a "1" state. The other input terminal of the gate is connected through a resistor 70 to a suitable source of positive voltage (which tends to hold the terminal in a "O" state), and is connected further to one side of a normally open switch 74. The other side of the switch is grounded. In the embodiment shown, switch 74 is of a type constructed to be closed momentarily simultaneously with staring of a race in pool 10. Gate 64 has its upper input terminal in FIG. 2 connected to the output terminal of gate 62, and its other input terminal connected to the Q terminal of flip-flop 68. The output terminal of gate 64 is connected to the trigger input of the flip-flop. Gate 66 has is upper terminal in FIG. 2 connected to the $\bar{Q}$ terminal of the flip-flop. The other input terminal of gate 66 is connected to conductor 60, and also is connected through a resistor 75 to a source of positive voltage which tends to hold the terminal in a "O" state. Preferably, this source of positive voltage is the same as the one mentioned above connected to resistor 70. The output terminal of gate 66 is connected to conductor 52. The J and K terminals of the flip-flop are grounded. Reset terminal R is connected to a reset conductor 76 which, in turn, is connected through a resistor 78 and a normally open switch 80 to the same source of positive voltage just discussed.

Each of the NAND gates in circuit 30 functions as follows: With a "O" state on either input terminal of the gate, the output terminal thereof is held in a "1" state; with both input terminals in "1" states, the output terminal is placed in a "O" state. The output terminals of gates 62, 66 are normally in "1" states, and the output terminal of gate 64 is normally in a "O" state.

With flip-flop 68 connected as shown, the Q and $\bar{Q}$ output terminals thereof are normally in "1" and "O" states, respectively. On the trigger terminal of the flip-flop switching from a "O" to a "1" state, the states on Q, $\bar{Q}$ reverse. A state change in the opposite direction on the trigger terminal produces no change in the states of Q, $\bar{Q}$. On the reset terminal switching from a "O" to a "1" state, $\bar{Q}$, Q are placed in (or left in, as the case may be) what was described above as their normal states. A state change in the reverse direction on the reset terminal has no effect on the states of Q, $\bar{Q}$.

Briefly describing the operation of the start circuit, with the various components in the circuit in their normal conditions just described, conductor 52 is held in a "1" state regardless of the presence of any pulses on conductor 60. With momentary closure of switch 74, the output terminal of gate 62 momentarily switches to a "O" state, which in turn results in the output terminal of gate 64 switching to a "1" state. This state change on the output terminal gate 64 triggers flip-flop 68, and causes the states on Q, $\bar{Q}$ to reverse. With such reversal of the states on Q, $\bar{Q}$, the output of gate 64 is held in a "1" state, and a "1" state is placed on the upper input terminal of gate 66 in FIG. 2. With this change, any pulses flowing over conductor 60 produce corresponding inverted pulses (i.e. 180° out of phase with pulses on conductor 60) on conductors 52, 54, 55. Such pulses are at a pulse rate of 1,000 pulses per second, and cause the states of conductors 52, 54, 55 to alternate between "1" and "0."

With momentary closure of switch 80, a positive voltage pulse, called a reset pulse, is supplied to conductor 76 which places this conductor in a "O" state. The reset pulse is supplied to the reset terminal of flip-flop 68, and termination of the pulse (i.e., a state change from "O" to "1") causes the Q, $\bar{Q}$ terminals to return to their normal states. As a consequence, the states on the output terminals of gates 64, 66 are returned to those which existed thereon prior to closing of switch 74. Conductors 52, 54, 55 are then returned to and held again in "1" states.

STOP CIRCUITS 32, 33

Still referring to FIG. 2, stop circuit 32 includes a pair of two-input NAND gates 83, 84 and a flip-flop 86. Gates 82, 84 are substantially the same in construction as the gates in circuit 30, and flip-flop 86 is substantially the same as flip-flop 68.

The upper input terminal of gate 82 in FIG. 2 is connected to ground, and thus is held in a "1" state. The other input terminal is connected through a resistor 88 to the same source of positive voltage mentioned earlier (which tends to hold the terminal in a "O" state), and is also connected to one side of a normally open switch 90. The other side of switch 90 is grounded. The upper input terminal of gate 84 in the figure is connected to the output terminal of gate 82, and the other input terminal is connected to previously mentioned conductor 56. The output terminal gate 84 is connected to the trigger terminal of flip-flop 86. The reset terminal of the flip-flop is connected through a conductor 92 to reset conductor 76. The Q terminal of flip-flop 86 is connected to conductor 56. The Q terminal of flip-flop 86 is connected to conductor 56. The Q terminal is left floating (i.e., unconnected to anything external to the flip-flop). The J and K terminals of the flip-flop are grounded.

The output terminals of gates 82, 84 normally occupy "1" and "O" states, respectively. Q normally has a "1" state on it, thereby placing conductor 56 normally in a "1" state.

On momentary closing of switch 90, the output terminal of gate 82 switches momentarily to a "O" state and this causes the output terminal of gate 84 to switch to a "1" state. The latter mentioned change causes terminal Q of flip-flop 86 to switch to a "O" state, whereby a "O" state is placed on conductor 56, in addition, the state change on the Q terminal results in the output of gate 84 being held in a "1" state.

This situation remains until there is a momentary closure of switch 80 to place a reset pulse on conductor 76. On termination of such a pulse, the Q terminal of flip-flop 86 returns to a "1" state. This returns a "1" state to conductor 56 and a "O" state to the output terminal of gate 84.

Stop circuit 33 is connected to the terminals of a normally open switch 93 which corresponds to switch 90. Circuit 33 performs in substantially the same manner as circuit 32.

INTERRUPTER CIRCUITS 40, 42

Interrupter circuit 40, illustrated in fig. 2, generally comprises two portions—one including a pair of two-input NAND gates 94, 96, and the other including a transistor 98. Gates 94, 96 are similar to the gates already described. The upper input terminal of gate 94 in FIG. 2 is grounded, and the other input terminal is connected to the emitter of transistor 98. The output terminal of gate 94 is connected to the lower input terminal of gate 96 in the figure, and also is connected through a conductor 100 to one side of previously mentioned switch 18.

The other side of switch **18** is grounded. The other input terminal of gate **96** is grounded, and the output terminal of the gate is connected through a capacitor **104** to the base of transistor **98**, and also to previously mentioned conductor **41**.

The base of transistor **98** is connected to ground through a resistor **108** and a diode **110** which is connected in parallel with the resistor. The emitter is connected to ground through a resistor **112**. The transistor's collector is connected to the same source of positive voltage as the one discussed earlier.

The output terminals of gates **94, 96** normally are in "**O**" and "1" states, respectively, and transistor **98** is normally nonconductive. As a consequence, conductor **41** normally has a "1" state on it.

With momentary closing of switch **18**, the output terminal of gate **94** and the lower input terminal of gate **96** in FIG. **2** switch to a "1" state, and the output terminal of gate **96** switches to a "**O**" state. This places a "**O**" state on conductor **41**. Capacitor **104** then charges through resistor **108**, and transistor **98** conducts. Conduction in transistor **98** locks the output terminals of gates **94, 96** in the states to which they have just been switched.

As capacitor **104** continues to charge, the voltage across resistor **108** decreases, and when such voltage drops below a certain level, transistor **98** stops conducting. The length of time required for this to occur (after initial closing of switch **18**) is determined primarily by the capacitance of capacitor **104** and by the resistance of resistor **108**. In the embodiment of the invention shown, this time interval is about ten seconds.

When transistor **98** stops conducting, the output terminals of gates **94, 96** are returned to the states which they had prior to closing of switch **18**. As a consequence, a "1" state is returned to conductor **41**. Capacitor **104** thereupon discharges through diode **110**.

Circuit **42** responds to momentary closure of switch **22** in essentially the same fashion as circuit **40** responds to closure of switch **18**. A time interval similar to that described in conjunction with circuit **40** also characterizes the operation of circuit **42**.

## DRIVER AMPLIFIERS 44, 48 AND GATES 46, 50

Gate **46** is a conventional unit known as a three-input NAND gate. It is similar in many respects to the gates already described herein, except that it has three instead of two input terminals. With a "**O**" state existing on any one of its input terminals, the output terminal of the gate is held in a "1" state. With all input terminals placed in a "1" state, the output terminal is placed in a "**O**" state. The connections to the input and output terminals of the gate have already been described.

Considering how gate **46** performs in the apparatus, with "1" states existing on conductors **55, 56, 41**, a "**O**" state exists on the output terminal of the gate. With conductors **56, 41** having "1" states on them, (the states normally present on these conductors), and with conductor **55** alternating between "**O**" and "1" states as the result of pulses coming from the output of gate **66** in the start circuit, inverted pulses corresponding to those just mentioned are supplied at the output terminal of gate **46** to conductor **43**. And it should be noted that these latter mentioned pulses are related in time, on a one-to-one basis, to pulses coming from gate **66**. More specifically, considering a single pulse from gate **46** on conductor **43**, the time when this pulse changes the state of the conductor from "**O**" to "1" is approximately one two-thousandths of a second later than the time when the corresponding pulse on conductor **55** changes the state of that conductor from "**O**" to "1." Thus, gate **46** is also referred to herein as a means for supplying electrical pulses. In the embodiment of the invention described herein, the pulses supplied over conductor **43**, and those supplied over conductors **55, 54, 52, 60, 58**, are referred to as a family of pulses since they are all traceable to a common source—namely generator **26**.

With a "**O**" state existing either on conductor **56** or on conductor **41**, the output terminal of gate **46** is held in a "1" state regardless of the presence of any pulses conductor **55**. Gate **50** (see FIG. **1**) performs in substantially the same manner.

Referring to FIG. **2**, driver amplifier **44** includes a pair of transistors **116, 118**. The emitter of transistor **116** is connected to ground and the base of the transistor is connected to conductor **43**. The collector of transistor **116** is connected to the base of transistor **118**, and also is connected to a source of positive voltage (which preferably is the same source mentioned above) through a resistor **122**. Positive voltage is supplied the collector of transistor **118** through a conductor **124**. The emitter of transistor **118** is connected to ground through a resistor **126**, and also is connected to previously mentioned conductor **45**.

With pulses produced at the output terminal of gate **46**, as mentioned above, amplifier **44** functions as a current amplifier making such pulses available at a relatively high current on conductor **45**. Amplifier **48** performs in a manner similar to that described for amplifier **44**.

## MASTER COUNTER 34

Referring first to FIG. **1**, counter **34** is made up of seven conventional counter circuits designated at **34***a* —**34***g*, inclusive. Circuits **34***a* —**34***d*, inclusive, and circuit **34***f*, are substantially the same in construction, and constitute what are known as divide-by-10 counter circuits Circuit **34***e* constitutes a divide-by-6 counter circuit. Circuit **34***g* constitutes a divide-by-2 counter circuit.

Turning now to FIG. **3** which further illustrates circuit **34***a* (which is representative of the divide-by-10 counter circuits), the circuit includes an input terminal **130**, a reset terminal **132**, a transfer terminal **134**, and four count-presenting output terminals **136, 138, 140, 142**. Input terminal **130** is connected to previously mentioned conductor **52**, and reset terminal **132** is connected to reset conductor **76**. Transfer terminal **134** is connected to the input terminal of counter circuit **34***b*.

Briefly describing the operation of circuit **34***a*, successive pulses supplied to input terminal **130** over conductor **52** are counted in circuit **34***a*. More specifically, that portion of a pulse causing the state of terminal **130** to change from "**O**" to "1" causes a new count to be registered and stored in the counter circuit in a manner well known to those skilled in the art. Circuit **34***a* counts in cycles, from zero to nine, and back to zero. For each successive pulse counted, the counter circuit produces a related set of voltage states (of the type so far discussed) on conductors **136, 138, 140, 142**. For every tenth pulse received and counted, circuit **34***a* produces a state change (from "**O**" to "1") on transfer terminal **134** which results in the registration of a count in the next adjacent counter circuit—circuit **34***b* in this case. Table I below illustrates the particular voltage states which exist on conductors **136, 138, 140, 142, 134** for different counts stored in circuit **34***a*.

TABLE I

Voltage States on Different Conductors

| Count | 136 | 138 | 140 | 142 | 134 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 |

Upon the application of a reset pulse over conductor **76** to reset terminal **132**, regardless of what count then exists in circuit **34***a*, the latter is switched to a zero-count condition.

Counter circuits **34***b*, **34***c*, **34***d*, **34***f* perform in a similar fashion. Pulses received at their respective input terminals are counted, and produce related sets of voltage states on their respective output and transfer terminals corresponding to those states shown in Table I above for circuit **34***a*.

Referring to FIG. **4**, counter circuit **34***e* is similar in many respects to the divide-by-10 counter circuits just described, except that it has three rather than four count-presenting output terminals. Thus, circuit **34***e* includes an input terminal **144**, a reset terminal **146**, a transfer terminal **148**, and count-presenting output terminals **150, 152, 154**. Input terminal **144** is connected to the transfer terminal of counter circuit **34***d*. Reset terminal **146** is connected to reset conductor **76**. Transfer terminal **148** is connected to the input terminal of counter circuit **34***f*.

The operation of circuit **34***e* is somewhat similar to that of the divide-by-10 counter circuits, except that it counts in cycles from zero to five, and then back to zero. A new count is registered and stored in the circuit whenever the state of input terminal **144** changes from "**O**" to "1." Table II below illustrates the particular voltage states that exist on conductors **150, 152, 154, 148** for different counts stored in circuit **34***e*.

TABLE II

Voltage States on Different Conductors

| Count | 150 | 152 | 154 | 148 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 0 |

Upon the application of a reset pulse to terminal **146**, counter circuit **34***e* returns to a zero-count condition.

Referring to FIG. **5**, counter circuit **34***g* includes an input terminal **156**, a reset terminal **158**, and a count-presenting output terminal **160**. Input terminal **156** is connected to the transfer terminal of counter **34***f*, and reset terminal **158** is connected to reset conductor **76**.

Circuit **34***g* counts from zero to one, and then returns to zero. With the counter in a zero-count condition, output terminal **160** is in a "**O**" state. A change from "**O**" to "**1**" in the state of input terminal **156** causes output terminal **160** to change its state. A reset pulse applied to terminal **158** places circuit **34***g* in a zero-count condition.

Considering counter **34** as a whole, it will be apparent that with pulses supplied at the rate of one thousand pulses per second to the input terminal of circuit **34***a*: circuit **34***a* produces at its output terminals voltage states reflecting thousandths of seconds; circuit **34***b*—hundredths of seconds; circuit **34***c*—tenths of seconds; circuit **34***d*—seconds, circuit **34***e*—tens of seconds; circuit **34***f*—minutes; and circuit **34***g*—tens of minutes. In the embodiment illustrated, counter **34** is employed to count from 0 to 20 minutes.

## INDICATOR CIRCUITS **36, 38**

Considering the construction of indicator circuit **36** (the two indicator circuits shown being substantially the same), it includes seven memory circuits **36***a*—**36***g*, inclusive (see FIG. **1**). Connected to memory circuits **36***a*——**36***f*, inclusive, in a manner which will be more fully described, are indicating devices, such as those shown at **162** in FIG. **1**, which produce a visible indication of the information (in the present case, a count) stored in the memory circuits. Preferably, devices **162** are well-known commercially available units called "Nixie" tubes. Connected to memory circuit **34***g* is an ordinary neon lamp **163**. Devices **162** and **163** are referred to herein collectively as output means.

Referring to FIG. **3**, memory circuit **36***a* includes four flip-flops indicated at **164, 166, 168, 170**. These flip-flops are substantially the same in construction as the ones described earlier. As can be seen, the trigger and reset terminals of all of these flip-flops are connected together, and are connected to previously mentioned conductor **45**. The K terminal of each flip-flop is grounded, and the Q terminal of each is left floating. The J terminals of flip-flops **164, 166, 168, 170** are connected to output terminals **136, 138, 140, 142**, respectively, of circuit **34***a*. The $\bar{Q}$ terminals of flip-flops **164, 166, 168, 170** are connected through conductors **172, 174, 176, 178**, respectively, to the input terminals of a conventional binary-coded-decimal to decimal translator **180**. Translator **180** is connected in a well-known fashion to one of devices **162**. In order to simplify FIG. **3** this connection is represented by a single line.

With the flip-flops in memory circuit **36***a* connected as shown, on a pulse being supplied thereto over conductor **45** which switches the conductor from a "**O**" state to a "**1**" state, each flip-flop places its $\bar{Q}$ output terminal in the same state as that which is then occupied by the J terminal of the flip-flops. Thus, each time such a state change occurs on conductor **45**, conductors **172, 174, 176, 178** are placed in the same states then characterizing conductors **136, 138, 140, 142**, respectively. The voltage conditions on conductors **172, 174, 176, 178** remain unchanged until the next pulse occurs on conductor **45** which causes a state change thereon from "**O**" to "**1**." At such time, the states on conductors **172, 174, 176, 178** adjust to reflect any change which may have occurred in the states of the respective associated output terminals of circuit **34***a*. If no change has occurred in the state of a particular output terminal, no state change occurs on the associated one of conductors **172, 174, 176, 178**.

Thus, it will be apparent that the voltage states on these conductors are indicative of the count which was stored in counter circuit **34***a* at the time of the last pulse over conductor **45**. The fact that a pulse on conductor **45** (coming from conductor **43**) follows its associated or corresponding pulse on conductor **55**, ensures ample time for a new count to be registered in counter **34**.

Translator **180** functions in a well-known manner to supply device **162** with information whereby the device presents in visible and decimal form a number reflecting the states on conductors **172, 174, 176, 178**. The number presented corresponds to the count in circuit **34***a* indicated by such states. It will be apparent, therefore, that each time a pulse is supplied over conductor **45** to the flip-flops in circuit **36***a*, device **162** indicates in decimal form the count then stored in counter circuit **34***a*.

Memory circuits **36***b*, **36***c*, **36***d* and **36***f* are similar in construction and operation to circuit **36***a*, and are connected to counter circuits **34***b*, **34***c*, **34***d* and **34***f*, respectively, in substantially the same manner that circuit **36***a* is connected to circuit **34***a*. Translators similar to translator **180** are provided for these memory circuits.

Referring to FIG. **4**, memory circuit **36***e* is similar in many ways to the memory circuits just described, except that it includes three rather than four flip-flops, indicated at **182, 184, 186**. The trigger, reset, K and Q terminals of these flip-flops are connected in substantially the same fashion as are the corresponding terminals of the flip-flops in circuit **36***a*. The J terminals of flip-flops **182, 184, 186** are connected to output terminals **150, 152, 154**, respectively, of counter circuit **34***e*, and the $\bar{Q}$ terminals are connected through conductors **188, 190, 192**, respectively, to the input terminals of a translator **194**. Translator **194** is connected to an indicating device **162** in much the same fashion as is translator **180**. Again, and since

this type of connection is well understood, only a single line is used to represent the connection for the sake of simplifying FIG. 4.

Memory circuit 36*e* performs in a manner similar to that described for circuit 36*a*, and translator 194 performs in a way similar to that described for translator 180. Each time a pulse occurs on conductor 45, the indicating device connected to translator 194 indicates in decimal form the count then stored in counter circuit 34*e*.

Completing a description of the apparatus, and referring to FIG. 5, memory circuit 36*g* includes a single flip-flop 196 which is substantially the same as the other flip-flops described so far. As in the case of the other flip-flops in the various memory circuits, flip-flop 196 has its trigger and reset terminals connected together and to conductor 45, and its K terminal grounded. The $\bar{Q}$ output terminal, however, rather than the Q terminal, is left floating. The J input terminal is connected to output terminal 160 of counter circuit 34*g*. The Q output terminal of the flip-flop is connected to the base of a transistor 198, the emitter of which is grounded, and the collector of which is connected to one side of lamp 163. The other side of lamp 163 is connected to a suitable source of positive voltage.

The operation of memory circuit 36*g* is similar to that of the other memory circuits described above. With conductor 160 in a "O" state (its normal state), the Q output of flip-flop 196 is held in a "1" state. As a consequence, transistor 198 is nonconductive, and lamp 163 is unlit.

With output terminal 160 placed in a "1" state (which occurs after the first pulse is received at input terminal 156 producing a state change thereon from "O" to "1"), 0, and on the next pulse thereafter occurring on conductor 45 which changes the state thereof from "O" to "1," the Q output of flip-flop 196 is placed in a "O" state, transistor 198 conducts, and lamp 163 lights up. It will be noted that lighting of lamp 163 marks a time of ten minutes.

With output terminal 160 returned to a "O" state (which occurs with the next pulse received at input terminal 156 producing a state change thereon from "O" to "1"), and after the next pulse thereafter (like the one described above) is received on conductor 45, lamp 163 is turned off. Turning off of the lamp marks a time period of 20 minutes.

Indicator circuit 38 (see FIG. 1) includes seven memory circuits 38*a*—38*g* which correspond to memory circuits 36*a*—36*g*, respectively, in circuit 36. Circuits 38*a*—38*g* are connected to counter circuits 34*a*—34*g*, respectively, in substantially the same fashion as are memory circuits 36*a*—36*g*. Circuits 38*a*—38*f* are connected to indicating devices, such as those shown at 165, which correspond to devices 162. Circuit 38*g* is connected to a neon lamp 167 which corresponds to lamp 163.

## Operation of Apparatus 24

Initially, the various components of the start, stop, and interrupter circuits occupy their normal conditions, with conductors 52, 54, 55, 56 and 57 in "1" states. The various counter circuits in master counter 34 are in zero-count conditions. Indicating devices 162, 165 present zeros, and lamps 163, 167 are unlit. Pulses resulting from the operation of generator 26 are produced on conductor 60 at the rate mentioned earlier, but initially have no effect on the voltage states of conductors 52, 54, 55.

Upon starting of a race in pool 10, switch 74 closes momentarily, as indicated earlier, and pulses are supplied over conductors 52, 54, 55 which change the states of these conductors alternately between "1" and "O" states. The pulses supplied over conductor 52 are fed to master counter 34 which maintains a running stored count of the number of pulses received. The pulses supplied over conductors 54, 55 result in the production of pulses (inverted, as explained earlier) on conductors 43, 49.

The pulses thus produced on conductors 43, 49 are fed through amplifiers 44, 48 and conductors 45, 51, respectively, to the various memory circuits in indicator circuits 36, 38, respectively. Each pulse transmitted over conductor 45 results in circuit 36 presenting (through devices 162 and lamp 163) a visible presentation reflecting the count then stored in master counter 34. Each pulse transmitted over conductor 51 results in similar action in circuit 38. As a consequence, so long as pulses continue to be received over conductors 45, 51, circuits 36, 38 produce corresponding running indications of the time elapsed from the beginning of the race.

On the swimmer occupying lane 12 in the pool, for example, completing his first lap, he engages actuator 16 which momentarily closes switch 18. As a consequence, conductor 41 is placed in a "O" state for a period of about ten seconds due to the operation of circuit 40 described above. This results in conductor 43 (and hence conductor 45) being placed and held in "O" states, with the supply of pulses over conductor 45 thus interrupted.

During the period of time that this situation remains, the running count presentation of indicator circuit 36 is stopped, with the indicator circuit sustaining in devices 162 and lamp 163 an indication of the count which was stored in the master counter at the time the swimmer engaged actuator 16. Sustaining of this count results from the operation of the memory circuits in circuit 36.

At the end of the 10-second period mentioned, conductor 41 returns to a "1" state, and pulses are again supplied circuit 36 over conductor 45. Circuit 36 then continues to present a running and updated indication reflecting the running count of counter 34.

A similar operation takes place with respect to circuit 38 on the swimmer in lane 14 engaging actuator 20.

At the end of the race, and as each swimmer finishes, the stop circuit associated with his lane may be operated. For example, upon the swimmer in lane 12 finishing, switch 90 may be closed momentarily to place a "O" state voltage on conductor 56. This action prevents any further flow of pulses over conductor 45 until the stop circuit is returned to its normal condition.

It should be understood that while momentary closure (accomplished in any suitable manner) of a switch is employed herein to operate a stop circuit, other means could be used. For example, and considering stop circuit 32, it might be desirable in certain instances to use, instead of switch 90, a suitable circuit which on completion of a race would, automatically and momentarily place a "1" state on the lower input terminal of gate 62 in FIG. 2.

The various circuits in the apparatus may be returned to the conditions which they had immediately prior to starting of the race through momentary closure of switch 80 which places a reset pulse on conductor 76.

Thus, the invention takes care of the problems mentioned earlier which have posed difficulties in the past. Split and finish times are clearly presented in a sustained fashion, and with a high degree of accuracy. Accuracy is enhanced by the fact that marking of split and finish times results from a swimmer striking an actuator located in the pool, and also by the fact that times are presented to the nearest one-thousandth of a second. Also contributing to accuracy is the fact that the indicator circuits for different swimmers receive information from a common timing source. Reliable time comparisons, therefore, are possible, and are obtainable during a race.

While the invention has been described in conjunction with a pair of indicator and interrupter circuits, it is appreciated that a greater or lesser number may be employed. Also, it is appreciated that the apparatus of the invention may be employed to time different types of events.

Thus, while an embodiment of the invention has been described herein, it is appreciated that variations and modifications are possible without departing from the spirit of the invention.

I claim and desire to secure by Letters Patent:

1. Electronic timing apparatus comprising

oscillator means for producing electrical pulses;

timer means operatively connected to said oscillator means including

at least one counting circuit adapted to receive pulses from said oscillator means, and operable to maintain a running count of the number of pulses so received with the particular count existing at any given time stored in the circuit, and

an indicator circuit operatively connected to said counting circuit placeable alternately and repeatedly in two different operating conditions during operation of said counting circuit, said indicator circuit when placed in one of said operating conditions presenting a running indication of the current total number of pulses counted by the counting circuit, and when placed in the other operating condition presenting a sustained indication of the total number of pulses counted by the counting circuit up to the time of such placement of the indicator circuit in said other operating condition; and

change-condition circuit means operatively connected to said indicator circuit operable to change the operating condition of the indicator circuit.

2. Electronic timing apparatus comprising

a pulser for producing electrical pulses,

a counter operatively connected to said pulser for receiving pulses therefrom, operable to produce a running count reflecting the total number of pulses received,

an indicator, and

means for alternatively coupling and uncoupling said indicator and counter,

said indicator being constructed to present a running indication of the current count in said counter when coupled to the same, and to present a sustained indication of the last count so indicated when uncoupled from the counter.

3. Electronic timing apparatus comprising

a pulser for producing electrical pulses,

a counter operatively connected to said pulser for receiving pulses therefrom, operable to produce a running count reflecting the total number of pulses received, and

an interruptible, automatically updatable indicator adapted for intermittent coupling to said counter, constructed whereby, during operation of the counter, whenever the indicator is uncoupled from the counter it presents a sustained indication of the last count in the counter at the time of such uncoupling, and whenever the indicator is coupled to the counter it automatically updates and presents a running indication of the current count in the counter.