

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
21 December 2007 (21.12.2007)

PCT

(10) International Publication Number  
**WO 2007/146754 A1**

(51) International Patent Classification:  
**F04D 27/00** (2006.01) **H02P 27/08** (2006.01)

(21) International Application Number:  
PCT/US2007/070658

(22) International Filing Date: 8 June 2007 (08.06.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
11/453,511 15 June 2006 (15.06.2006) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

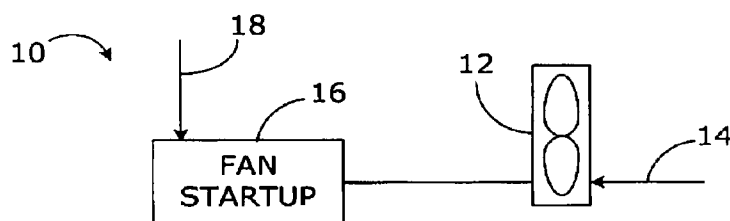
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: APPARATUS AND METHOD TO PROVIDE REDUCED FAN NOISE AT STARTUP



(57) Abstract: In some embodiments, a system includes an electronic system board, a fan positioned to provide cooling for the electronic system board, wherein the fan is configured to be controlled by a pulse width modulated signal, and a fan startup circuit configured to operate the fan in accordance with a first operating condition during startup and in accordance with a second operating condition after startup. Other embodiments are disclosed and claimed.

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## **APPARATUS AND METHOD TO PROVIDE REDUCED FAN NOISE AT STARTUP**

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**[0001]** The invention relates to acoustic noise management techniques. More particularly, some embodiments of the invention relate to an apparatus and method to provide reduced fan noise at startup.

### 10 **BACKGROUND AND RELATED ART**

**[0002]** Many electronic systems require or benefit from the use of noise management devices. In some electronic systems, fan speed may be controlled by a fan control circuit. However, during startup and before the fan control circuit  
15 is initialized, the fan may operate at an unnecessarily high fan speed which causes an undesirable amount of fan noise during startup of the electronic system.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

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**[0003]** Various features of the invention will be apparent from the following description of preferred embodiments as illustrated in the accompanying drawings, in which like reference numerals generally refer to the same parts throughout the drawings. The drawings are not necessarily to scale, the  
25 emphasis instead being placed upon illustrating the principles of the invention.

[0004] Fig. 1 is a block diagram of a noise management apparatus in accordance with some embodiments of the invention.

[0005] Fig. 2 is a block diagram of a processor-based system utilizing a noise management circuit in accordance with some embodiments of the invention.

[0006] Fig. 3 is another block diagram of a processor-based system utilizing a noise management circuit in accordance with some embodiments of the invention.

[0007] Fig. 4 is a flow diagram in accordance with some embodiments of the invention.

[0008] Fig. 5 is a block diagram of another processor-based system utilizing a noise management circuit in accordance with some embodiments of the invention.

[0009] Fig. 6 is a logic diagram of a fan startup circuit in accordance with some embodiments of the invention.

[0010] Fig. 7 is a schematic diagram of another fan startup circuit in accordance with some embodiments of the invention.

## DESCRIPTION

[0011] In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular structures, architectures, interfaces, techniques, etc. in order to provide a thorough understanding of the various aspects of the invention. However, it will be apparent to those skilled in

the art having the benefit of the present disclosure that the various aspects of the invention may be practiced in other examples that depart from these specific details. In certain instances, descriptions of well known devices, circuits, and methods are omitted so as not to obscure the description of the present invention  
5 with unnecessary detail.

**[0012]** With reference to Figs. 1, a noise management device 10 includes a fan 12 configured to be controlled by a pulse width modulated (PWM) signal 14 and a fan startup circuit 16 coupled to the fan 12 and configured to operate  
10 the fan 12 in accordance with a first operating condition during startup and in accordance with a second operating condition after startup. For example, the first operating condition may correspond to a reduced fan noise during startup. For example, the fan startup circuit 16 may be configured to operate the fan 12 with a reduced fan speed during startup. In some embodiments,  
15 the fan startup circuit 16 may be configured to provide a reduced operating voltage to the fan 12 during startup.

**[0013]** In some embodiments, the fan startup circuit 16 may be configured to receive a signal 18 indicating that the fan 12 is ready to operate in accordance with the second operating condition. For example, the second  
20 operating condition may correspond to pulse width modulated (PWM) operation by another fan control circuit. For example, the fan startup circuit 16 may be configured to provide a full operating voltage to the fan 12 in response to the signal 18 indicating that the fan 12 is ready to operate in accordance with the second operating condition.

**[0014]** With reference to Fig. 2, an electronic system 20 includes an electronic system board 21, a fan 22 positioned to provide cooling for the electronic system board 21, wherein the fan 22 is configured to be controlled by pulse width modulated (PWM) signal 23, and a fan startup circuit 24

5 configured to operate the fan 22 in accordance with a first operating condition during startup and in accordance with a second operating condition after startup. For example, the first operating condition may correspond to a reduced fan noise during startup. For example, the fan startup circuit 24 may be configured to operate the fan 22 with a reduced fan speed during startup.

10 In some embodiments, the fan startup circuit 24 may be configured to provide a reduced operating voltage to the fan 22 during startup.

**[0015]** In some embodiments, the fan startup circuit 24 may be configured to receive a signal 25 indicating that the fan 22 is ready to operate in accordance with the second operating condition. For example, the second

15 operating condition may correspond to pulse width modulated (PWM) operation by another fan control circuit 28. For example, the fan startup circuit 24 may be configured to provide a full operating voltage to the fan 22 in response to the signal 25 indicating that the fan 22 is ready to operate in accordance with the second operating condition.

20 **[0016]** In some embodiments, the system 20 comprises a processor-based system including a processor 26 on the electronic system board 21 and a basic input / output system (BIOS) 27, wherein the BIOS 27 provides the signal 25 indicating that the fan 22 is ready to operate in accordance with the second operating condition. For example, the BIOS 27 may provide the

signal 25 indicating that the fan 22 is ready to operate in accordance with the second operating condition after a successful completion of a power on self test (POST).

**[0017]** With reference to Fig. 3, another system 30 is similar to the system 20, with like reference numerals referring to similar elements. Those skilled in the art will understand that in some embodiments the BIOS 27 does not necessarily directly control the fan circuitry (e.g. the fan startup circuit 24 and / or the fan control circuit 28). In some embodiments, the BIOS 27 may send a signal to a general purpose input / output port (GPIO 32, for example, usually located at a South Bridge-ICH or SIO) which may then toggle the signal 25 to enable the fan startup circuit 24 to switch to the second operating condition. Likewise, in some embodiments, the BIOS 27 does not necessarily have a direct interface with the fan control circuit 28. In some embodiments, the BIOS 27 may provide a signal to a hardware monitor circuit (HWM 34, e.g. a Heceta circuit) which may then interface with the fan control circuit 28.

**[0018]** With reference to Fig. 4, some embodiments of the invention involve a method to reduce fan noise during startup, including providing a fan configured to be controlled by a pulse width modulated (PWM) signal (e.g. at block 41), operating the fan in accordance with a first operating condition during startup (e.g. at block 42), and operating the fan in accordance with a second operating condition after startup (e.g. at block 43). For example, the first operating condition may correspond to a reduced fan noise during startup (e.g. at block 44). For example, operating the fan in accordance with the first operating condition may include operating the fan with a reduced fan speed

during startup (e.g. at block 45). In some embodiments, operating the fan with a reduced fan speed may include providing a reduced operating voltage to the fan during startup (e.g. at block 46).

**[0019]** Some embodiments may further involve receiving a signal  
5 indicating that the fan is ready to operate in accordance with the second operating condition (e.g. at block 47). For example, operating the fan in accordance with the second operating condition may include providing pulse width modulated (PWM) control signals to the fan (e.g. at block 48). Some  
10 embodiments of the invention may further involve providing a full operating voltage to the fan in response to the signal indicating that the fan is ready to operate in accordance with the second operating condition (e.g. at block 49).

**[0020]** With reference to Fig. 5, a block diagram of a processor-based system corresponds to an example of a desktop system board 50, also referred to as a motherboard, utilizing a noise management circuit in  
15 accordance with some embodiments of the invention. The noise management circuit may provide a solution for acoustic suppression of PWM fan noise during startup of an electronic system utilizing the desktop board (e.g. a personal computer (PC) or server system).

**[0021]** In some conventional personal computers, when the desktop board  
20 initially boots up, the PWM controlled fan for the CPU may throttle at full speed for a period of time (e.g. a few seconds) before the fan is controlled by the fan control circuit. The fan control circuit first needs to be initialized through the BIOS before it is able to generate the correct PWM signal to control the fan speed. This initial spin of the fan at full throttle may create an undesirable noise for the end user.

**[0022]** Advantageously, some embodiments of the present invention may prevent the PWM fan from operating at full speed before the BIOS initializes the fan control circuit. For example, some embodiments of the invention may switch the voltage supply for the fan to a lower operating voltage (e.g. 5V or even 3.3V) instead of the full operating voltage (e.g. typically 12V) before the POST is completed. The lower operating voltage may force the fan to spin at a reduced speed (e.g. half or lower of its maximum speed), thereby reducing the amount of fan noise during startup. After the POST is completed, when the BIOS has had a chance to execute the required code and complete the initialization of the fan control circuit, the BIOS can then cause a signal to be sent indicating that the PWM fan is ready to operate under PWM control. Upon receipt of the appropriate signal, the voltage supply for the fan may be switched back to the nominal full operating voltage. After startup, the fan control and the PWM fan may operate in the normal PWM controlled mode.

**[0023]** The desktop board 50 includes a processor 56 coupled to a graphics and memory controller hub (GMCH) which may be coupled to an I/O controller hub (ICH). The GMCH may support an AGP slot and memory access (e.g. either DDR or DIMMs). The ICH may support an SMBus, a low pin count (LPC) bus, primary and secondary IDE devices, a PCI bus (coupled to several PCI slots), and several USB ports. A hardware monitor circuit 58 may be coupled to the ICH over the SMBus. A firmware hub (FWH) may be coupled to the ICH over the LPC bus. A super I/O (SIO) circuit 57 may be coupled to the ICH over the LPC bus. For example, the SIO circuit 57 may be an LPC device that includes the keyboard, mouse, and floppy drive controllers, and the parallel and serial ports.

**[0024]** In some embodiments of an electronic system including the desktop board 50, the system further includes one or more fans 52 positioned to provide cooling for the desktop board 50 (and processor 56), wherein the fan(s) 52 are configured to be controlled by PWM signal(s) 53, and a fan startup circuit 54 configured to operate the fan(s) 52 in accordance with a first operating condition during startup and in accordance with a second operating condition after startup. For example, the first operating condition may correspond to a reduced fan noise during startup. For example, the fan startup circuit 54 may be configured to operate the fan(s) 52 with a reduced fan speed during startup. For example, the fan startup circuit 54 may be configured to provide a reduced operating voltage to the fan(s) 52 during startup.

**[0025]** In some embodiments, the fan startup circuit 54 may be configured to receive a signal 55 indicating that the fan is ready to operate in accordance with the second operating condition (e.g. from the SIO circuit 57). For example, the second operating condition may correspond to pulse width modulated operation by another fan control circuit (e.g. the hardware monitor circuit 58). For example, the fan startup circuit 54 may be configured to provide a full operating voltage to the fan(s) 52 in response to the signal 55 indicating that the fan(s) 52 are ready to operate in accordance with the second operating condition.

**[0026]** The desktop board 50 may further include a BIOS stored in non-volatile memory (e.g. a flash memory, a firmware hub, etc.). The BIOS may provide the typical instructions and operations for initializing the desktop board 50. The BIOS may further include instructions to cause the SIO circuit

57 to provide the signal 55 indicating that the fan(s) 52 are ready to operate in accordance with the second operating condition. For example, the BIOS may include instructions to cause the SIO circuit 57 to provide the signal 55 indicating that the fan(s) 52 are ready to operate in accordance with the  
5 second operating condition after a successful completion of a power on self test (POST).

**[0027]** For some desktop boards, the SIO circuit 57 may be implemented by a Port Angeles ASIC (e.g. part no. LPC47M172) available from Standard Microsystems Corporation (SMSC) or similar device from National  
10 Semiconductor (NS) and the hardware monitor circuit 58 may be implemented by a Heceta ASIC available from SMSC or Infineon, which may provide PWM fan control. For example, in some applications, the GPIO5 pin on the Port Angeles ASIC may be used to provide the signal 55 to the fan startup circuit 54 (e.g. the pin may be set by the BIOS following a successful POST).

15 **[0028]** With reference to Fig. 6, an example fan startup circuit 60 receives a signal 62 which indicates if a fan is ready to operate under a second operating condition. The signal 62 is provided directly to a second switch circuit S2 and is also inverted by an inverter 63. The inverted signal is provided to a first switch circuit S1. The first switch circuit S1 switches a first voltage V1 onto an output  
20 signal 64. The second switch circuit S2 switches a second voltage V2 onto the output signal 64. When the signal 62 is low (nominally 0V), the first switch S1 is closed and the voltage V1 is applied to the output signal 64. When the signal 62 is high (nominally 3.3V), the second switch circuit S2 is closed and the voltage V2 is applied to the output signal 64. Accordingly, the fan startup circuit 60 may be

configured to operate the fan in accordance with a first operating condition during startup (e.g. the first voltage V1) and in accordance with a second operating condition (e.g. the second voltage V2) after startup.

**[0029]** With reference to Fig. 7, another example fan startup circuit 70

5 includes an N-Type FET QN1 and a P-Type MOSFET QN2, both of which have their gates G coupled to a signal 72 which indicates if the fan(s) are ready to operate under PWM control. For example, during startup, the signal 72 may be low (nominally 0V) and after POST the signal 72 may be set high (nominally 3.3V). QN2 may be configured to provide a reduced operating voltage of VCC  
10 (nominally 5V) to pin 2 of a four pin fan header J1 (the output voltage 78 to the fan), while QN1 may be configured to provide the full operating voltage (nominally 12V) to pin 2 of the fan header J1. Fan control signal 74 may be provided to pin 1 (for 3 pin fans) of the fan header J1. Fan control signal 76 may be provided to pin 4 (for 4 pins fans) of the fan header J1. Pin 3 of the fan header J1 may provide an  
15 output signal to the HW monitor (e.g. a tach signal to the Heceta).

Advantageously, the fan startup circuit 70 may be added to many existing desktop board without major redesign or switching to linear DC fan control.

**[0030]** Another advantage of the fan startup circuit 70 is that the fan startup circuit 70 may be populated or de-populated as desired to bypass the fan startup  
20 circuit 70 (and support older designs). For example, to reduce fan noise during startup, the transistors QN1 and QN2 may be populated and the resistor R1 may be de-populated, such that 5V (nominally) is provided to pin 2 during startup and 12V is provided to pin 2 after the signal 72 is asserted. To support older designs, the two transistors QN1 and QN2 may be de-populated and the resistor R1 may

be populated, such that 12V is always provided to pin 2. For three pin fans, the resistor R2 and the transistor QN3 may be populated and the resistor R3 may be depopulated. For four pin fans, the resistor R3 may be populated and the resistor R2 and the transistor QN3 may be de-populated.

5   **[0031]**       Those skilled in the art will appreciate that, given the benefit of the present description, a numerous variety of other circuits and combinations of hardware and / or software may be configured to provide an appropriate fan startup circuits in accordance with other embodiments of the invention. The examples of Figs. 6 and 7 are non-limiting examples of suitable circuits.

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**[0032]**       The foregoing and other aspects of the invention are achieved individually and in combination. The invention should not be construed as requiring two or more of such aspects unless expressly required by a particular claim. Moreover, while the invention has been described in connection with what  
15 is presently considered to be the preferred examples, it is to be understood that the invention is not limited to the disclosed examples, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and the scope of the invention.

## CLAIMS

What is claimed is:

1. An apparatus, comprising:

5 a fan configured to be controlled by a pulse width modulated signal; and

a fan startup circuit coupled to the fan and configured to operate the fan in accordance with a first operating condition during startup and in accordance with a second operating condition after startup.

10

2. The apparatus of claim 1, wherein the first operating condition corresponds to a reduced fan noise during startup.

3. The apparatus of claim 2, wherein the fan startup circuit is  
15 configured to operate the fan with a reduced fan speed during startup.

4. The apparatus of claim 3, wherein the fan startup circuit is configured to provide a reduced operating voltage to the fan during startup.

20 5. The apparatus of claim 4, wherein the fan startup circuit is configured to receive a signal indicating that the fan is ready to operate in accordance with the second operating condition.

6. The apparatus of claim 5, wherein the second operating condition corresponds to a pulse width modulated operation by another fan control circuit.

5 7. The apparatus of claim 6, wherein the fan startup circuit is configured to provide a full operating voltage to the fan in response to the signal indicating that the fan is ready to operate in accordance with the second operating condition.

10 8. A method to reduce fan noise during startup, comprising:  
providing a fan configured to be controlled by a pulse width modulated signal;  
operating the fan in accordance with a first operating condition during startup; and  
15 operating the fan in accordance with a second operating condition after startup.

9. The method of claim 8, wherein the first operating condition corresponds to a reduced fan noise during startup.

20 10. The method of claim 9, wherein operating the fan in accordance with the first operating condition comprises:  
operating the fan with a reduced fan speed during startup.

11. The method of claim 10, wherein operating the fan with a reduced fan speed comprises:

providing a reduced operating voltage to the fan during startup.

5 12. The method of claim 11, further comprising:

receiving a signal indicating that the fan is ready to operate in accordance with the second operating condition.

10 13. The method of claim 12, wherein operating the fan in accordance with the second operating condition comprises:

providing pulse width modulated control signals to the fan.

14. The method of claim 13, further comprising:

15 providing a full operating voltage to the fan in response to the signal indicating that the fan is ready to operate in accordance with the second operating condition.

15. A system, comprising:

an electronic system board;

20 a fan positioned to provide cooling for the electronic system board, wherein the fan is configured to be controlled by pulse width modulated signal; and

a fan startup circuit configured to operate the fan in accordance with a first operating condition during startup and in accordance with a second operating condition after startup.

5           16.    The system of claim 15, wherein the first operating condition corresponds to a reduced fan noise during startup.

          17.    The system of claim 16, wherein the fan startup circuit is configured to operate the fan with a reduced fan speed during startup.

10

          18.    The system of claim 17, wherein the fan startup circuit is configured to provide a reduced operating voltage to the fan during startup.

          19.    The system of claim 18, wherein the fan startup circuit is  
15 configured to receive a signal indicating that the fan is ready to operate in accordance with the second operating condition.

          20.    The system of claim 19, wherein the second operating condition corresponds to pulse width modulated operation by another fan control circuit.

20

          21.    The system of claim 20, wherein the fan startup circuit is configured to provide a full operating voltage to the fan in response to the signal indicating that the fan is ready to operate in accordance with the second operating condition.

22. The system of claim 21, further comprising:  
a processor; and  
a basic input / output system (BIOS), wherein the BIOS provides  
5 the signal indicating that the fan is ready to operate in accordance with the  
second operating condition.

23. The system of claim 21, wherein the BIOS provides the signal  
indicating that the fan is ready to operate in accordance with the second  
10 operating condition after a successful completion of a power on self test  
(POST).

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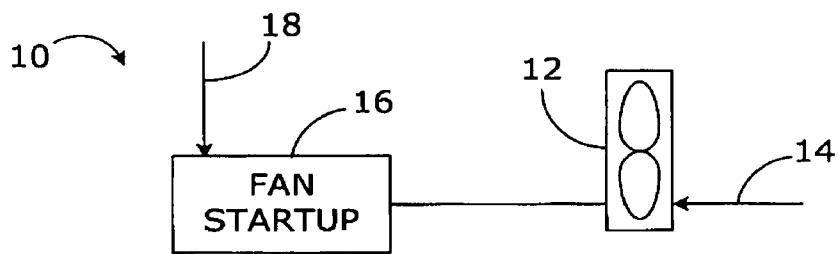


Fig. 1

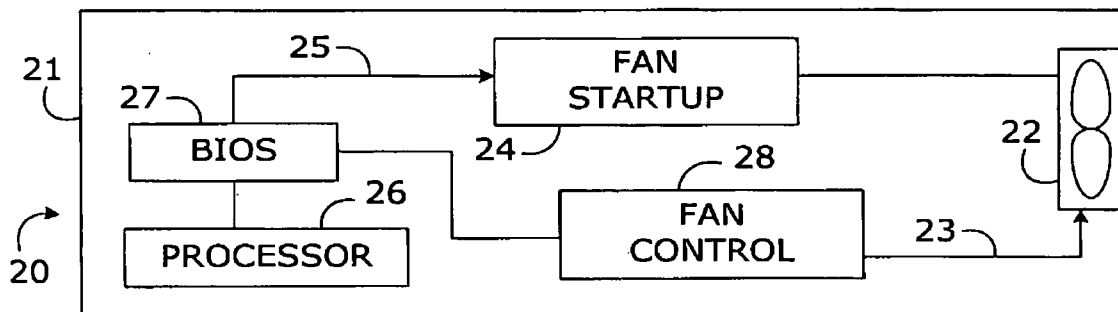


Fig. 2

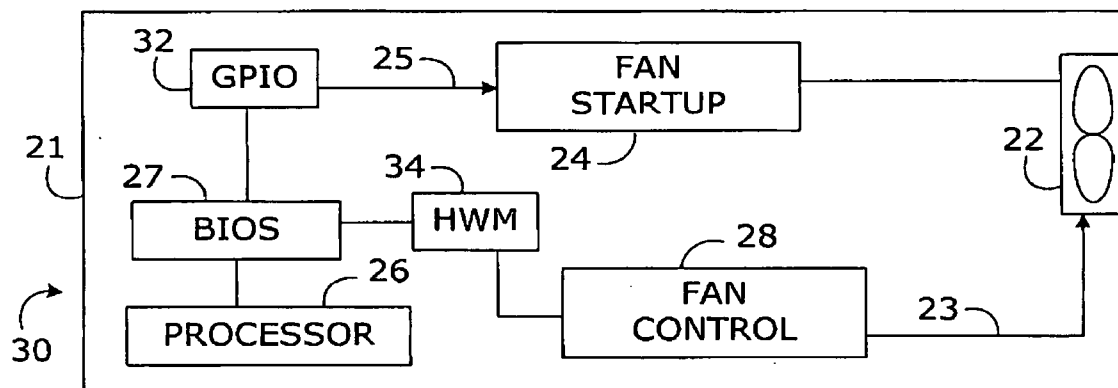


Fig. 3

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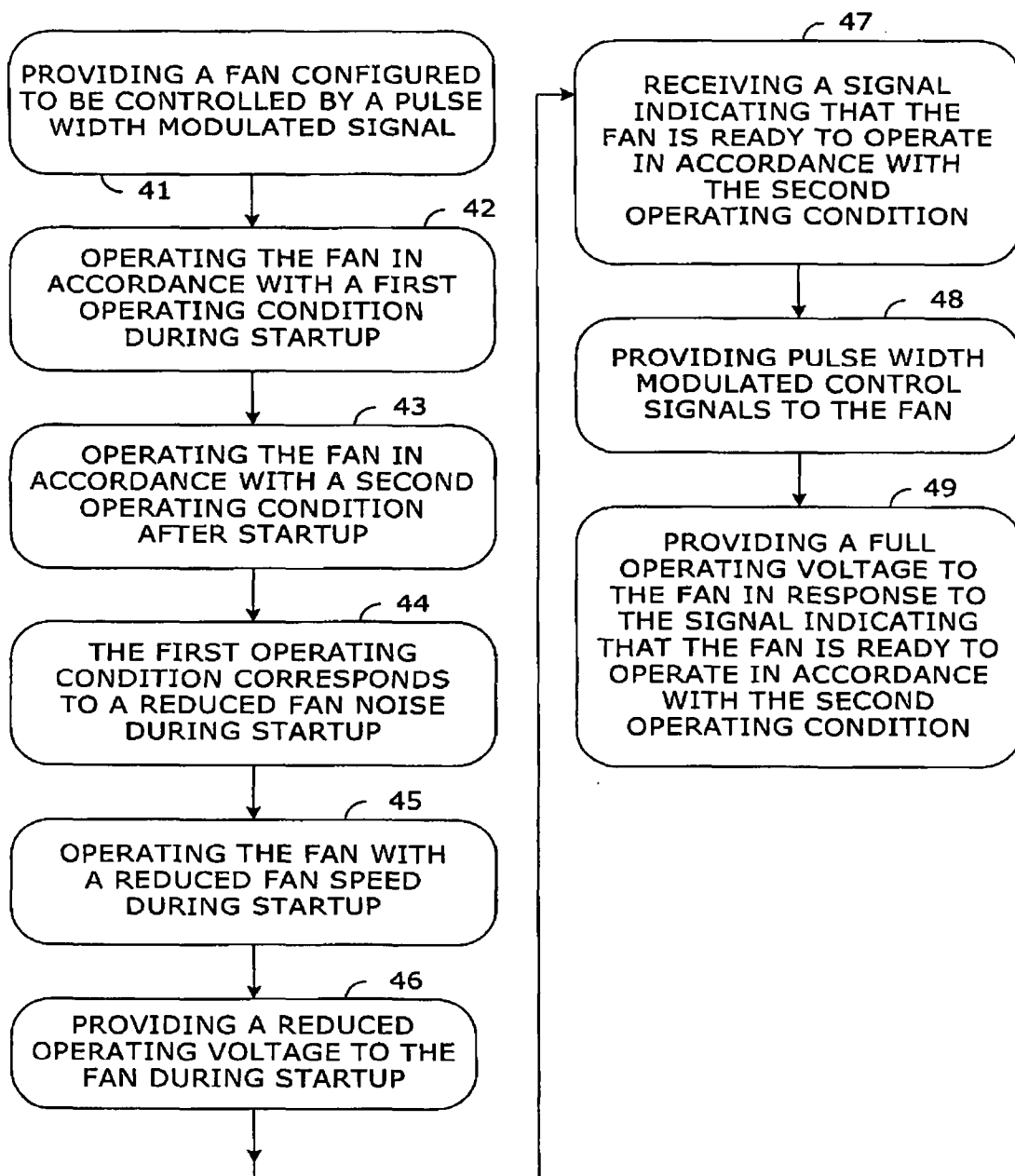


Fig. 4

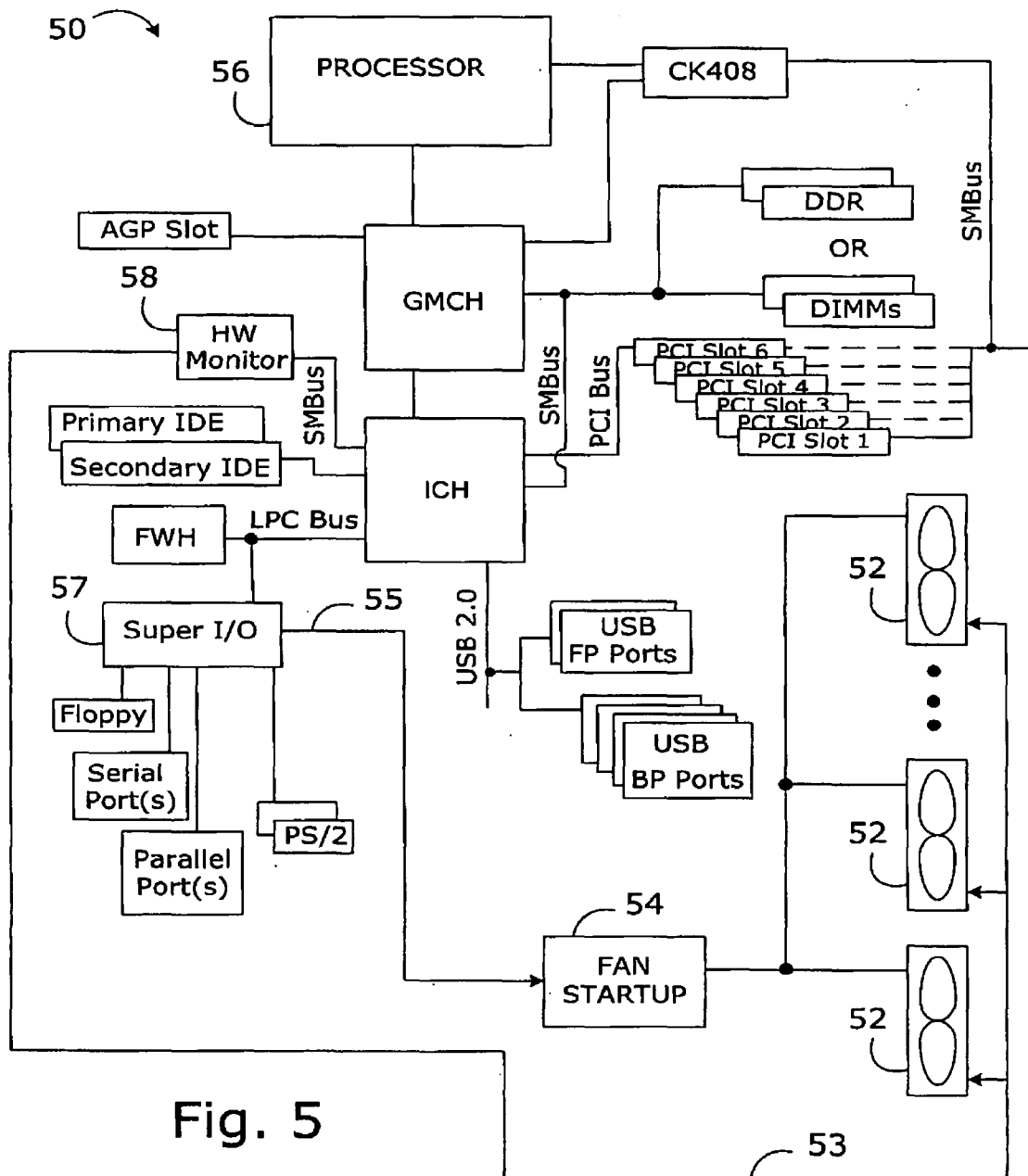


Fig. 5

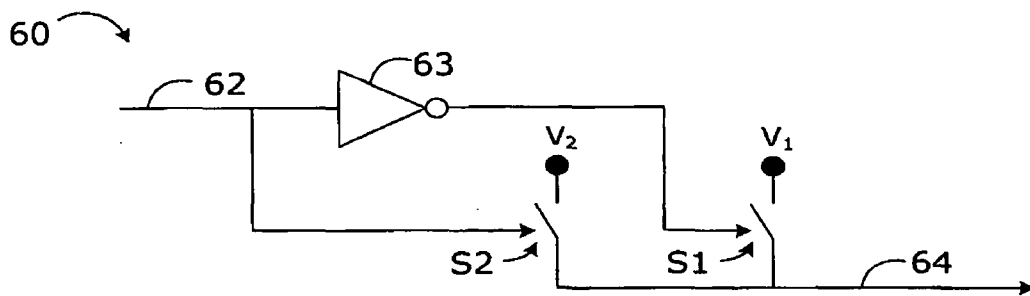


**Fig. 6**

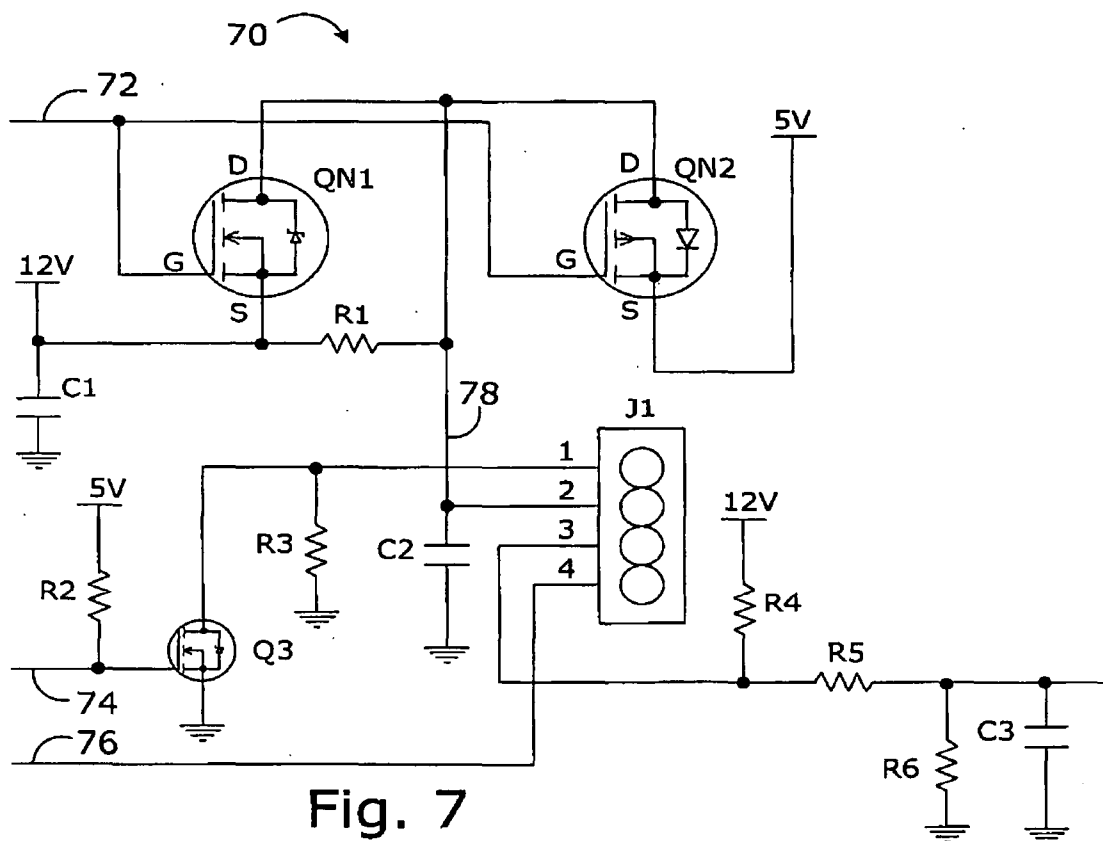


**Fig. 7**

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2007/070658****A. CLASSIFICATION OF SUBJECT MATTER****F04D 27/00(2006.01)i, H02P 27/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC8 : F04D 27/00, F04D 27/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models since 1975

Japanese utility models and applications for utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS (KIPO internal) &amp; keywords: "fan", "startup", "control", and "noise"

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                     | Relevant to claim No.    |
|-----------|--------------------------------------------------------------------------------------------------------|--------------------------|
| Y<br>A    | US 6779981 B2 (HUANG ET AL.) 24 August 2004<br>See figures 1- 6and column 6, line 5-column 7, line 10. | 1-5, 8-13<br>6, 7, 14-23 |
| Y<br>A    | JP 09-197922 A (RICOH CO., LTD.) 31 July 1997<br>See paragraphs 4-11.                                  | 1-5, 8-13<br>6, 7, 14-23 |
| Y<br>A    | JP 08-123298 A (CANON INC.) 17 May 1996<br>See paragraphs 21-31.                                       | 1-5, 8-13<br>6, 7, 14-23 |

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

28 SEPTEMBER 2007 (28.09.2007)

Date of mailing of the international search report

**28 SEPTEMBER 2007 (28.09.2007)**

Name and mailing address of the ISA/KR



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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2007/070658**Patent document  
cited in search reportPublication  
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