(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 December 2015 (30.12.2015)

(10) International Publication Number
WO 2015/199644 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2014/043683

(22) International Filing Date:
23 June 2014 (23.06.2014)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

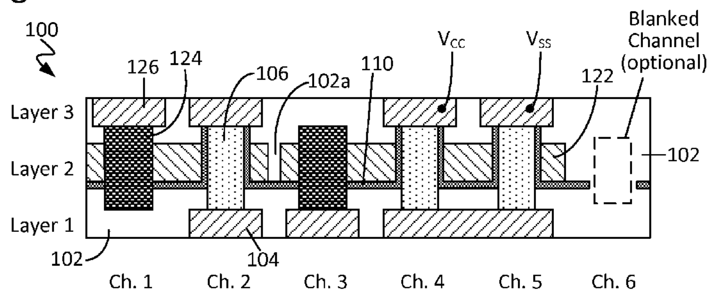
Declarations under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report (Art. 21(3))*

WO 2015/199644 A1

(54) Title: TECHNIQUES FOR FORMING VERTICAL TRANSISTOR ARCHITECTURES

Figure 1N



(57) Abstract: Techniques are disclosed for forming vertical transistor architectures. In accordance with some embodiments, a semiconductor layer is disposed over a lower interconnect layer and patterned into a plurality of vertical semiconductor bodies (e.g., nanowires and/or other three-dimensional semiconductor structures) in a regular, semi-regular, or irregular array, as desired for a given target application or end-use. Thereafter, a gate layer surrounding the active channel portion of each (or some sub-set) of the vertical semiconductor bodies is formed, followed by an upper interconnect layer, in accordance with some embodiments. During processing, a given vertical semiconductor body optionally may be removed and, in accordance with some embodiments, either: (1) blanked to provide a dummy channel; or (2) replaced with an electrically conductive plug to provide a via or other inter-layer routing. Processing can be performed in multiple iterations, for example, to provide multi-level/stacked vertical transistor circuit architectures of any standard and/or custom configuration.

TECHNIQUES FOR FORMING VERTICAL TRANSISTOR ARCHITECTURES

BACKGROUND

In a typical vertical transistor architecture, each conducting channel is provided by a silicon nanowire that is oriented perpendicularly with respect to the plane of an underlying semiconductor substrate. Each vertical channel is wrapped with a three-dimensional metal gate in a so-called gate-all-around (GAA) configuration, and source and drain contacts are electrically coupled with the ends of each vertical channel.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a cross-sectional view of an integrated circuit (IC) configured in accordance with an embodiment of the present disclosure.

Figure 1A′ illustrates a three-dimensional perspective view of the IC of Figure 1A.

Figure 1B is a cross-sectional view of the IC of Figure 1A after transfer of a semiconductor layer thereto, in accordance with an embodiment of the present disclosure.

Figure 1C is a cross-sectional view of the IC of Figure 1B after patterning the semiconductor layer, in accordance with an embodiment of the present disclosure.

Figure 1C′ illustrates a three-dimensional perspective view of the IC of Figure 1C.

Figure 1D is a cross-sectional view of the IC of Figure 1C after further formation of the dielectric layer or so-called inter-layer dielectric (ILD), in accordance with an embodiment of the present disclosure.

Figure 1E is a cross-sectional view of the IC of Figure 1D after formation of a second dielectric layer or so-called gate dielectric, in accordance with an embodiment of the present disclosure.

Figure 1E′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1E.

Figure 1F is a cross-sectional view of the IC of Figure 1E after further formation of the ILD and planarization, in accordance with an embodiment of the present disclosure.

Figure 1G is a cross-sectional view of the IC of Figure 1F after formation and patterning of a hardmask layer and patterning of the IC therewith, in accordance with an embodiment of the present disclosure.

Figure 1H is a cross-sectional view of the IC of Figure 1G after removal of the hardmask layer, further formation of the ILD, and planarization, in accordance with an embodiment of the present disclosure.

Figure 1H′ illustrates a three-dimensional perspective view of the IC of Figure 1H.

Figure 1I is a cross-sectional view of the IC of Figure 1H after formation and patterning of a second hardmask layer and patterning of the IC therewith, in accordance with an embodiment of the present disclosure.

Figure 1J is a cross-sectional view of the IC of Figure 1I after formation of a gate layer, 5 in accordance with an embodiment of the present disclosure.

Figure 1K is a cross-sectional view of the IC of Figure 1J after recessing the gate layer, in accordance with an embodiment of the present disclosure.

Figure 1K′ illustrates a three-dimensional perspective view of the IC of Figure 1K.

Figure 1L is a cross-sectional view of the IC of Figure 1K after patterning, in accordance 10 with an embodiment of the present disclosure.

Figure 1M is a cross-sectional view of the IC of Figure 1L after formation of one or more electrically conductive plugs, in accordance with an embodiment of the present disclosure.

Figure 1M′ illustrates a three-dimensional perspective view of the IC of Figure 1M.

Figure 1N is a cross-sectional view of the IC of Figure 1M after thinning, further 15 formation of the ILD and one or more interconnects, and planarization, in accordance with an embodiment of the present disclosure.

Figure 1N′ illustrates a three-dimensional perspective view of the IC of Figure 1N.

Figure 2 is a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure

20 Figure 3A is a cross-sectional view of an example IC configured in accordance with another embodiment of the present disclosure.

Figure 3B is a cross-sectional view of an example IC configured in accordance with another embodiment of the present disclosure.

Figure 4 illustrates a three-dimensional perspective view of an example inverter including 25 a single vertical semiconductor layer configured in accordance with an embodiment of the present disclosure.

Figure 5 illustrates a three-dimensional perspective view of an example inverter including two vertical semiconductor layers configured in accordance with another embodiment of the present disclosure.

30 Figure 6 illustrates a three-dimensional perspective view of an example NAND logic gate including two vertical semiconductor layers configured in accordance with an embodiment of the present disclosure.

Figure 7 illustrates a computing system implemented with integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines, right angles, etc., and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for forming vertical transistor architectures. In accordance with some embodiments, a semiconductor layer is disposed over a lower interconnect layer and then patterned into a plurality of vertical semiconductor bodies (e.g., nanowires and/or other three-dimensional semiconductor structures) in a regular, semi-regular, or irregular array, as desired for a given target application or end-use. Thereafter, a gate layer surrounding the active channel portion of each vertical semiconductor body of the array (or some sub-set thereof) is formed, followed by an upper interconnect layer, in accordance with some embodiments. During processing, a given vertical semiconductor body optionally may be removed and, in accordance with some embodiments, either: (1) blanked to provide a dummy channel; or (2) replaced with an electrically conductive plug to provide a via or other inter-layer routing. Processing can be performed in multiple iterations, for example, to provide multi-level/stacked vertical transistor architectures of any standard and/or custom configuration. In accordance with some embodiments, the techniques disclosed herein can be utilized, for example, in forming single vertical channel devices, as well as in special-purpose circuit fabrication (e.g., including multiple levels of semiconductor channels and routings, such as memory bitcell arrays or logic gates). Numerous configurations and variations will be apparent in light of this disclosure.

General Overview

Planar (horizontal channel) transistor devices face limitations with respect to scaling down in size and with respect to integration in microchips. Vertical transistor devices may provide a desirable alternative for next-generation microelectronics. However, vertical transistor architectures pose a variety of processing complications that existing integrated fabrication

methodologies do not adequately address or otherwise acknowledge. For instance, traditional vertical transistor architectures typically include at least three routing layers: (1) a lower source/drain layer below the vertical channel; (2) a gate at the same level as the vertical channel; and (3) an upper drain/source layer above the vertical channel. Given their positioning relative to one another, the lower routing layer in vertical transistor architectures is normally required to be fabricated prior to fabricating the vertical channel, and as such, existing bulk processing approaches generally are not compatible. Furthermore, as the gate in traditional horizontal channel devices is typically configured to serve as a local interconnect, it may be desirable to configure the gate of a vertical channel device to similarly serve as a local interconnect, for example, to provide for design compatibility between horizontal and vertical devices. However, given that the gate in a vertical transistor is located at the same level as the vertical channel, existing invasive processing approaches risk damage to the vertical channel device during formation.

Thus, and in accordance with some embodiments of the present disclosure, techniques are disclosed for forming vertical transistor architectures. In accordance with some embodiments, a semiconductor layer is disposed over a lower interconnect layer and then patterned into a plurality of vertical semiconductor bodies (e.g., nanowires and/or other three-dimensional semiconductor structures) in a regular, semi-regular, or irregular array, as desired for a given target application or end-use. Thereafter, a gate layer surrounding the active channel portion of each vertical semiconductor body of the array (or some sub-set thereof) is formed, followed by an upper interconnect layer, in accordance with some embodiments. During processing, a given vertical semiconductor body optionally may be removed and, in accordance with some embodiments, either: (1) blanked at that location to provide a dummy channel; or (2) replaced at that location with an electrically conductive plug to provide a via or other inter-layer routing. Processing can be performed in multiple iterations, for example, to provide multi-level/stacked vertical transistor architectures of any standard and/or custom configuration. In accordance with some embodiments, the techniques disclosed herein can be utilized, for example, in forming single vertical channel transistor devices, as well as in higher level circuits including multiple levels of semiconductor channels and routings, as desired.

In accordance with some embodiments, the disclosed techniques can be utilized, for example, to provide a given vertical channel device with any desired arrangement of electrical connections (e.g., source to gate; drain to gate; source to drain; source to gate to drain). In some cases, the disclosed techniques can be utilized, for example, to provide a vertical channel architecture including a gate layer configured, in accordance with an embodiment, to serve as a local interconnect for a host IC. In accordance with some embodiments, techniques disclosed

herein can be utilized, for example, in forming traditional as well as advanced vertical metal-oxide-semiconductor (MOS) devices, such as tunnel field-effect transistor (TFET) devices, quantum superlattices, and other heterostructures that typically exhibit sharp and precise construction. Use of the disclosed techniques may be detected, for example, by visual or other 5 inspection (e.g., microscope, etc.) of a given semiconductor architecture (or other IC) having one or more vertical transistor devices configured as described herein, in accordance with some embodiments.

Methodology and Structure

Figures 1A–1N illustrate an integrated circuit (IC) fabrication process flow, in 10 accordance with an embodiment of the present disclosure. As described herein, the disclosed process flow can be used to form any of a wide range of vertical channel architectures, such as, for example, a bit cell (e.g., as in Figures 1N and 2), a CMOS-like device (e.g., as in Figure 3A), a TFET-like device (e.g., as in Figure 3B), an inverter (e.g., as in Figures 4 and 5), and a NAND logic gate (e.g., as in Figure 6), each discussed in turn below. It should be noted, however, that 15 the present disclosure is not so limited only to these example structures/devices. Numerous vertical semiconductor channel architectures that can be formed, in part or in whole, using techniques disclosed herein will be apparent in light of this disclosure. Also, as discussed herein, the disclosed process flow can be used, in accordance with some embodiments, to provide a given vertical semiconductor channel architecture with any of a wide range of electrical 20 connections (e.g., source to gate; drain to gate; source to drain; source to gate to drain; etc.), as desired for a given target application or end-use.

The process may begin as in Figure 1A, which is a cross-sectional view of an integrated circuit (IC) 100 configured in accordance with an embodiment of the present disclosure. Figure 1A′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1A (with dielectric 25 layer 102 graphically omitted for ease of viewing). As can be seen, IC 100 initially may include a dielectric layer 102. In accordance with some embodiments, dielectric layer 102 can be formed, for example, on a substrate, wafer, or any other suitable surface, and in some cases may be formed as an inter-layer dielectric (ILD). Dielectric layer 102 can be formed from any suitable electrically insulating or dielectric material (or combination of such materials), using 30 any of a wide range of suitable techniques. For instance, in accordance with some embodiments, dielectric layer 102 may be formed from: (1) an oxide, such as silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), or a carbon (C)-doped oxide; (2) a nitride, such as silicon nitride (Si_3N_4); (3) a polymer, such as perfluorocyclobutane or polytetrafluoroethylene; (4) a phosphosilicate glass (PSG); (5) a fluorosilicate glass (FSG); (6) an organosilicate glass (OSG), such as silsesquioxane

or siloxane, carbosilane material (e.g., methyl- or ethyl-bridged silicates or carbosilane-ringed structures, such as 1,3,5-trisilacyclohexane derivatives); and/or (7) a combination of any one or more thereof. It should be noted, however, that the present disclosure is not so limited, as in a more general sense, and in accordance with some embodiments, dielectric layer 102 may be formed, in part or in whole, from any dielectric material (e.g., low-κ dielectric, high-κ dielectric, or otherwise), as desired for a given target application or end-use. In accordance with some embodiments, dielectric layer 102 may be formed, for example, using: (1) a physical vapor deposition (PVD) process; (2) a chemical vapor deposition (CVD) process, such as plasma-enhanced CVD (PECVD); (3) a spin-on deposition (SOD) process; and/or (4) a combination of any one or more thereof. Other suitable materials and techniques for forming dielectric layer 102 will depend on a given application and will be apparent in light of this disclosure.

As can be seen further from Figure 1A, dielectric layer 102 may have one or more electrical interconnects 104 (e.g., a lower routing layer) formed therein. The geometry of a given interconnect 104 can be customized (e.g., polygonal, curvilinear, or any other geometric shape), as desired for a given target application or end-use, and in accordance with some example embodiments, may be: (1) a single-damascene interconnect structure (e.g., a trench; a via); (2) a dual-damascene interconnect structure (e.g., a trench with an underlying via); (3) an anisotropic interconnect structure; and/or (4) an isotropic interconnect structure. Numerous suitable configurations for interconnect(s) 104 will be apparent in light of this disclosure.

A given interconnect 104 may be formed from any suitable electrically conductive material (or combination of such materials), using any of a wide range of suitable techniques. For example, in accordance with some embodiments, a given interconnect 104 may be formed from: (1) tungsten (W); (2) copper (Cu); (3) cobalt (Co); (4) molybdenum (Mo); (5) rhodium (Rh); (6) beryllium (Be); (7) chromium (Cr); (8) manganese (Mn); (9) aluminum (Al); (10) ruthenium (Ru); (11) palladium (Pd); (12) nickel (Ni); (13) cobalt tungsten phosphide (CoWP); (14) cobalt tungsten boron (CoWB); (15) copper germanium (CuGe); (16) silicon (Si); and/or (17) an alloy or other combination of any one or more thereof. In accordance with some embodiments, interconnect(s) 104 may be formed, for example, using: (1) an electroplating process; (2) an electroless deposition process; (3) a chemical vapor deposition (CVD) process; and/or (4) a combination of any one or more thereof. Other suitable materials and techniques for forming a given interconnect 104 will depend on a given application and will be apparent in light of this disclosure.

After formation of interconnect(s) 104, it may be desirable in some instances to planarize IC 100, for example, to remove any undesired excess (e.g., overburden) of: (1) a given interconnect 104; and/or (2) dielectric layer 102. To that end, IC 100 may undergo a chemical-

mechanical planarization (CMP) process, an etch-and-clean process, and/or any other suitable planarization/polish process, as will be apparent in light of this disclosure. In some cases, after planarization, dielectric layer 102 and interconnect(s) 104 may have a thickness, for example, in the range of about 10–50 nm (e.g., about 10–30 nm, about 30–50 nm, or any other sub-range in
5 the range of about 10–50 nm). However, the dimensions of dielectric layer 102 and/or a given interconnect 104 are not so limited only to this example range, as in a more general sense, and in accordance with some embodiments, the dimensions of dielectric layer 102 and interconnect(s) 104 can be customized, as desired for a given target application or end-use. Also, as will be appreciated in light of this disclosure, the dimensions of dielectric layer 102 and/or the one or
10 more interconnects 104 may change (e.g., may increase and/or decrease) during processing, as described herein. In some cases, dielectric layer 102 and/or a given interconnect 104 may have a substantially uniform thickness over the topography provided, for example, by any underlying layers of IC 100 (e.g., a substrate, wafer, or any other suitable surface). In some other instances, however, dielectric layer 102 and/or a given interconnect 104 may be provided with a non-
15 uniform or otherwise varying thickness over such topography. For example, in some cases a first portion of dielectric layer 102 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. In some cases, a first portion of a given interconnect 104 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable dimensions for dielectric layer 102 and
20 interconnect(s) 104 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 1B, which is a cross-sectional view of the IC 100 of Figure 1A after transfer of a semiconductor layer 106 thereto, in accordance with an embodiment of the present disclosure. Semiconductor layer 106 can be formed from any
25 suitable semiconductor material (or combination of such materials), using any of a wide range of suitable techniques. For example, in accordance with some embodiments, semiconductor layer 106 may be formed from: (1) silicon (Si); (2) germanium (Ge); (3) silicon germanium (SiGe); (4) a III-V compound, such as gallium arsenide (GaAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), or indium phosphide (InP); and/or (5) a combination of any one or more thereof.
30 In accordance with some embodiments, semiconductor layer 106 may be provided over IC 100 using a blanket semiconductor transfer process, such as, for example: (1) an ion-cut process; (2) an amorphous layer blister process; (3) a strain-induced spalling process; (4) a backside grinding process; and/or (5) a combination of any one or more thereof. Other suitable materials and techniques for providing semiconductor layer 106 over IC 100 will depend on a given
35 application and will be apparent in light of this disclosure.

Furthermore, the dimensions of semiconductor layer 106 can be customized, as desired for a given target application or end-use, and in some instances may be selected, in part or in whole, based on the desired channel length for IC 100. In accordance with some embodiments, semiconductor layer 106 may have a thickness, for example, in the range of about 10–100 nm (e.g., about 10–50 nm, about 50–100 nm, or any other sub-range in the range of about 10–100 nm). In some cases, semiconductor layer 106 may have a substantially uniform thickness over the topography provided, for example, by any underlying layers of IC 100 (e.g., dielectric layer 102; a given interconnect 104). In some instances, semiconductor layer 106 may be provided as a substantially conformal layer over such topography. In some other instances, however, semiconductor layer 106 may be provided with a non-uniform or otherwise varying thickness over such topography. For example, in some cases a first portion of semiconductor layer 106 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable dimensions for semiconductor layer 106 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 1C, which is a cross-sectional view of the IC 100 of Figure 1B after patterning semiconductor layer 106, in accordance with an embodiment of the present disclosure. Figure 1C′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1C (with dielectric layer 102 graphically omitted for ease of viewing). As can be seen, semiconductor layer 106 may be patterned into one or more semiconductor bodies 106 (e.g., nanowires and/or other three-dimensional semiconductor structures). To that end, any suitable lithographic patterning technique (or combination of such techniques) may be utilized. For example, in accordance with some embodiments, the one or more semiconductor bodies 106 may be patterned using: (1) an immersion lithography process; (2) an electron-beam (e-beam) lithography process; (3) an extreme ultraviolet (EUV) lithography process; and/or (4) a combination of any one or more thereof. It should be noted that, in accordance with some embodiments, semiconductor layer 106 may be patterned to form not only semiconductor bodies 106 which ultimately will serve as the one or more semiconductor channels of IC 100, but also semiconductor bodies 106 which ultimately will be removed and replaced at such locations with dummies and/or vias for IC 100 (as described herein). Other suitable techniques for patterning semiconductor layer 106 into one or more semiconductor bodies 106 will depend on a given application and will be apparent in light of this disclosure.

The geometry, dimensions, spacing, and arrangement of the one or more semiconductor bodies 106 (e.g., nanowires and/or other three-dimensional semiconductor structures) formed from semiconductor layer 106 can be customized, as desired for a given target application or end-use, and in some cases may be selected, in part or in whole, based on the desired

semiconductor channel performance for a given host IC 100. In some instances, a given semiconductor body 106 may be generally cylindrical in shape, having a circular, elliptical, or other curvilinear cross-sectional profile, whereas in some other instances, a given semiconductor body 106 may be generally prismatic in shape, having a square, rectangular, hexagonal, or other polygonal cross-sectional profile. In some cases, a given semiconductor body 106 may have a width/diameter (D_1), for example, in the range of about 1–20 nm (e.g., about 1–5 nm, about 5–10 nm, about 10–15 nm, about 15–20 nm, or any other sub-range in the range of about 1–20 nm). In some cases, a given semiconductor body 106 may have a height/length (D_2), for example, in the range of about 10–100 nm (e.g., about 10–25 nm, about 25–50 nm, about 50–100 nm, or any other sub-range in the range of about 10–100 nm). In some instances, semiconductor layer 106 may be patterned into a regular array of semiconductor bodies 106 (e.g., nanowires and/or other three-dimensional semiconductor structures), in which all or nearly all of the bodies 106 are arranged in a systematic manner in relation to one another. In some other instances, semiconductor layer 106 may be patterned into a semi-regular array of semiconductor bodies 106 (e.g., nanowires and/or other three-dimensional semiconductor structures), in which a sub-set of the bodies 106 are arranged in a systematic manner in relation to one another, but at least one other body 106 is not so arranged. In some still other instances, semiconductor layer 106 may be patterned into an irregular array of semiconductor bodies 106 (e.g., nanowires and/or other three-dimensional semiconductor structures), in which the bodies 106 are not arranged in a systematic manner in relation to one another. In some cases, neighboring semiconductor bodies 106 may be substantially equidistantly spaced from one another (e.g., may exhibit a substantially constant spacing). In some other cases, however, the spacing of the one or more semiconductor bodies 106 may be varied, as desired. In some example cases, neighboring semiconductor bodies 106 may be separated from one another by a distance in the range of about 5–50 nm (e.g., about 5–25 nm, about 25–50 nm, or any other sub-range in the range of about 5–50 nm). Other suitable geometries, dimensions, spacing, and arrangements for the one or more semiconductor bodies 106 (e.g., nanowires and/or other three-dimensional semiconductor structures) of IC 100 will be apparent in light of this disclosure.

The process may continue as in Figure 1D, which is a cross-sectional view of the IC 100 of Figure 1C after further formation of dielectric layer 102, in accordance with an embodiment of the present disclosure. As can be seen, IC 100 may undergo further formation of dielectric layer 102, for example, within the interstitial space(s) between the one or more semiconductor bodies 106. To that end, dielectric layer 102 may be further formed using any suitable technique (or combination of techniques), such as those discussed above, for instance, with respect to Figure 1A. As dielectric layer 102 is further formed, it may extend up a sidewall portion of a

given semiconductor body 106 by a distance (D_3), for example, in the range of about 1–10 nm (e.g., about 1–5 nm, about 5–10 nm, or any other sub-range in the range of about 1–10 nm). It should be noted, however, that the present disclosure is not so limited only to this example range, as in a more general sense, and in accordance with some embodiments, the amount by which IC 100 is further filled with dielectric layer 102 may be customized, as desired for a given target application or end-use.

The process may continue as in Figure 1E, which is a cross-sectional view of the IC 100 of Figure 1D after formation of a dielectric layer 110, in accordance with an embodiment of the present disclosure. Figure 1E′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1E (with dielectric layer 102 graphically omitted and dielectric layer 110 partially graphically omitted for ease of viewing). Dielectric layer 110 can be formed from any suitable dielectric material (or combination of such materials), using any of a wide range of suitable techniques. For example, in accordance with some embodiments, dielectric layer 110 may be formed from: (1) hafnium oxide (HfO_2); (2) zirconium dioxide (ZrO_2); (3) tantalum pentoxide (Ta_2O_5); (4) silicon dioxide (SiO_2); (5) aluminum oxide (Al_2O_3); (6) titanium dioxide (TiO_2); (7) lanthanum oxide (La_2O_3); (8) hafnium silicate ($HfSiO_4$); (9) zirconium silicate ($ZrSiO_4$); (10) strontium titanate ($SrTiO_3$); and/or (11) a combination of any one or more thereof. It should be noted, however, that the present disclosure is not so limited, as in a more general sense, and in accordance with some embodiments, dielectric layer 110 may be formed, in part or in whole, from any dielectric material (e.g., low-κ dielectric, high-κ dielectric, or otherwise), as desired for a given target application or end-use. In accordance with some embodiments, dielectric layer 110 may be formed, for example, using: (1) a chemical vapor deposition (CVD) process, such as plasma-enhanced CVD (PECVD); (2) an atomic layer deposition (ALD) process; and/or (3) a combination of any one or more thereof. Other suitable materials and techniques for forming dielectric layer 110 will depend on a given application and will be apparent in light of this disclosure.

Furthermore, the dimensions of dielectric layer 110 can be customized, as desired for a given target application or end-use. In accordance with some embodiments, dielectric layer 110 may have a thickness, for example, in the range of about 1–10 nm (e.g., about 1–2.5 nm, about 2.5–5 nm, about 5–7.5 nm, about 7.5–10 nm, or any other sub-range in the range of about 1–10 nm). In some instances, dielectric layer 110 may have a substantially uniform thickness over the topography provided, for example, by any underlying layers of IC 100 (e.g., the one or more semiconductor bodies 106; dielectric layer 102). In some instances, dielectric layer 110 may be provided as a substantially conformal layer over such topography. In some other instances, however, dielectric layer 110 may be provided with a non-uniform or otherwise varying

thickness over such topography. For example, in some cases a first portion of dielectric layer 110 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable dimensions for dielectric layer 110 will depend on a given application and will be apparent in light of this disclosure.

5 The process may continue as in Figure 1F, which is a cross-sectional view of the IC 100 of Figure 1E after further formation of dielectric layer 102 and planarization, in accordance with an embodiment of the present disclosure. As can be seen, IC 100 may undergo further formation of dielectric layer 102, for example, within the interstitial space(s) between the one or more semiconductor bodies 106 and attendant portion(s) of dielectric layer 110. To that end, dielectric 10 layer 102 may be further formed using any suitable technique (or combination of techniques), such as those discussed above, for instance, with respect to Figure 1A. As dielectric layer 102 is further formed, it may extend over an upper surface of dielectric layer 110 (or otherwise over an upper portion of a given semiconductor body 106). After this further formation of dielectric layer 102, it may be desirable in some instances to planarize IC 100, for example, to remove any 15 undesired excess (e.g., overburden) thereof. To that end, IC 100 may undergo any suitable planarization/polish process, such as those discussed above, for instance, with respect to Figure 1A. In some cases, through planarization, the thickness of dielectric layer 102 may be reduced so as to make an upper surface of dielectric layer 102 substantially flush (e.g., precisely flush or otherwise within a given tolerance) with an upper surface of dielectric layer 110 (or an upper 20 surface of a given semiconductor body 106), such as can be seen generally from Figure 1F. However, the present disclosure is not so limited, as in a more general sense, and in accordance with some embodiments, dielectric layer 102 may be reduced to any given thickness, as desired for a given target application or end-use. Numerous suitable configurations will be apparent in light of this disclosure.

25 The process may continue as in Figure 1G, which is a cross-sectional view of the IC 100 of Figure 1F after formation and patterning of a hardmask layer 114 and patterning of IC 100 therewith, in accordance with an embodiment of the present disclosure. Hardmask layer 114 can be formed from any suitable hardmask material (or combination of such materials), using any of a wide range of suitable techniques. For example, in accordance with some embodiments, 30 hardmask layer 114 may be formed from: (1) a highly carbon (C)-containing hardmask (e.g., having a carbon content greater than or equal to about 40% by weight); (2) silicon dioxide (SiO_2); (3) silicon nitride (Si_3N_4); (4) silicon oxynitride (SiO_xN_y); and/or (5) a combination of any one or more thereof. In accordance with some embodiments, hardmask layer 114 may be formed using: (1) a physical vapor deposition (PVD) process, such as sputter deposition; (2) a 35 chemical vapor deposition (CVD) process, such as plasma-enhanced CVD (PECVD); (3) a spin-

on deposition (SOD) process; (4) an atomic layer deposition (ALD) process; and/or (5) a combination of any one or more thereof. Other suitable materials and techniques for forming hardmask layer 114 will depend on a given application and will be apparent in light of this disclosure.

5 Furthermore, the dimensions of hardmask layer 114 can be customized, as desired for a given target application or end-use. In accordance with some embodiments, hardmask layer 114 may have a thickness, for example, in the range of about 1–30 nm (e.g., about 1–10 nm, about 10–20 nm, about 20–30 nm, or any other sub-range in the range of about 1–30 nm). In some instances, hardmask layer 114 may have a substantially uniform thickness over the topography 10 provided, for example, by any underlying layers of IC 100 (e.g., dielectric layer 110; a given semiconductor body 106; dielectric layer 102). In some instances, hardmask layer 114 may be provided as a substantially conformal layer over such topography. In some other instances, however, hardmask layer 114 may be provided with a non-uniform or otherwise varying thickness over such topography. For example, in some cases a first portion of hardmask layer 15 114 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable dimensions for hardmask layer 114 will be apparent in light of this disclosure.

After formation thereof, hardmask layer 114 may undergo patterning using any suitable lithographic patterning technique (or combination of such techniques), such as those discussed 20 above, for instance, with respect to forming semiconductor bodies 106. In accordance with some embodiments, hardmask layer 114 may be patterned, for example, to reveal one or more channels of IC 100 that are to be optionally blanked (e.g., selectively etched out or otherwise removed from IC 100 and replaced at such location with additional material for dielectric layer 102, as discussed below). Thereafter, the process may continue with utilizing the patterned 25 hardmask layer 114 as a mask and etching out one or more semiconductor bodies 106 (and associated portions of dielectric layer 110, if present) and into dielectric layer 102, forming one or more openings 116 in IC 100, as generally can be seen from Figure 1G. To that end, IC 100 may be patterned, in accordance with some embodiments, using a dry etching process and/or a wet etching process. In some instances, an anisotropic plasma etching process may be 30 employed. Also, in accordance with some embodiments, the etch chemistry for etching IC 100 can be customized, as desired, and in some instances may be selective to etching the material(s) of semiconductor bodies 106 and/or dielectric layer 110 as compared to the material(s) of hardmask layer 114 and/or dielectric layer 102. Furthermore, the geometry and dimensions of a given opening 116 (and thus of a given optional blanked region of IC 100) can be customized, as 35 desired for a given target application or end-use, and in some instances may depend, at least in

part, on the type of etch process and/or etch chemistry utilized. Other suitable techniques for patterning IC 100 with one or more openings 116 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 1H, which is a cross-sectional view of the IC 100 of Figure 1G after removal of hardmask layer 114, further formation of dielectric layer 102, and planarization, in accordance with an embodiment of the present disclosure. Figure 1H′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1H (with dielectric layer 102 graphically omitted and dielectric layer 110 partially graphically omitted for ease of viewing). Hardmask layer 114 can be removed from IC 100 using any suitable planarization/polish process, cleans, etc., as typically done. In some instances in which hardmask layer 114 is a highly carbon (C)-containing hardmask (e.g., having a carbon content greater than or equal to about 40% by weight), an oxygen (O_2)-based plasma ashing and clean process may be utilized, in accordance with some embodiments. Other suitable techniques for removing hardmask layer 114 will depend on a given application and will be apparent in light of this disclosure.

After removing hardmask layer 114, IC 100 may undergo further formation of dielectric layer 102, for example, to fill a given opening 116 to optionally blank a given channel of IC 100, in accordance with some embodiments. To that end, dielectric layer 102 may be further formed using any suitable technique (or combination of techniques), such as those discussed above, for instance, with respect to Figure 1A. As dielectric layer 102 is further formed, it may extend over an upper surface of dielectric layer 110 (or otherwise over an upper portion of a given semiconductor body 106). After this further formation of dielectric layer 102, it may be desirable in some instances to planarize IC 100, for example, to remove any undesired excess (e.g., overburden) thereof. To that end, IC 100 may undergo any suitable planarization/polish process, such as those discussed above, for instance, with respect to Figure 1A. In some cases, through planarization, the thickness of dielectric layer 102 may be reduced so as to make an upper surface of dielectric layer 102 substantially flush (e.g., precisely flush or otherwise within a given tolerance) with an upper surface of dielectric layer 110 (or an upper surface of a given semiconductor body 106), such as can be seen generally from Figure 1H. However, the present disclosure is not so limited, as in a more general sense, and in accordance with some embodiments, dielectric layer 102 may be reduced to any given thickness, as desired for a given target application or end-use. Numerous suitable configurations will be apparent in light of this disclosure.

The process may continue as in Figure 1I, which is a cross-sectional view of the IC 100 of Figure 1H after formation and patterning of a hardmask layer 118 and patterning of IC 100 therewith, in accordance with an embodiment of the present disclosure. Hardmask layer 118 can

be formed from any suitable hardmask material (or combination of materials), using any of a wide range of suitable techniques, and in some cases may be formed using any of the example materials and example techniques discussed above, for instance, with respect to hardmask layer 114. Furthermore, the dimensions of hardmask layer 118 can be customized, as desired for a given target application or end-use, and in some cases may be substantially similar to those discussed above, for instance, with respect to hardmask layer 114. In some instances, hardmask layer 118 may have a substantially uniform thickness over the topography provided, for example, by any underlying layers of IC 100 (e.g., dielectric layer 102; dielectric layer 110; a given semiconductor body 106). In some instances, hardmask layer 118 may be provided as a substantially conformal layer over such topography. In some other instances, however, hardmask layer 118 may be provided with a non-uniform or otherwise varying thickness over such topography. For example, in some cases a first portion of hardmask layer 118 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable material, dimensions, and techniques for forming hardmask layer 118 will depend on a given application and will be apparent in light of this disclosure.

After formation thereof, hardmask layer 118 may undergo patterning using any suitable lithographic patterning technique (or combination of such techniques), such as those discussed above, for instance, with respect to forming semiconductor bodies 106. In accordance with some embodiments, hardmask layer 118 may be patterned, for example, to protect one or more portions of underlying dielectric layer 102 (e.g., the one or more optionally blanked channels of IC 100, as discussed above; one or more separator portions 102a, as generally shown in Figure 1I). Thereafter, the process may continue with utilizing the patterned hardmask layer 118 as a mask and etching out a portion of dielectric layer 102 to provide a gate trench 120 in IC 100, as generally can be seen from Figure 1I. To that end, IC 100 may be patterned, in accordance with some embodiments, using a dry etching process and/or a wet etching process. In some instances, an anisotropic plasma etching process may be employed. Also, in accordance with some embodiments, the etch chemistry for etching IC 100 can be customized, as desired, and in some instances may be selective to etching the material(s) of dielectric layer 102 as compared to the material(s) of hardmask layer 118, dielectric layer 110, and/or semiconductor bodies 106. Furthermore, the geometry and dimensions of a gate trench 120 can be customized, as desired for a given target application or end-use, and in some instances may depend, at least in part, on the type of etch process and/or etch chemistry utilized. In some cases, dielectric layer 102 may be etched out until underlying dielectric layer 110 is reached. Other suitable techniques for patterning IC 100 with gate trench 120 will depend on a given application and will be apparent in light of this disclosure.

After patterning gate trench 120, the process may continue with removing hardmask layer 118 from IC 100. To that end, any suitable planarization/polish process, cleans, etc., as typically done, may be utilized. In some cases, a plasma ashing and clean process (e.g., such as that discussed above with respect to hardmask layer 114) may be utilized. Other suitable techniques
5 for removing hardmask layer 118 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 1J, which is a cross-sectional view of the IC 100 of Figure 1I after formation of a gate layer 122, in accordance with an embodiment of the present disclosure. In accordance with some embodiments, gate layer 122 may be configured to serve
10 not only as a gate for one or more vertical transistors of IC 100, but also as a local interconnect within IC 100. Gate layer 122 can be formed from any suitable gate material (or combination of such materials), using any of a wide range of suitable techniques. For example, in accordance with some embodiments, gate layer 122 may be formed from: (1) tungsten (W); (2) aluminum (Al); (3) titanium (Ti); (4) titanium nitride (TiN); (5) polysilicon (doped or undoped); and/or (6)
15 an alloy or other combination of any one or more thereof. In accordance with some embodiments, IC 100 may be globally filled with a gate layer 122 of any desired initial thickness, and in some cases, gate layer 122 may be formed with sufficient initial thickness, for example, so as to extend out of gate trench 120 and over an upper surface of dielectric layer 110 and/or dielectric layer 102 (e.g., as can be seen generally from Figure 1J). To that end, gate layer
20 122 may be formed, in accordance with some embodiments, using: (1) a physical vapor deposition (PVD) process; (2) a chemical vapor deposition (CVD) process; (3) an electroplating process; (4) an electroless deposition process; and/or (5) a combination of any one or more thereof. Other suitable materials and techniques for forming gate layer 122 will depend on a given application and will be apparent in light of this disclosure.

25 The process may continue as in Figure 1K, which is a cross-sectional view of the IC 100 of Figure 1J after recessing gate layer 122, in accordance with an embodiment of the present disclosure. Figure 1K′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1K (with dielectric layer 102 graphically omitted and dielectric layer 110 partially graphically omitted for ease of viewing). In accordance with some embodiments, gate layer 122 may be
30 recessed to remove excess thereof from IC 100 to achieve a given desired gate thickness. To that end, gate layer 122 may undergo: (1) any suitable planarization/polish process, such as those discussed above, for instance, with respect to Figure 1A; and/or (2) any suitable dry etching process and/or wet etching process. The dimensions of gate layer 122 may be customized, as desired for a given target application or end-use, and in some cases may be selected, at least in
35 part, based on the desired active semiconductor channel length of a given host IC 100. In

accordance with some embodiments, gate layer 122 may have a thickness (after recessing), for example, in the range of about 10–30 nm (e.g., about 10–20 nm, about 20–30 nm, or any other sub-range in the range of about 10–30 nm). In some instances, gate layer 122 may have a substantially uniform thickness over the topography provided, for example, by any underlying layers of IC 100 (e.g., portions of dielectric layer 110 within gate trench 120). In some other instances, however, gate layer 122 may be provided with a non-uniform or otherwise varying thickness over such topography. For example, in some cases a first portion of gate layer 122 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable dimensions for gate layer 122 will depend on a given application and will be apparent in light of this disclosure.

As can be seen, the resultant gate layer 122 may be configured, in accordance with some embodiments, to surround the active channel portion of each vertical semiconductor body 106 (or some sub-set thereof), as desired. In some cases, the presence of a given separator portion 102a of dielectric layer 102 may facilitate designation of sub-sets of bodies 106 for IC 100. In some cases, gate layer 122 may be a continuous layer, whereas in some other cases, gate layer 122 may have one or more regions of discontinuity (e.g., gaps), such as where a separator portion 102a resides and/or where a blanked channel is optionally formed (e.g., as generally shown in Figure 1K). As can be seen further, after recessing gate layer 122 to achieve a given desired gate thickness, IC 100 may undergo further formation of dielectric layer 102, for example, within the interstitial space(s) over gate layer 122 between the one or more semiconductor bodies 106 and attendant dielectric layer 110. To that end, dielectric layer 102 may be further formed using any suitable technique (or combination of techniques), such as those discussed above, for instance, with respect to Figure 1A. As dielectric layer 102 is further formed, it may come to join with a given separator portion 102a of IC 100, if present. Also, as dielectric layer 102 is further formed, it may extend over an upper surface of dielectric layer 110 over a given semiconductor body 106. After this further formation of dielectric layer 102, it may be desirable in some instances to planarize IC 100, for example, to remove any undesired excess (e.g., overburden) thereof. To that end, IC 100 may undergo any suitable planarization/polish process, such as those discussed above, for instance, with respect to Figure 1A. In some cases, through planarization, the thickness of dielectric layer 102 may be reduced so as to make an upper surface of dielectric layer 102 substantially flush (e.g., precisely flush or otherwise within a given tolerance) with an upper surface of dielectric layer 110 over a given semiconductor body 106, such as can be seen generally from Figure 1K. However, the present disclosure is not so limited, as in a more general sense, and in accordance with some embodiments, dielectric layer

102 may be reduced to any given thickness, as desired for a given target application or end-use. Numerous suitable configurations will be apparent in light of this disclosure.

The process may continue as in Figure 1L, which is a cross-sectional view of the IC 100 of Figure 1K after patterning, in accordance with an embodiment of the present disclosure. As can be seen, one or more channels of IC 100 may be selectively etched out (or otherwise removed) and replaced, for example, with one or more electrically conductive plugs 124, as discussed below with respect to Figure 1M. In particular, one or more semiconductor bodies 106 (and associated portions of dielectric layer 110) may be etched out, forming one or more openings 128 in IC 100, as generally can be seen from Figure 1L. To that end, IC 100 may be patterned, in accordance with some embodiments, using a dry etching process and/or a wet etching process. In some instances, an anisotropic plasma etching process may be employed. Also, in accordance with some embodiments, the etch chemistry for etching IC 100 can be customized, as desired, and in some instances may be selective to etching the material(s) of semiconductor bodies 106 and/or dielectric layer 110 as compared to the material(s) of gate layer 122 and/or dielectric layer 102. Furthermore, the geometry and dimensions of a given opening 128 (and thus of a given electrically conductive plug 124 of IC 100) can be customized, as desired for a given target application or end-use, and in some instances may depend, at least in part, on the type of etch process and/or etch chemistry utilized. Other suitable techniques for patterning IC 100 with one or more openings 128 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 1M, which is a cross-sectional view of the IC 100 of Figure 1L after formation of one or more electrically conductive plugs 124, in accordance with an embodiment of the present disclosure. Figure 1M′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1M (with dielectric layer 102 graphically omitted and dielectric layer 110 partially graphically omitted for ease of viewing). By filling a given opening 128 with an electrically conductive plug 124, a given channel of IC 100 may be converted to a via-type interconnect, in accordance with some embodiments. In some cases, a given electrically conductive plug 124 may be configured to serve, at least in part, as an inter-layer routing element for a host IC 100. In accordance with some embodiments, a given electrically conductive plug 124 may be configured to provide an electrical connection, for example, between: (1) a given upper interconnect 126 and an underlying gate layer 122; (2) a given lower interconnect 104 and an overlying gate layer 122; (3) a given upper interconnect 126 and a given underlying lower interconnect 104; and/or (4) a given upper interconnect 126, an underlying gate layer 122, and a given underlying interconnect 104. Numerous configurations and combinations of electrical connections will be apparent in light of this disclosure.

The one or more electrically conductive plugs 124 of IC 100 can be formed from any suitable electrically conductive material (or combination of such materials), using any of a wide range of techniques. For example, in accordance with some embodiments, a given electrically conductive plug 124 may be formed from: (1) tungsten (W); (2) titanium (Ti); (3) aluminum
5 (Al); (4) copper (Cu); and/or (5) an alloy (e.g., Ti-W) or other combination of any one or more thereof. In accordance with some embodiments, the one or more electrically conductive plugs 124 may be formed, for example, using: (1) a physical vapor deposition (PVD) process; (2) a chemical vapor deposition (CVD) process; (3) an electroplating process; (4) an electroless deposition process; and/or (5) a combination of any one or more thereof. Other suitable
10 materials and techniques for forming electrically conductive plug(s) 124 will depend on a given application and will be apparent in light of this disclosure.

Furthermore, the dimensions of a given electrically conductive plug 124 can be customized, as desired for a given target application or end-use, and in some cases may depend, at least in part, on the dimensions of a given host opening 128. In accordance with some
15 embodiments, a given electrically conductive plug 124 may have a width/diameter, for example, about equal to the width/diameter of a given semiconductor body 106 and associated portion(s) of dielectric layer 110 removed from IC 100 in forming a given opening 128. In accordance with some embodiments, a given electrically conductive plug 124 may have a length/height, for example, about equal to the length/height of a given semiconductor body 106 and associated
20 portion(s) of dielectric layer 110 removed from IC 100 in forming a given opening 128. Other suitable dimensions for the electrically conductive plug(s) 124 of IC 10 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 1N, which is a cross-sectional view of the IC 100 of Figure 1M after thinning, further formation of dielectric layer 102 and one or more
25 interconnects 126 (e.g., an upper routing layer), and planarization, in accordance with an embodiment of the present disclosure. Figure 1N′ illustrates a three-dimensional perspective view of the IC 100 of Figure 1N (with dielectric layer 102 graphically omitted and dielectric layer 110 partially graphically omitted for ease of viewing). After formation of electrically conductive plug(s) 124, IC 100 may undergo thinning, in accordance with some embodiments, to
30 remove any undesired portion of: (1) dielectric layer 102; (2) dielectric layer 110; and/or (3) electrically conductive plug(s) 124. To that end, IC 100 may undergo any suitable planarization/polish process, such as those discussed above, for instance, with respect to Figure 1A. As can be seen from Figure 1N, through planarization, one or more portions of dielectric layer 110 may be removed, exposing a given underlying semiconductor body 106 (e.g., at an
35 upper end thereof). In some cases, through planarization, the thickness of dielectric layer 102

may be reduced so as to make an upper surface of dielectric layer 102 substantially flush (e.g., precisely flush or otherwise within a given tolerance) with an upper surface of a given semiconductor body 106 and/or a given electrically conductive plug 124, such as can be seen generally from Figure 1N. However, the present disclosure is not so limited, as in a more general sense, and in accordance with some embodiments, dielectric layer 102 and/or dielectric layer 110 may be reduced to any given thickness, as desired for a given target application or end-use. Numerous suitable configurations will be apparent in light of this disclosure.

After thinning, one or more electrical interconnects 126 may be formed over IC 100, in accordance with some embodiments. To that end, IC 100 may undergo further formation of dielectric layer 102, for example, using any suitable technique (or combination of techniques), such as those discussed above, for instance, with respect to Figure 1A. In turn, dielectric layer 102 may be patterned using any suitable lithographic patterning technique (or combination of such techniques), such as those discussed above, for instance, with respect to patterning semiconductor layer 106, and one or more electrical interconnects 126 (e.g., an upper routing layer) may be formed within the resultant patterned dielectric layer 102. In accordance with some embodiments, a given interconnect 126 may be electronically coupled, for example, with an underlying electrically conductive plug 124 or with a given semiconductor body 106 (and associated dielectric layer 110). The geometry of a given interconnect 126 can be customized, as desired for a given target application or end-use, and in some cases may be selected from any of the example geometries discussed above, for instance, with respect to interconnect(s) 104. Also, a given interconnect 126 of IC 100 can be formed from any suitable electrically conductive material (or combination of such materials), using any of a wide range of suitable techniques, and in some cases may be formed from using one or more of the example materials and techniques discussed above, for instance, with respect to interconnect(s) 104. Other suitable materials, configurations, and techniques for forming interconnect(s) 126 will depend on a given application and will be apparent in light of this disclosure.

After formation of interconnect(s) 126, it may be desirable in some instances to planarize IC 100, for example, to remove any undesired excess (e.g., overburden) of: (1) a given interconnect 126; and/or (2) dielectric layer 102. To that end, IC 100 may undergo any suitable planarization/polish process, such as those discussed above, for instance, with respect to Figure 1A. In some cases, after planarization, a given interconnect 126 may have a thickness, for example, in the range of about 10–50 nm (e.g., about 10–30 nm, about 30–50 nm, or any other sub-range in the range of about 10–50 nm). However, the dimensions of interconnect(s) 126 are not so limited only to this example range, as in a more general sense, and in accordance with some embodiments, the dimensions of interconnect(s) 126 can be customized, as desired for a

given target application or end-use. In some cases, interconnect(s) 126 may have a substantially uniform thickness over the topography provided, for example, by any underlying layers of IC 100 (e.g., a given electrically conductive plug 124; a given semiconductor body 106 and associated dielectric layer 110; dielectric layer 102). In some other instances, however, a given interconnect 126 may be provided with a non-uniform or otherwise varying thickness over such topography. For example, in some cases a first portion of a given interconnect 126 may have a thickness within a first range, while a second portion thereof has a thickness within a second, different range. Other suitable dimensions for interconnect(s) 126 will depend on a given application and will be apparent in light of this disclosure.

As can be seen with respect to the example IC 100 of Figure 1N, Layers 1 and 3 are configured as the source/drain, Layer 2 is configured as the gate, and each of Layers 1, 2, and 3 is configured to serve, at least in part, as a local interconnect for IC 100. Also, within the example context of the IC 100 of Figure 1N, Channel 1 is a via-type interconnect (e.g., an electrically conductive plug 124) that electrically connects drain/source Layer 3 and gate Layer 2, and Channel 3 is a via-type interconnect (e.g., an electrically conductive plug 124) that electrically connects source/drain Layer 1 and gate Layer 2. Furthermore, within the example IC 100 of Figure 1N, Channels 2, 4, and 5 are active vertical transistors, whereas Channel 6 is etched out and the gate is cut so as to optionally blank that channel region of IC 100.

Numerous variations on the process flow of Figures 1A–1N, discussed above, will be apparent in light of this disclosure. For example, in accordance with some other embodiments, rather than forming dielectric layer 110 over IC 100 as described above with respect to Figure 1E (e.g., after patterning semiconductor layer 106 into one or more semiconductor bodies 106 as in Figures 1B and 1C and after further formation of dielectric layer 102 as in Figure 1E), dielectric layer 110 alternatively may be formed after etching dielectric 102 to form gate trench 120 (e.g., as described with respect to Figure 1I) and prior to formation of gate layer 122 (e.g., as described with respect to Figure 1J). Consequently, as can be seen by comparing the IC 100 of Figure 1N with Figure 2, which is a cross-sectional view of an IC 101 configured in accordance with another embodiment of the present disclosure, the IC 101 resulting from formation of dielectric layer 110 later in the process flow (e.g., between Figures 1I and 1J) may differ, to a greater or lesser degree, in its configuration as compared with formation of dielectric layer 110 earlier in the process flow (e.g., at Figure 1E between Figures 1D and 1F). In some cases, dielectric layer 110 may have one or more regions of discontinuity (e.g., gaps), such as where a separator portion 102a resides and/or where a blanked channel is optionally formed (e.g., as generally shown in Figure 2). In some cases, dielectric layer 110 may be configured to extend only

partially up the exterior sidewall of a given semiconductor body 106 so as not to make contact with an overlying interconnect 126 (e.g., as generally shown in Figure 2).

It should be noted, however, that the present disclosure is not so limited only to the example devices and electrical connections shown with respect to the IC 100 of Figure 1N and the IC 101 of Figure 2, as in a more general sense, the techniques disclosed herein can be utilized, in part or in whole, to form vertical semiconductor channel devices having any given quantity and configuration of vertical semiconductor device layers and electrical connections, as desired for a given target application or end-use. For instance, consider Figure 3A, which is a cross-sectional view of an example IC configured in accordance with another embodiment of the present disclosure. As can be seen here, the depicted example IC includes a single vertical semiconductor layer having interchangeable source and drain layers (e.g., interconnects 104 and 126) and a single gate (e.g., gate layer 122). Thus, the example IC of Figure 3A may be considered, in a general sense, a CMOS-like device. In contrast, consider Figure 3B, which is a cross-sectional view of an example IC configured in accordance with another embodiment of the present disclosure. As can be seen here, the depicted example IC includes two vertical semiconductor layers having fixed source and drain layers (e.g., interconnects 104, 126a, and 126b), sharing a common drain layer (e.g., interconnect 126a), and having multiple gates (e.g., gate layers 122a and 122b). More particularly, in the IC of Figure 3B, the lower vertical semiconductor device layer is configured as a p-type device (e.g., interconnect 104, gate 122a, and interconnect 126a), and the upper vertical semiconductor device layer is configured as an n-type device (e.g., interconnect 126a, gate 122b, and interconnect 126b). Thus, the example IC of Figure 3B may be considered, in a general sense, a TFET-like device.

Figure 4 illustrates a three-dimensional perspective view of an example inverter including a single vertical semiconductor layer (e.g., of nanowires and/or other three-dimensional semiconductor structures) configured in accordance with an embodiment of the present disclosure. Figure 5 illustrates a three-dimensional perspective view of an example inverter including two vertical semiconductor layers (e.g., of nanowires and/or other three-dimensional semiconductor structures) configured in accordance with another embodiment of the present disclosure. Figure 6 illustrates a three-dimensional perspective view of an example NAND logic gate including two vertical semiconductor layers (e.g., of nanowires and/or other three-dimensional semiconductor structures) configured in accordance with an embodiment of the present disclosure. As will be appreciated in light of this disclosure, the disclosed techniques can be used, in accordance with some embodiments, to form an IC having any quantity of gates (e.g., gate layers 122a, 122b, etc.), routing layers (e.g., interconnects 104, 126a, 126b, etc.), semiconductor channels (e.g., semiconductor bodies 106), vias (e.g., electrically conductive

plugs 124), and surrounding dielectric media (e.g., dielectric layer 102). Numerous vertical semiconductor channel architectures that may be fabricated, in part or in whole, using the disclosed techniques will be apparent in light of this disclosure.

Example System

5 Figure 7 illustrates a computing system 1000 implemented with integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and 10 electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc. Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. 15 These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage 20 device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise 25 integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-30 solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth,

derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices formed using the disclosed techniques as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit including: a first interconnect; at least one vertically oriented semiconductor body disposed over the first interconnect, wherein a first end of the at

least one vertically oriented semiconductor body is in electronic contact with the first interconnect; a gate layer surrounding an active channel portion of the at least one vertically oriented semiconductor body and configured as a second interconnect; and a third interconnect disposed over the gate layer, wherein a second end of the at least one vertically oriented
5 semiconductor body is in electronic contact with the third interconnect.

Example 2 includes the subject matter of any of Examples 1 and 3–25, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and at least one of those vertically oriented semiconductor bodies has been replaced with a conductive via to provide an inter-layer routing.

10 Example 3 includes the subject matter of any of Examples 1–2 and 4–25, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and at least one body location of that array is filled with a conductive material to provide a via for an inter-layer routing.

Example 4 includes the subject matter of any of Examples 1–3 and 5–25, wherein the at
15 least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and at least one of those vertically oriented semiconductor bodies has been replaced with an insulating material.

Example 5 includes the subject matter of any of Examples 1–4 and 6–25, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented
20 semiconductor bodies arranged in an array, and at least one body location of that array is filled with an insulating material.

Example 6 includes the subject matter of any of Examples 1–5 and 9–25, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented nanowires arranged in a regular array.

25 Example 7 includes the subject matter of any of Examples 1–5 and 9–25, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented nanowires arranged in a semi-regular array.

Example 8 includes the subject matter of any of Examples 1–5 and 9–25, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented nanowires
30 arranged in an irregular array.

Example 9 includes the subject matter of any of Examples 1–8 and 10–25 and further includes a blanked channel adjacent to the at least one vertically oriented semiconductor body.

Example 10 includes the subject matter of any of Examples 1–9 and 11–25 and further includes a via configured to provide an electrical connection between the first interconnect and
35 the gate layer.

Example 11 includes the subject matter of any of Examples 1–10 and 12–25 and further includes a via configured to provide an electrical connection between the third interconnect and the gate layer.

Example 12 includes the subject matter of any of Examples 1–11 and 13–25 and further includes a via configured to provide an electrical connection between the first interconnect and the third interconnect.

Example 13 includes the subject matter of any of Examples 1–12 and 14–25 and further includes a via configured to provide an electrical connection between the first interconnect, the gate layer, and the third interconnect.

Example 14 includes the subject matter of any of Examples 1–13 and 15–25, wherein the gate layer includes at least one of tungsten (W), aluminum (Al), titanium (Ti), titanium nitride (TiN), polysilicon, and/or a combination of any one or more thereof.

Example 15 includes the subject matter of any of Examples 1–14 and 16–25, wherein the at least one vertically oriented semiconductor body includes at least one of silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), indium phosphide (InP), and/or a combination of any one or more thereof.

Example 16 includes the subject matter of any of Examples 1–15 and 17–25, wherein the at least one vertically oriented semiconductor body has a length in the range of about 10–100 nm.

Example 17 includes the subject matter of any of Examples 1–16 and 18–25, wherein the at least one vertically oriented semiconductor body has a width/diameter in the range of about 1–20 nm.

Example 18 includes the subject matter of any of Examples 1–17 and 20–25, wherein the gate layer is a continuous layer having a thickness in the range of about 10–30 nm.

Example 19 includes the subject matter of any of Examples 1–17 and 20–25, wherein the gate layer is a discontinuous layer having one or more gaps therein and having a thickness in the range of about 10–30 nm.

Example 20 includes the subject matter of any of Examples 1–19 and 21–25 and further includes a dielectric layer disposed over the at least one vertically oriented semiconductor body, wherein the dielectric layer is sandwiched between the gate layer and the active channel portion of the at least one vertically oriented semiconductor body.

Example 21 includes the subject matter of Example 20, wherein the dielectric layer includes at least one of hafnium oxide (HfO_2), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), lanthanum

oxide (La_2O_3), hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), strontium titanate ($SrTiO_3$), and/or a combination of any one or more thereof.

Example 22 includes the subject matter of Example 20, wherein the dielectric layer has a thickness in the range of about 1–10 nm.

5 Example 23 is a memory including the subject matter of any of Examples 1–22.

Example 24 is an inverter including the subject matter of any of Examples 1–22.

Example 25 is a logic gate including the subject matter of any of Examples 1–22.

Example 26 is a method of forming an integrated circuit, the method including: providing a semiconductor layer over a first interconnect; patterning the semiconductor layer into at least 10 one vertically oriented semiconductor body, wherein a first end of the at least one vertically oriented semiconductor body is in electronic contact with the first interconnect; forming a gate layer surrounding an active channel portion of the at least one vertically oriented semiconductor body, wherein the gate layer is configured as a second interconnect; and providing a third interconnect over the gate layer, wherein a second end of the at least one vertically oriented 15 semiconductor body is in electronic contact with the third interconnect.

Example 27 includes the subject matter of any of Examples 26 and 28–48, wherein providing the semiconductor layer over the first interconnect includes: transferring the semiconductor layer to the first interconnect utilizing at least one of an ion-cut process, an amorphous layer blister process, a strain-induced spalling process, a backside grinding process, 20 and/or a combination of any one or more thereof.

Example 28 includes the subject matter of any of Examples 26–27 and 29–48, wherein the semiconductor layer includes at least one of silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), indium phosphide (InP), and/or a combination of any one or more thereof.

25 Example 29 includes the subject matter of any of Examples 26–28 and 30–48, wherein the semiconductor layer has a thickness in the range of about 10–100 nm.

Example 30 includes the subject matter of any of Examples 26–29 and 31–48, wherein patterning the semiconductor layer into the at least one vertically oriented semiconductor body involves at least one of an immersion lithography process, an electron-beam (e-beam) 30 lithography process, an extreme ultraviolet (EUV) lithography process, and/or a combination of any one or more thereof.

Example 31 includes the subject matter of any of Examples 26–30 and 34–48, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented nanowires arranged in a regular array.

Example 32 includes the subject matter of any of Examples 26–30 and 34–48, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented nanowires arranged in a semi-regular array.

Example 33 includes the subject matter of any of Examples 26–30 and 34–48, wherein
5 the at least one vertically oriented semiconductor body is a plurality of vertically oriented nanowires arranged in an irregular array.

Example 34 includes the subject matter of any of Examples 26–33 and 35–48, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies, and wherein prior to forming the gate layer, the method further includes:
10 replacing at least one of the plurality of vertically oriented semiconductor bodies with a dielectric material.

Example 35 includes the subject matter of Example 34, wherein the dielectric material provides a blanked channel.

Example 36 includes the subject matter of any of Examples 26–35 and 37–48, wherein
15 the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and wherein the method further includes: removing at least one of those vertically oriented semiconductor bodies to provide an empty location within the array; and filling that location with a conductive material to provide a via for an inter-layer routing.

20 Example 37 includes the subject matter of any of Examples 26–36 and 38–48, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies, and wherein prior to providing the third interconnect over the gate layer, the method further includes: replacing at least one of the plurality of vertically oriented semiconductor bodies with an electrically conductive material.

25 Example 38 includes the subject matter of Example 37, wherein the electrically conductive material provides an electrical connection between the first interconnect and the gate layer.

Example 39 includes the subject matter of Example 37, wherein the electrically conductive material provides an electrical connection between the third interconnect and the gate
30 layer.

Example 40 includes the subject matter of Example 37, wherein the electrically conductive material provides an electrical connection between the first interconnect and the third interconnect.

Example 41 includes the subject matter of Example 37, wherein the electrically conductive material provides an electrical connection between the first interconnect, the gate layer, and the third interconnect.

Example 42 includes the subject matter of any of Examples 26–41 and 43–48, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and wherein the method further includes: removing at least one of those vertically oriented semiconductor bodies to provide an empty location within the array; and filling that location with an insulating material.

Example 43 includes the subject matter of any of Examples 26–42 and 44–48, wherein the gate layer includes at least one of tungsten (W), aluminum (Al), titanium (Ti), titanium nitride (TiN), polysilicon, and/or a combination of any one or more thereof.

Example 44 includes the subject matter of any of Examples 26–43 and 46–48, wherein the gate layer is a continuous layer having a thickness in the range of about 10–30 nm.

Example 45 includes the subject matter of any of Examples 26–43 and 46–48, wherein the gate layer is a discontinuous layer having one or more gaps therein and having a thickness in the range of about 10–30 nm.

Example 46 includes the subject matter of any of Examples 26–45 and 47–48, wherein prior to forming the gate layer, the method further includes: forming a dielectric layer over the at least one vertically oriented semiconductor body, wherein the dielectric layer is sandwiched between the gate layer and the active channel portion of the at least one vertically oriented semiconductor body.

Example 47 includes the subject matter of Example 46, wherein the dielectric layer includes at least one of hafnium oxide (HfO_2), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), lanthanum oxide (La_2O_3), hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), strontium titanate ($SrTiO_3$), and/or a combination of any one or more thereof.

Example 48 includes the subject matter of Example 46, wherein the dielectric layer has a thickness in the range of about 1–10 nm.

Example 49 is an integrated circuit including a first transistor device layer including: a first routing layer; a first plurality of vertically oriented semiconductor nanowires disposed over the first routing layer, wherein a first end of at least one of the first plurality of vertically oriented semiconductor nanowires is in electronic contact with the first routing layer; a first gate surrounding an active channel portion of at least one of the first plurality of vertically oriented semiconductor nanowires and configured as a first interconnect for the first transistor device layer; and a second routing layer disposed over the first gate, wherein a second end of at least

one of the first plurality of vertically oriented semiconductor nanowires is in electronic contact with the second routing layer.

Example 50 includes the subject matter of any of Examples 49 and 51–60, wherein the first transistor device layer further includes a blanked channel adjacent to the first plurality of vertically oriented semiconductor nanowires.

Example 51 includes the subject matter of any of Examples 49–50 and 52–60, wherein at least one of the first plurality of vertically oriented semiconductor nanowires has been replaced with an insulating material.

Example 52 includes the subject matter of any of Examples 49–51 and 53–60, wherein the first transistor device layer further includes a via configured to provide at least one of an electrical connection between the first routing layer and the first gate, an electrical connection between the second routing layer and the first gate, an electrical connection between the first routing layer and the second routing layer, and/or an electrical connection between the first routing layer, the first gate, and the second routing layer.

Example 53 includes the subject matter of any of Examples 49–52 and 54–60, wherein at least one of the first plurality of vertically oriented semiconductor nanowires has been replaced with a conductive via to provide an inter-layer routing.

Example 54 includes the subject matter of any of Examples 49–53 and 55–60, wherein the first plurality of vertically oriented semiconductor nanowires is arranged in a regular array.

Example 55 includes the subject matter of any of Examples 49–54 and 56–60 and further includes a second transistor device layer disposed over the first transistor device layer, the second transistor device layer including: the second routing layer; a second plurality of vertically oriented semiconductor nanowires disposed over the second routing layer, wherein a first end of at least one of the second plurality of vertically oriented semiconductor nanowires is in electronic contact with the second routing layer; a second gate surrounding an active channel portion of at least one of the second plurality of vertically oriented semiconductor nanowires and configured as a second interconnect for the second transistor device layer; and a third routing layer disposed over the second gate, wherein a second end of at least one of the second plurality of vertically oriented semiconductor nanowires is in electronic contact with the third routing layer.

Example 56 includes the subject matter of Example 55, wherein the second transistor device layer further includes a blanked channel adjacent to the second plurality of vertically oriented semiconductor nanowires.

Example 57 includes the subject matter of Example 55, wherein at least one of the second plurality of vertically oriented semiconductor nanowires has been replaced with an insulating material.

Example 58 includes the subject matter of Example 55, wherein the second transistor device layer further includes a via configured to provide at least one of an electrical connection between the second routing layer and the second gate, an electrical connection between the third routing layer and the second gate, an electrical connection between the second routing layer and the third routing layer, and/or an electrical connection between the second routing layer, the second gate, and the third routing layer.

Example 59 includes the subject matter of Example 55, wherein at least one of the second plurality of vertically oriented semiconductor nanowires has been replaced with a conductive via to provide an inter-layer routing.

Example 60 includes the subject matter of any of Examples 55–59, wherein the second plurality of vertically oriented semiconductor nanowires is arranged in a regular array.

The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the present disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the present disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future-filed applications claiming priority to this application may claim the disclosed subject matter in a different manner and generally may include any set of one or more limitations as variously disclosed or otherwise demonstrated herein.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

5 a first interconnect;

at least one vertically oriented semiconductor body disposed over the first interconnect, wherein a first end of the at least one vertically oriented semiconductor body is in electronic contact with the first interconnect;

a gate layer surrounding an active channel portion of the at least one vertically oriented
10 semiconductor body and configured as a second interconnect; and

a third interconnect disposed over the gate layer, wherein a second end of the at least one vertically oriented semiconductor body is in electronic contact with the third interconnect.

2. The integrated circuit of claim 1, wherein the at least one vertically oriented
15 semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and at least one of those vertically oriented semiconductor bodies has been replaced with a conductive via to provide an inter-layer routing.

3. The integrated circuit of claim 1, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an
20 array, and at least one body location of that array is filled with a conductive material to provide a via for an inter-layer routing.

4. The integrated circuit of claim 1, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and at least one of those vertically oriented semiconductor bodies has been replaced with
25 an insulating material.

5. The integrated circuit of claim 1, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and at least one body location of that array is filled with an insulating material.

6. The integrated circuit of claim 1, wherein the at least one vertically oriented
30 semiconductor body is a plurality of vertically oriented nanowires arranged in a regular array.

7. The integrated circuit of claim 1 further comprising a blanked channel adjacent to the at least one vertically oriented semiconductor body.

8. The integrated circuit of claim 1 further comprising a via configured to provide at least one of:

an electrical connection between the first interconnect and the gate layer;

an electrical connection between the third interconnect and the gate layer;

an electrical connection between the first interconnect and the third interconnect; and/or

an electrical connection between the first interconnect, the gate layer, and the third interconnect.

5

9. The integrated circuit of claim 1 further comprising a dielectric layer disposed over the at least one vertically oriented semiconductor body, wherein the dielectric layer is sandwiched between the gate layer and the active channel portion of the at least one vertically oriented semiconductor body.

10

10. A memory comprising the integrated circuit of any of claims 1–9.

11. An inverter comprising the integrated circuit of any of claims 1–9.

12. A logic gate comprising the integrated circuit of any of claims 1–9.

13. A method of forming an integrated circuit, the method comprising:

providing a semiconductor layer over a first interconnect;

15

patterning the semiconductor layer into at least one vertically oriented semiconductor body, wherein a first end of the at least one vertically oriented semiconductor body is in electronic contact with the first interconnect;

forming a gate layer surrounding an active channel portion of the at least one vertically oriented semiconductor body, wherein the gate layer is configured as a second interconnect; and

20

providing a third interconnect over the gate layer, wherein a second end of the at least one vertically oriented semiconductor body is in electronic contact with the third interconnect.

14. The method of claim 13, wherein providing the semiconductor layer over the first interconnect comprises:

25

transferring the semiconductor layer to the first interconnect utilizing at least one of an ion-cut process, an amorphous layer blister process, a strain-induced spalling process, a backside grinding process, and/or a combination of any one or more thereof.

30

15. The method of claim 13, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies, and wherein prior to forming the gate layer, the method further comprises:

replacing at least one of the plurality of vertically oriented semiconductor bodies with a dielectric material, wherein the dielectric material provides a blanked channel.

35

16. The method of claim 13, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and wherein the method further comprises:

removing at least one of those vertically oriented semiconductor bodies to provide an empty location within the array; and

filling that location with a conductive material to provide a via for an inter-layer routing.

17. The method of claim 13, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies, and wherein prior to providing the third interconnect over the gate layer, the method further comprises:

replacing at least one of the plurality of vertically oriented semiconductor bodies with an electrically conductive material, wherein the electrically conductive material provides at least one of:

an electrical connection between the first interconnect and the gate layer;

an electrical connection between the third interconnect and the gate layer;

an electrical connection between the first interconnect and the third interconnect; and/or

an electrical connection between the first interconnect, the gate layer, and the third interconnect.

18. The method of claim 13, wherein the at least one vertically oriented semiconductor body is a plurality of vertically oriented semiconductor bodies arranged in an array, and wherein the method further comprises:

removing at least one of those vertically oriented semiconductor bodies to provide an empty location within the array; and

filling that location with an insulating material.

19. The method of claim 13, wherein prior to forming the gate layer, the method further comprises:

forming a dielectric layer over the at least one vertically oriented semiconductor body, wherein the dielectric layer is sandwiched between the gate layer and the active channel portion of the at least one vertically oriented semiconductor body.

20. An integrated circuit comprising:

a first transistor device layer comprising:

a first routing layer;

a first plurality of vertically oriented semiconductor nanowires disposed over the first routing layer, wherein a first end of at least one of the first plurality of

vertically oriented semiconductor nanowires is in electronic contact with the first routing layer;

a first gate surrounding an active channel portion of at least one of the first plurality of vertically oriented semiconductor nanowires and configured as a first interconnect for the first transistor device layer; and

a second routing layer disposed over the first gate, wherein a second end of at least one of the first plurality of vertically oriented semiconductor nanowires is in electronic contact with the second routing layer.

21. The integrated circuit of claim 20, wherein the first transistor device layer further comprises at least one of:

a blanked channel adjacent to the first plurality of vertically oriented semiconductor nanowires; and/or

a via configured to provide at least one of:

an electrical connection between the first routing layer and the first gate;

an electrical connection between the second routing layer and the first gate;

an electrical connection between the first routing layer and the second routing layer; and/or

an electrical connection between the first routing layer, the first gate, and the second routing layer.

22. The integrated circuit of claim 20, wherein at least one of the first plurality of vertically oriented semiconductor nanowires has been replaced with an insulating material or a conductive via to provide an inter-layer routing.

23. The integrated circuit of claim 20 further comprising:

a second transistor device layer disposed over the first transistor device layer, the second transistor device layer comprising:

the second routing layer;

a second plurality of vertically oriented semiconductor nanowires disposed over the second routing layer, wherein a first end of at least one of the second plurality of vertically oriented semiconductor nanowires is in electronic contact with the second routing layer;

a second gate surrounding an active channel portion of at least one of the second plurality of vertically oriented semiconductor nanowires and configured as a second interconnect for the second transistor device layer; and

a third routing layer disposed over the second gate, wherein a second end of at least one of the second plurality of vertically oriented semiconductor nanowires is in electronic contact with the third routing layer.

24. The integrated circuit of claim 20, wherein the second transistor device layer further comprises at least one of:

a blanked channel adjacent to the second plurality of vertically oriented semiconductor nanowires; and/or

a via configured to provide at least one of:

an electrical connection between the second routing layer and the second gate;

an electrical connection between the third routing layer and the second gate;

an electrical connection between the second routing layer and the third routing layer; and/or

an electrical connection between the second routing layer, the second gate, and the third routing layer.

25. The integrated circuit of claim 20, wherein at least one of the second plurality of vertically oriented semiconductor nanowires has been replaced with an insulating material or a conductive via to provide an inter-layer routing.

Figure 1A

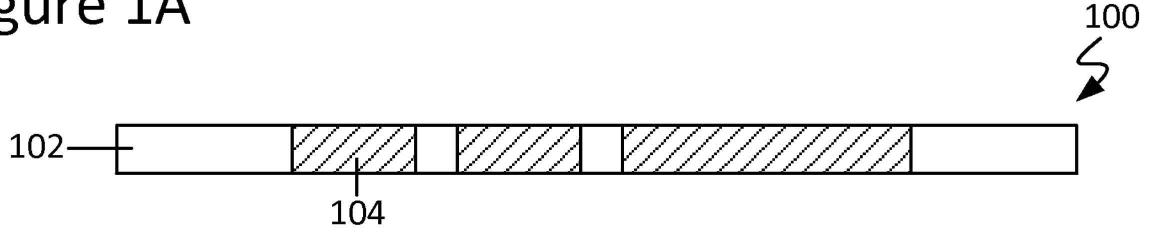


Figure 1A'

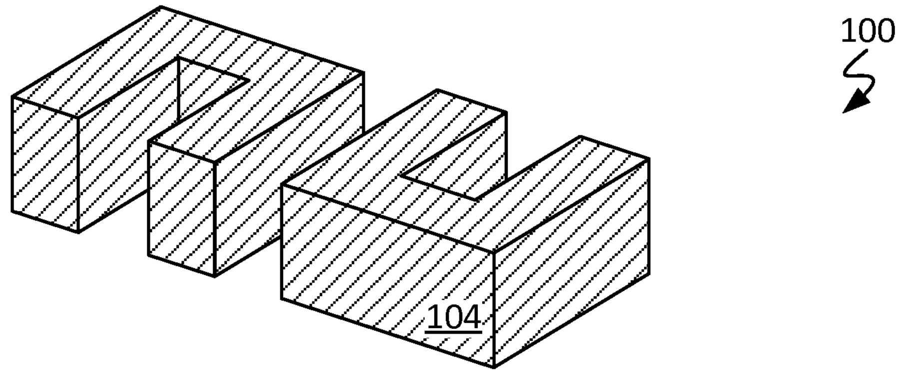


Figure 1B

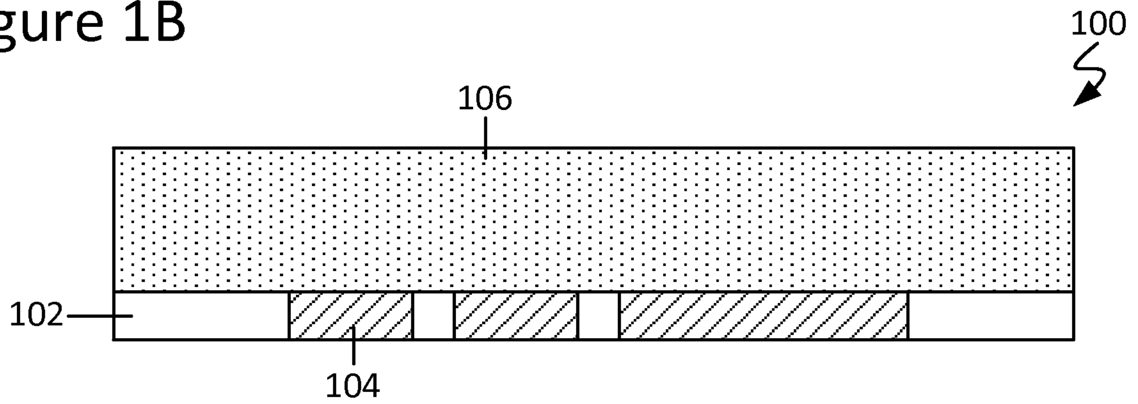


Figure 1C

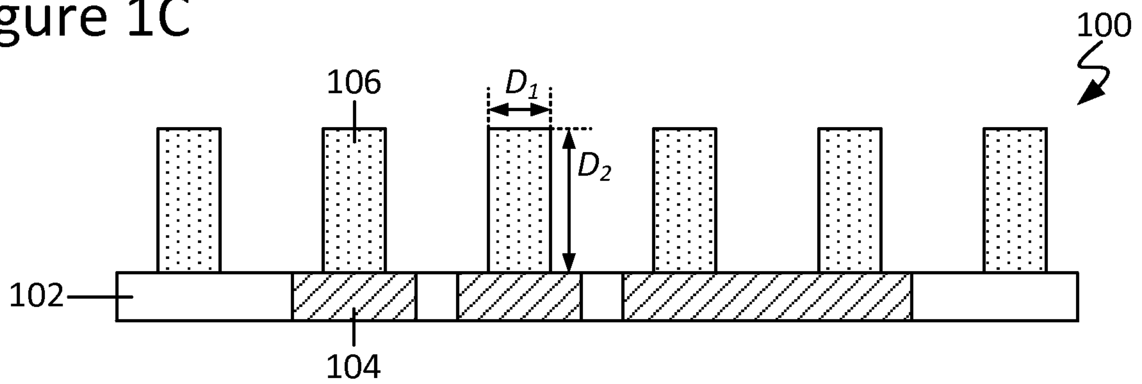


Figure 1C'

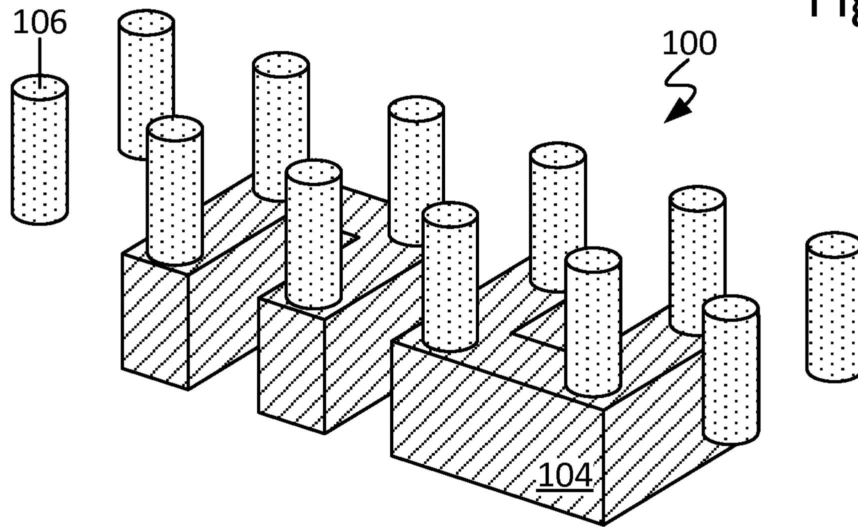


Figure 1D

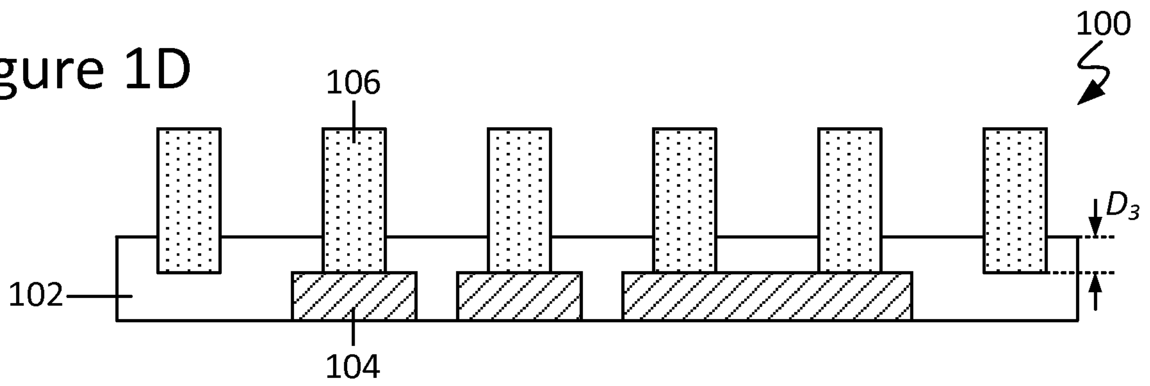
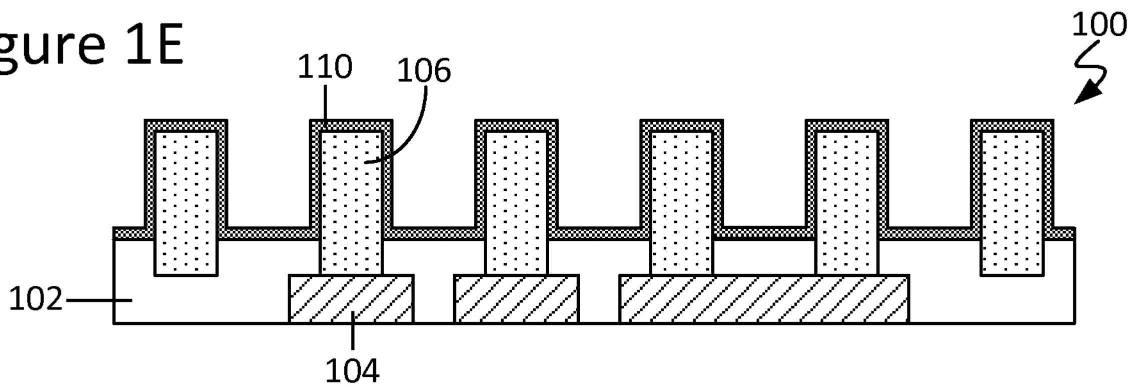


Figure 1E



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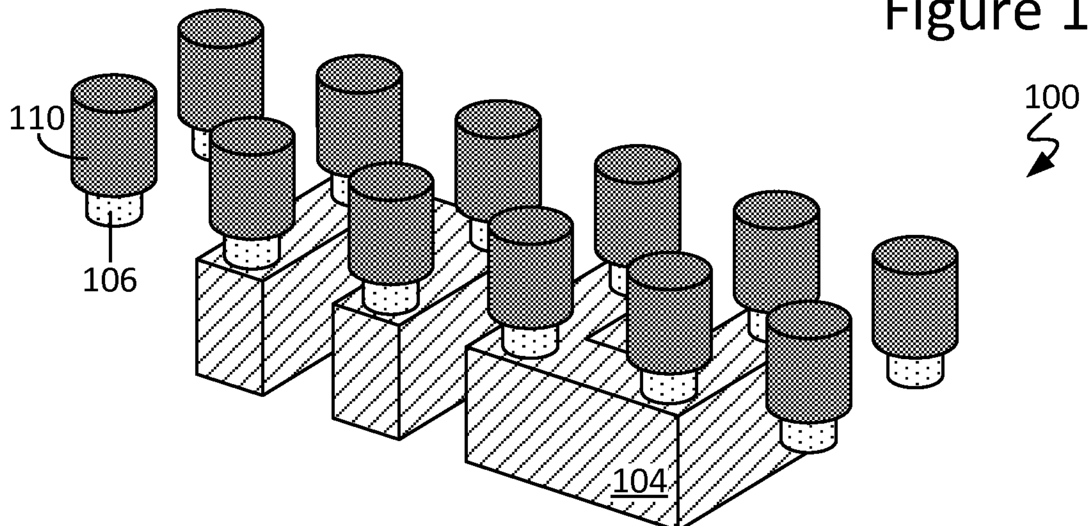


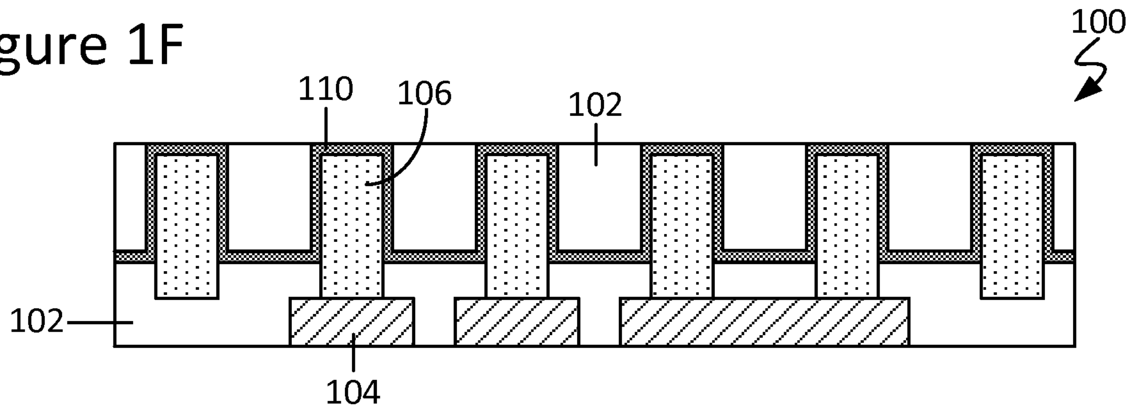


Figure 1F
100
110
106
102
102
104

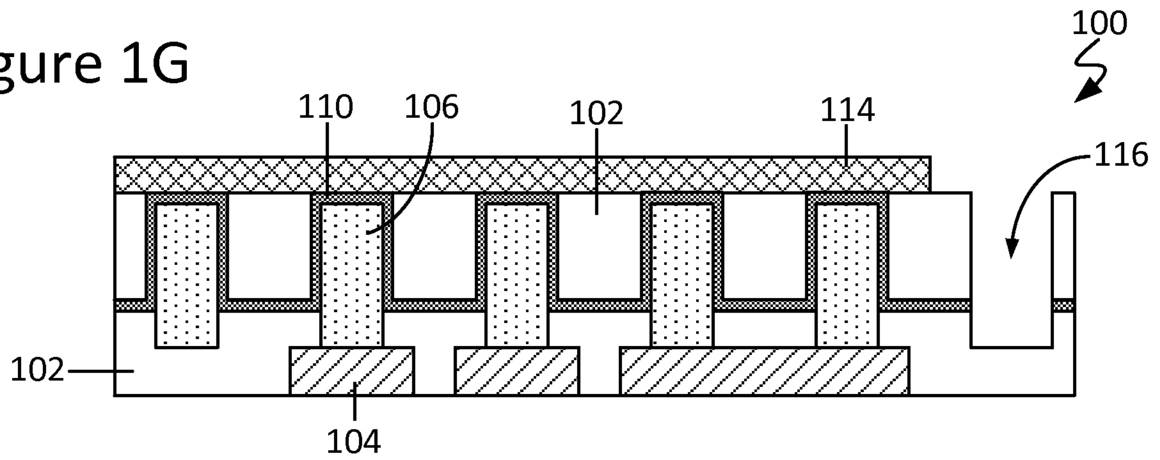


Figure 1G
100
110
106
102
114
116
102
104

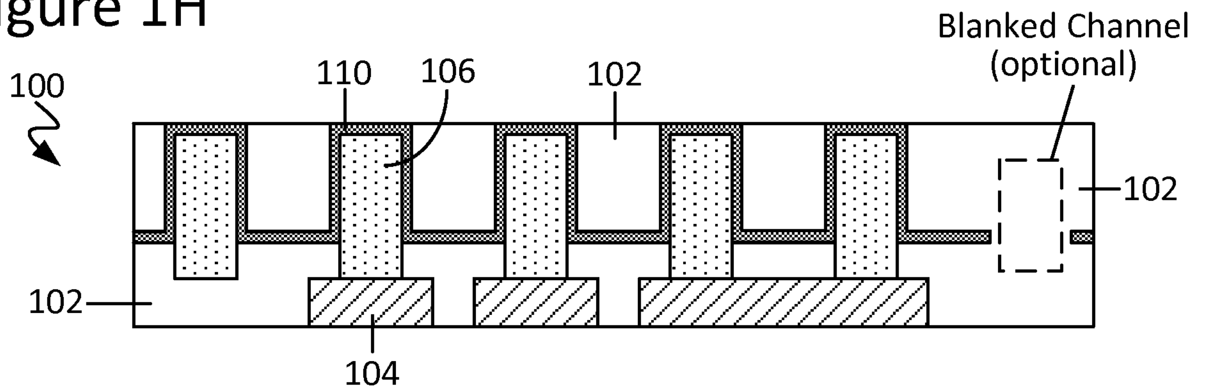


Figure 1H
Blanked Channel
(optional)
100
110
106
102
102
102
104

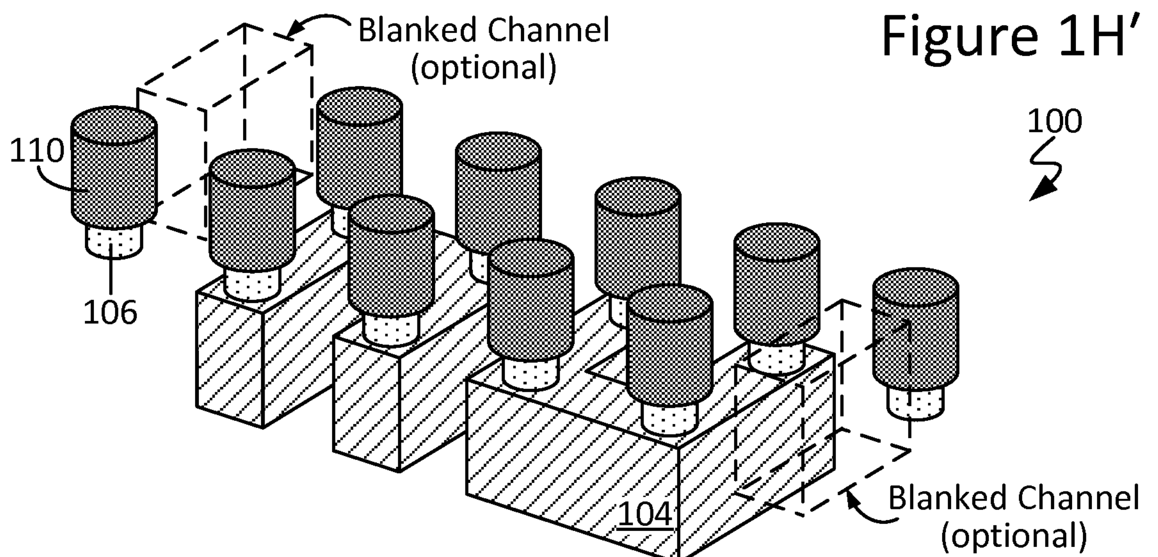

Blanked Channel
(optional)
Figure 1H'
100
110
106
104
Blanked Channel
(optional)

Figure 1I

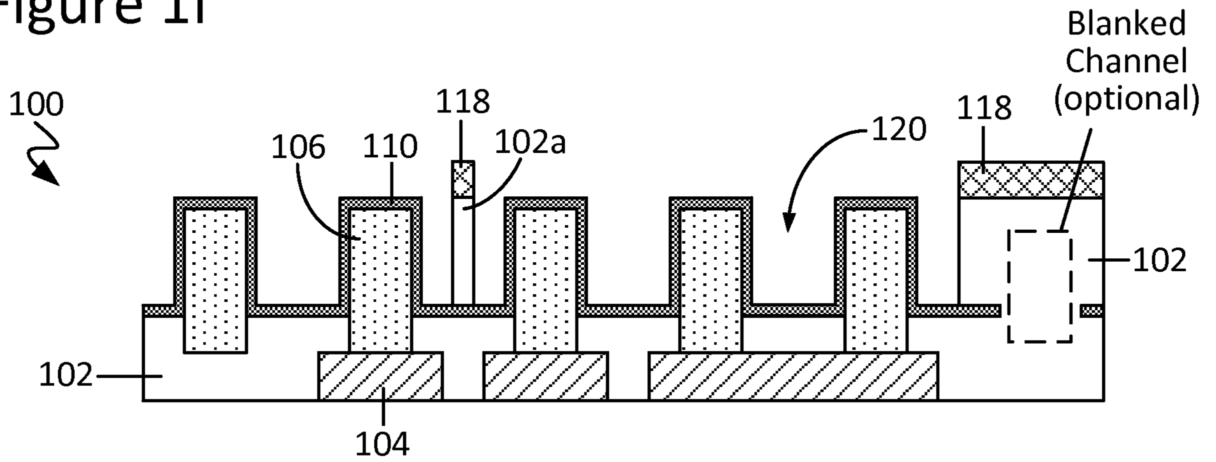


Figure 1J

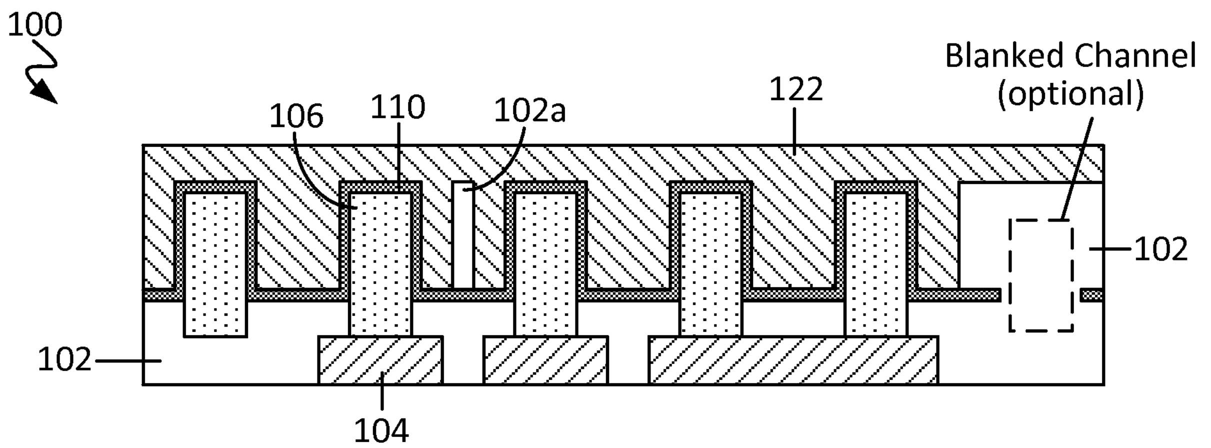
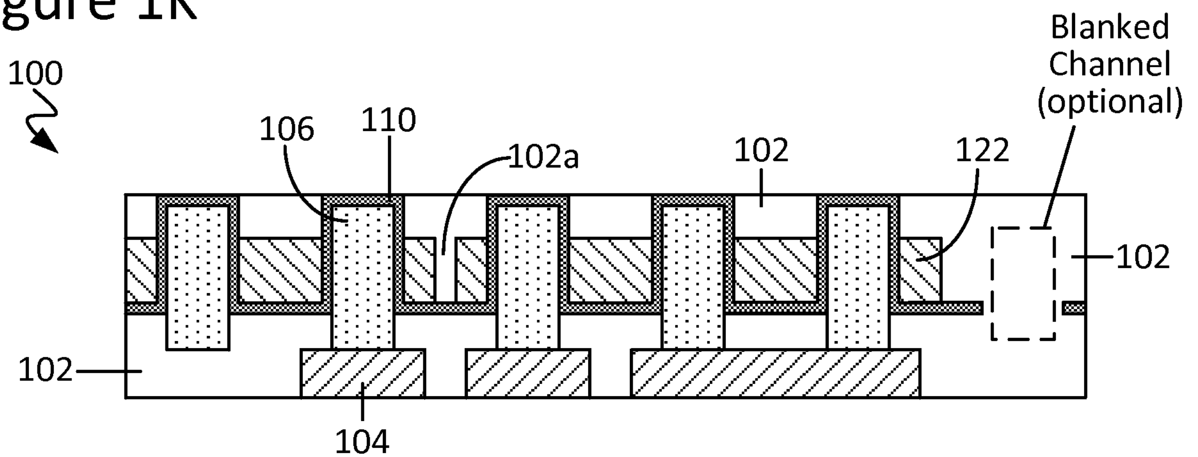


Figure 1K



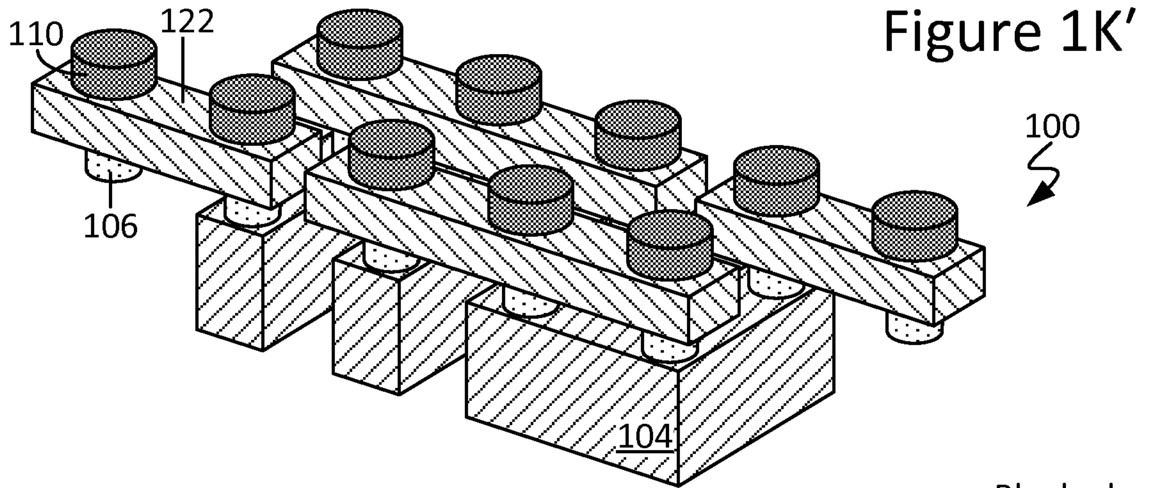


Figure 1K'
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122
106
100
104

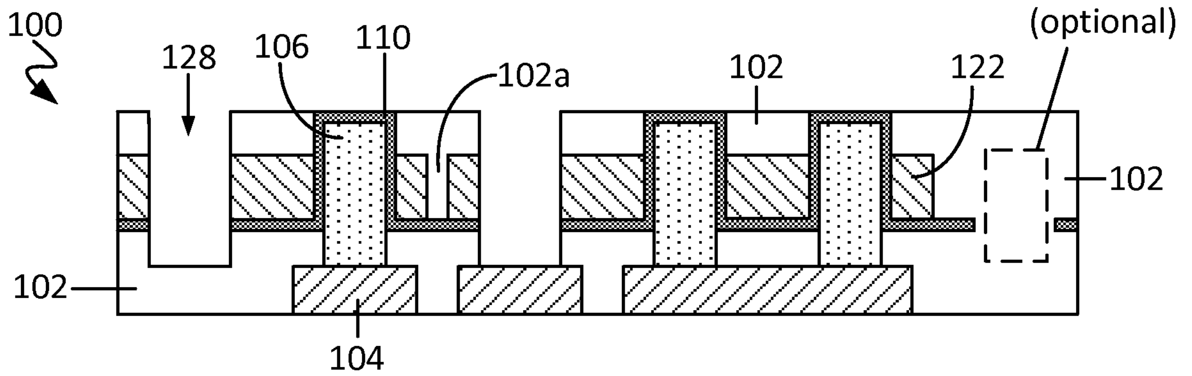
Figure 1L
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128
106
110
102a
102
122
Blanked
Channel
(optional)
102
102
104

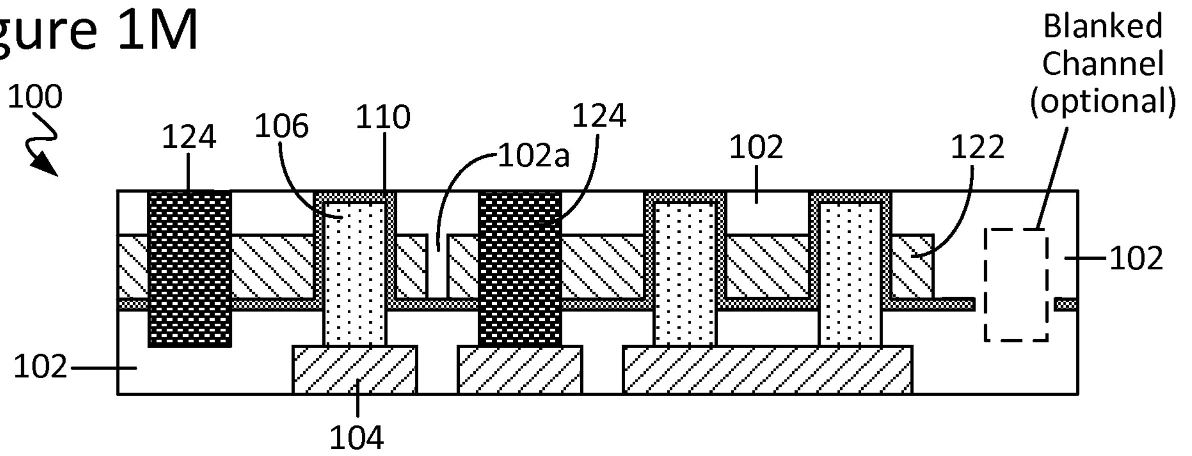
Figure 1M
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124
106
110
102a
124
102
122
Blanked
Channel
(optional)
102
102
104

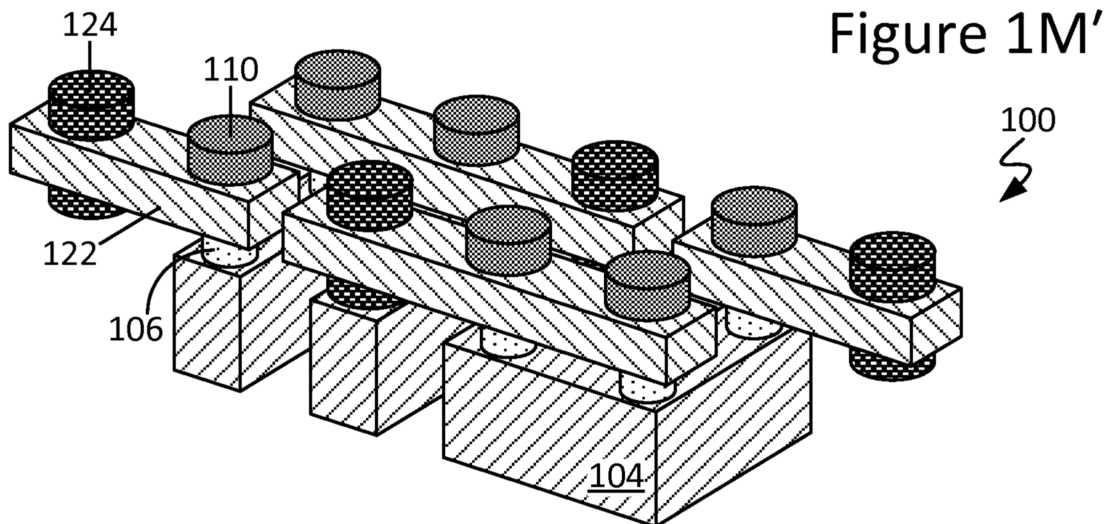
Figure 1M'
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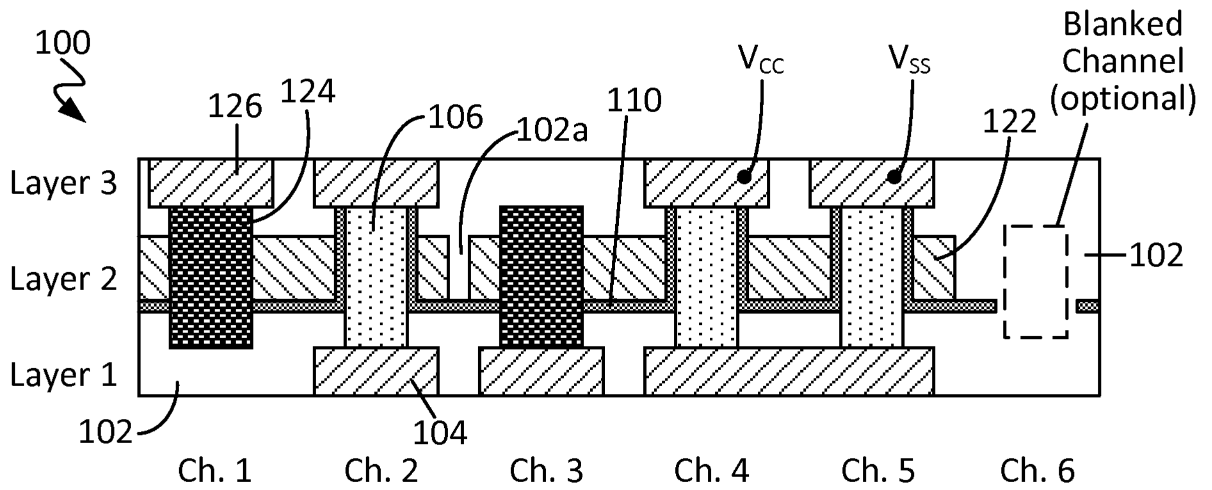
100
122
106
104

Figure 1N



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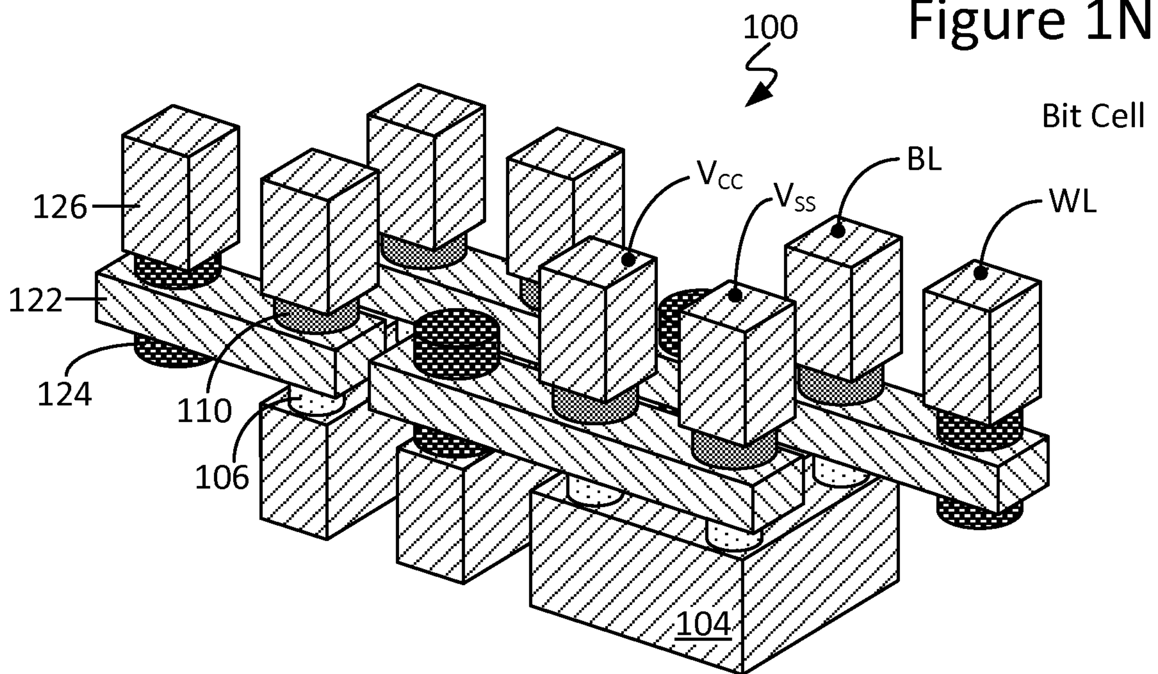

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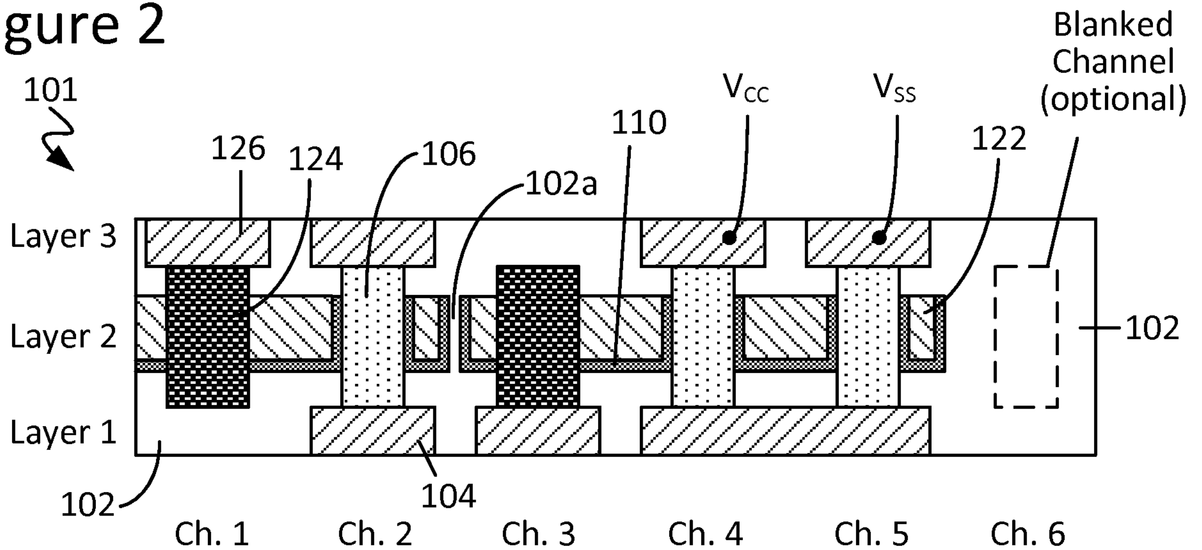


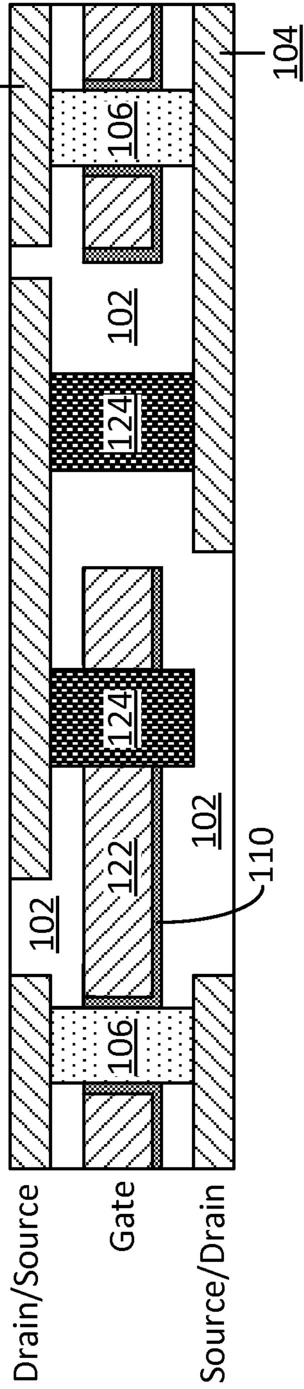


Figure 3A

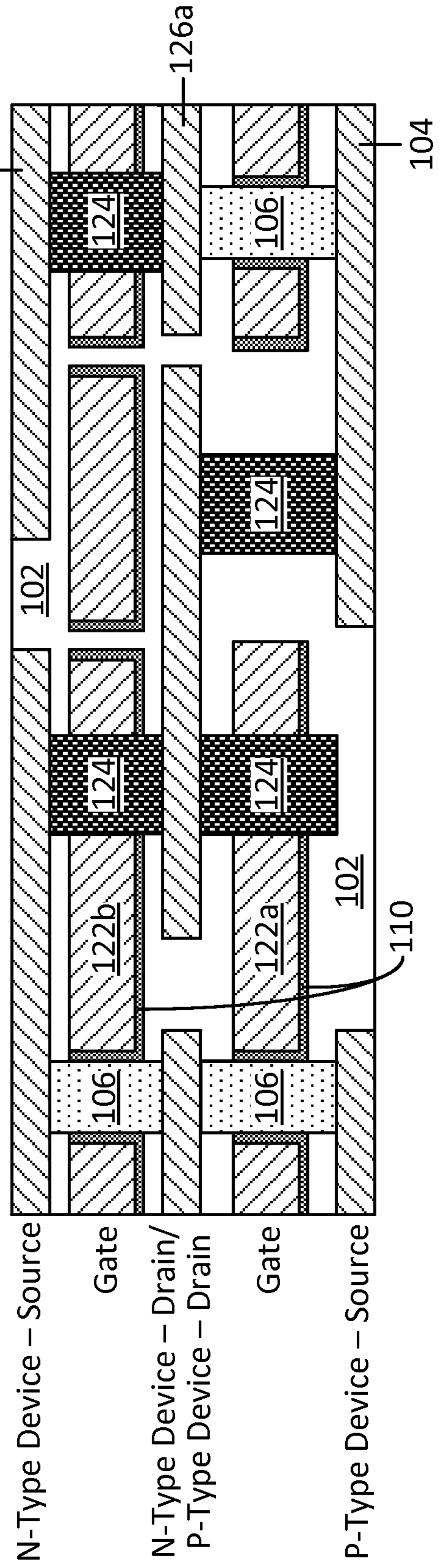


Figure 3B

Figure 4

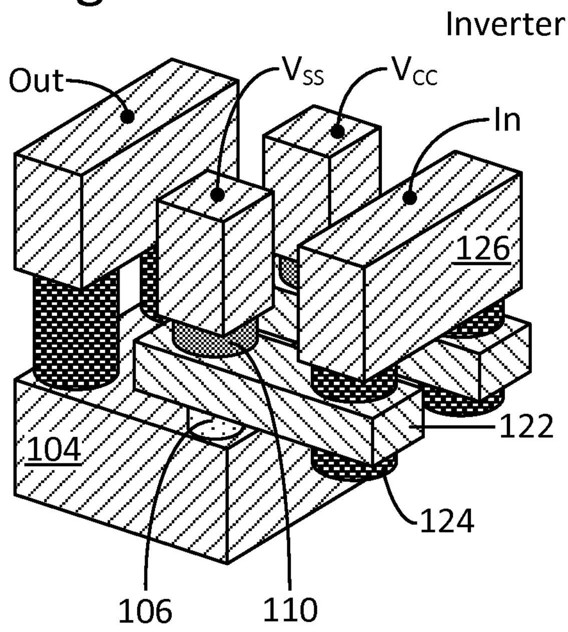


Figure 5

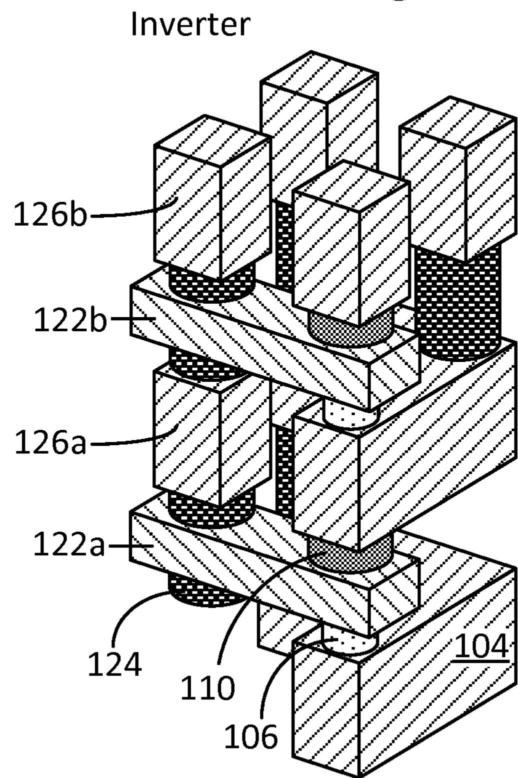


Figure 6

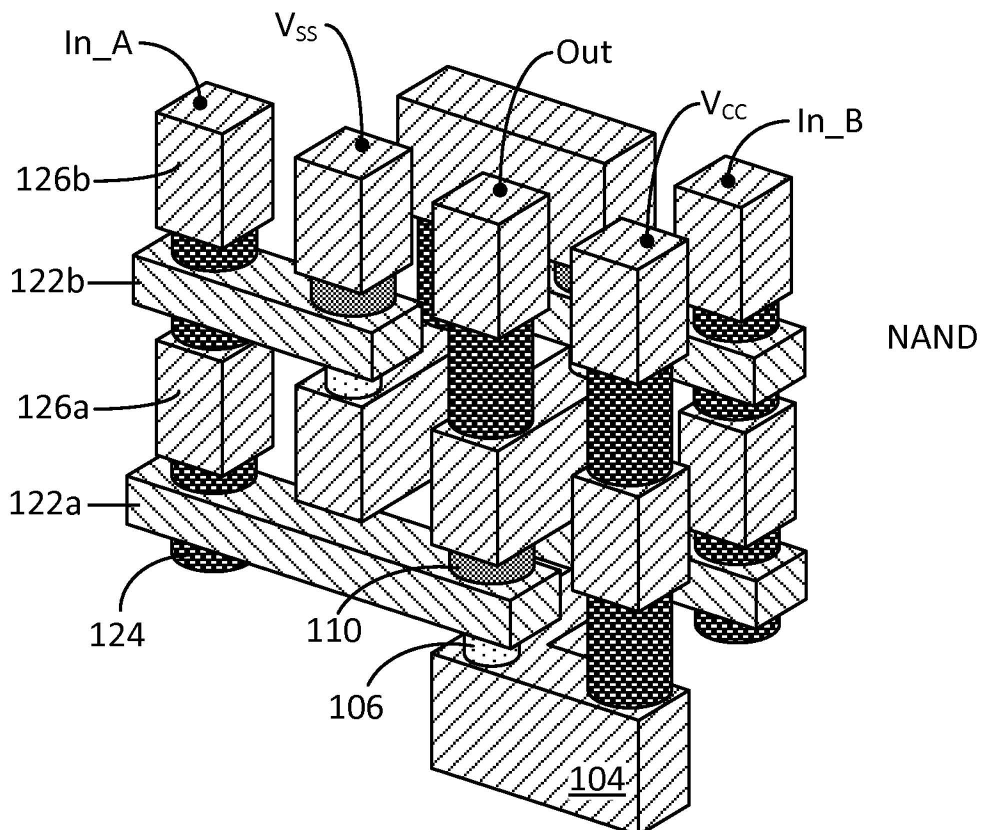
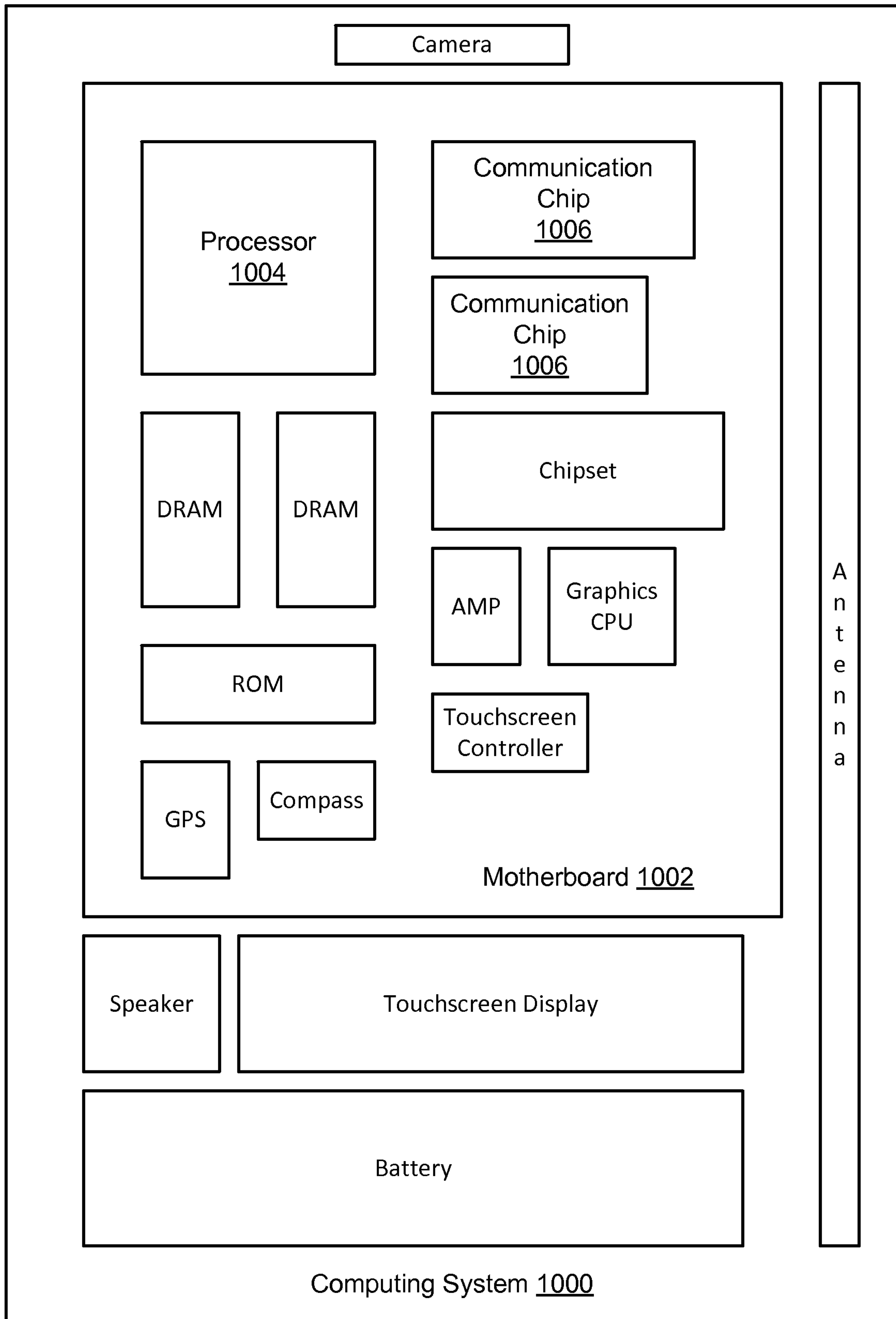


Figure 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/043683

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 23/52; H01L 27/088; H01L 21/336; G06F 12/14; H01L 29/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: vertical, channel, transistor, interconnect, semiconductor, gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005-0253143 A1 (NORIKATSU TAKAURA et al.) 17 November 2005 See abstract, paragraphs [0018], [0091]-[0107], claims 1, 3, 7 and figures 2, 4, 7B, 7C, 8A-8D.	1-25
A	US 2008-0048327 A1 (SANG-YUN LEE) 28 February 2008 See abstract, paragraphs [0045]-[0055], claims 1-7 and figures 2, 4.	1-25
A	US 2013-0015500 A1 (TAKASHI IZUMIDA et al.) 17 January 2013 See abstract, paragraphs [0028]-[0039], claim 1 and figures 1A-1C.	1-25
A	US 2010-0203695 A1 (YONG-CHUL OH et al.) 12 August 2010 See abstract, paragraphs [0040]-[0079] and figures 1, 2.	1-25
A	US 2010-0038709 A1 (KUO-CHEN WANG et al.) 18 February 2010 See abstract, paragraphs [0048]-[0052] and figures 1, 2.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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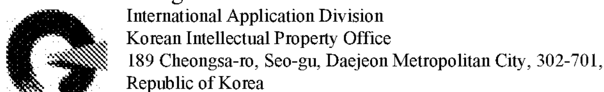
Date of the actual completion of the international search
26 March 2015 (26.03.2015)

Date of mailing of the international search report
26 March 2015 (26.03.2015)

Name and mailing address of the ISA/KR

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KIM, Tae Hoon

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