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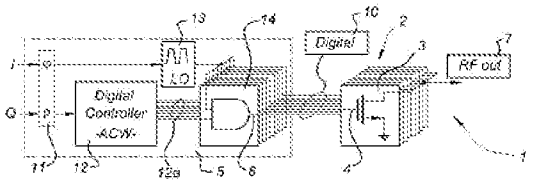
(54) **Digital transmitter with high power output**

(57) An RF transmitter (1) having a gate-segmented power output stage (2) and a digital driver (5). The gate-segmented power output stage (2) includes a field-effect transistor with a plurality of gate fingers (32) and drain fingers (31) that define a gate periphery. The field-effect transistor comprises a plurality of power output stage segments (3) that each correspond to a respective part of the gate periphery, and that each have a respective power output stage segment input (4). The digital driver (5) has control outputs (6) which are connected to corresponding ones of the respective power output stage segment inputs (4), and is configured for individually switching each of the power output stage segments (3) between an on mode and a cut-off mode in dependence of one or more input signals to obtain a modulated RF carrier signal at an output (7) of the gate-segmented power output stage (2).



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Digital transmitter with high power output

Field of the invention

The present invention relates to an RF transmitter, comprising a power output stage and a digital driver connected to the power output stage, specifically suitable for high-speed and high-power applications, such as 5G mMIMO base stations.

Background art

The article by V. Diddi et al. entitled "Broadband digitally-controlled power amplifier based on CMOS / GaN combination," 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, 2016, pp. 258-261, discloses a digital RF power transmitter configuration with a control part and (single) amplifier stage, wherein the control part provides an analogue signal to the power amplifier stage.

Summary of the invention

The present invention seeks to provide an improved RF transmitter implementation, which is specifically suited for high-speed, high-frequency, RF power applications, such as 5G massive Multiple Input Multiple Output (mMIMO) base stations.

According to the present invention, an RF transmitter is provided, comprising a gate-segmented power output stage, said power output stage comprising a field-effect transistor having a plurality of gate fingers and a plurality of drain fingers that define a gate periphery, the field-effect transistor comprising a plurality of power output stage segments that each correspond to a respective part of the gate periphery and that each have a respective power output stage segment input. The RF transmitter further comprises a digital driver having control outputs which are connected to corresponding ones of the respective power output stage segment inputs, the digital driver being configured for individually switching each of the power output stage segments between an on-mode and a cut-off mode, in dependence of one or more input signals, e.g. baseband signals in combination with one or more RF carrier signals and/or one or more RF reference clocks, to obtain a modulated RF carrier signal at an output of the gate-segmented power output stage.

Typically, a power field-effect transistor comprises a plurality of gate fingers and a plurality of drain fingers to realize the required output power. According to the present invention, the gate-segmented power output stage corresponds to a gate-segmented version of this large transistor. To this end, the transistor is segmented into a plurality of smaller power output stage segments. Each of these segments corresponds to a respective part of the gate periphery.

For example, the field-effect transistor may comprise n gate fingers, each having a gate width of l mm. In this respect, it is noted that the gate fingers and drain fingers are elongated structures. The longitudinal direction of the gate finger will be referred to as the width direction. Hence, in the abovementioned example, the gate periphery corresponds to $n \times l$ mm. It is possible to segment the field-effect transistor into p power output stage segments each corresponding to a part of the gate periphery, for example to $n \times l / p$ mm.

Each power output stage segment may be formed by one or more of the plurality of gate fingers. For example, one or more adjacently arranged gate fingers can be grouped into a respective gate segment. Each power output stage segment may then correspond to one or more gate segment.

The one or more gate fingers may be arranged in a pattern consisting of parallel rows, wherein at least one row comprises a plurality of gate fingers, wherein the gate fingers in said at least one row are aligned such that their width directions are in line. Such pattern closely resembles that of an unsegmented power transistor. Furthermore, each row can be associated with an active area that is continuous in the width direction such that a single active area is provided for each row, wherein the active area corresponds to all gate fingers in that row.

The one or more gate fingers extend over a respective active area. More in particular, the one or more gate fingers are separated from the underlying semiconductor by a thin gate oxide. The thickness of the gate fingers is typically very small. To avoid high ohmic losses, thicker metal structures are used that also have the shape of fingers. These structures are connected to the gate fingers and are referred to as gate runners. Similar considerations hold for the drain fingers. These relatively thin fingers each form an ohmic contact to a respective drain region. Thicker finger shaped metal structures are then also used to minimize ohmic losses. As the shapes of the gate runners and gate fingers typically correspond, they will hereinafter both be referred to as gate fingers. Similar considerations hold for the drain fingers and the finger like metal structures connected to them.

Adjacent power output stage segments may share a drain finger.

The power field-effect transistor of the present invention preferably comprises a drain bar from which all drain fingers extend. For the efficient generation of power, it is preferred that the difference in phase delay associated with the various different paths inside the field-effect transistor is kept at a minimum. The present invention particularly relates to RF transmitters of which an operational frequency ranges from 1 GHz to 50 GHz and for which an absolute phase difference for signals propagating via adjacent power output stage segments from the respective power output stage segment input to the drain bar is less than 5 degrees at the operational frequency for each pair of adjacent power output stage segments.

Further embodiments are defined by the dependent claims as attached, and described below in the detailed description, together with the associated advantages.

Short description of drawings

The present invention will be discussed in more detail below, with reference to the attached drawings, in which

Fig. 1 shows a block diagram of a prior-art Cartesian (low-power) fully-digital RF transmitter;

Fig. 2 shows a block diagram of a prior-art polar hybrid-digital/analogue (power) transmitter;

Fig. 3 shows a block diagram of an embodiment of a polar fully-digital power RF transmitter with a gate-segmented power output stage according to the present invention;

Fig. 4 shows a conceptual view of a further embodiment of a power RF transmitter according to the present invention;

Fig. 5 shows a conceptual view of an even further embodiment of an RF transmitter of the present invention;

Fig. 6 shows a conceptual top view of an embodiment of a LDMOS/GaN power die with a fully thermometer gate-segmented power output stage arranged to be edge-connected in accordance with the present invention;

Fig. 7A shows a top view of an embodiment of a LDMOS die with two edge-connected gate-segmented power output stages in accordance with the present invention, and Fig. 7B show a corresponding detailed view;

Fig. 8 shows a top view of an embodiment of a gate-segmented power output stage, implemented in an LDMOS power die and arranged to be flip-chip connected, in accordance with the present invention;

Fig. 9 shows a polar DTX configuration with gate-segmented power output stage featuring an output signal down-conversion path and DPD signal correction, usable in various embodiments of the present invention;

Fig. 10 shows a (multi-phase) Cartesian DTX configuration with a gate-segmented power output stage featuring an output signal down-conversion path and DPD signal correction, usable in various embodiments of the present invention;

Fig. 11 shows a concept of DTX featuring multiple segmented output stages configured as high efficiency transmitter (e.g. N-Way Doherty or N-way outphasing transmitter), usable in various embodiments of the present invention;

Fig. 12 shows a conceptual top view of an embodiment of an LDMOS/GaN power die with flip-chipped CMOS/SOI controller - driver, having two thermometer gate-segmented power output stages configured for Doherty operation in accordance with the present invention.

Description of embodiments

The present invention relates to the general need for low-cost, highly-integrated and energy-efficient transmitter (TX) line-ups for wireless applications like base stations and line drivers such as Data Over Cable Service Interface Specification (DOCSIS) drivers. The currently used analogue-intensive TX solutions in these applications still suffer from poor integration, complicated design logistics, bandwidth limitations due to input and output impedance matching of their active devices, while having inherent linearity/efficiency trade-offs. Fully digital-TX (DTX) solutions can in theory offer higher integration and better RF performance than their analogue counterparts at all of the mentioned aspects. However, so far, all DTX implementations reported, fail to meet the needs of DOCSIS and sub-6 GHz base stations, including the upcoming 5G mMIMO generation in terms of RF output power and efficiency.

Although DTX solutions have been the subject of research investigations over more than a decade, all DTX solutions reported fail to reach the output powers needed for commercial base-stations. This is true even for the new mMIMO base stations that use a lower output power per TX

line-up (e.g. peak-powers ranging from 5W-50W, instead of the traditional macro-cell base station that use peak powers exceeding 100W). For these base stations, in addition to the output power requirements, also an overall average (TX system) efficiency is targeted of 40% or higher.

To understand the output power - efficiency limitations in existing DTX solutions, it is important to know that all presently known Radio-Frequency Digital Analogue Converter (RFDAC) like DTX reported solutions make exclusively use of high-speed (low-voltage) digital CMOS/SOI technologies, since high-speed switching is mandatory for achieving DTX operation at RF frequencies. An example of an RFDAC-like DTX solution implemented in a high-speed, low-breakdown voltage technology can be found in [1] for a Cartesian concept targeting high video bandwidth for its transmit signals at moderate efficiencies. Another example of an RFDAC implementation that aims for higher peak efficiencies can be found in [2], which shows polar operation, an operation which is typically more restricted in terms of video bandwidth. RFDAC DTX concepts that aim for a better compromise between peak efficiency and video bandwidth have been also proposed and are based on the use of multiple RF clock phases [3]. In addition to this also RFDAC DTX concepts that use an efficiency enhancement technique to increase the average efficiency for complex modulated waveforms have been reported, like RFDAC based Doherty [4], as well as RFDAC based out-phasing.

However, the use of these high-speed low-voltage breakdown (e.g. 1.1 – 2.5V) CMOS/SOI technologies also in their output stages, directly limits them in using higher voltage swings at their output stages, and consequently in reaching the required power levels for base stations. Attempts to reach higher output powers with DTX concepts, e.g. by using device stacking in the output stage, power combining, combinations with thicker-gate-oxide devices, or the use of switched capacitor concepts, improves the output power in these works to some extent, but also results in higher circuit complexity in their final output stages (sometimes referred to sub-PAs), with all its associated parasitics. Since reaching good TX system efficiency and output power is strongly negatively affected by these circuit parasitics, all reported DTX solutions reported have been limited in their peak output power capabilities to at most a few watts. These power and efficiency limitations, combined with the limited number of effective bits that can be reached for DTX configurations that aim for higher output powers (limiting the dynamic range) are the reasons that up to date, all base stations are analogue in nature for their TX path, especially when it comes to the final power amplifier. Attempts to digitalize the TX path more and more, e.g. by using RFDAC drivers are on-going but so far all fail to include the final PA stage [6]. Also visionary articles or existing patents, simply give no clue on how to implement the required sub-PAs at sufficient power levels.

In view of this, Fig. 1 shows a block diagram of a prior art Cartesian digital transmitter 50, in which the digital baseband I[n] and Q[n] data are first fed to a digital pre-distorter (DPD) 51. This element passes the pre-corrected digital baseband data to digital decoders 52, 52' that control the clock-gating circuits 53, 53' that utilize a RF carrier 54, and the sub-RFDACs 55, 55' / sub-PAs 56, 56' to generate the analogue output signals I(t) and Q(t), which are combined in combiner 57 and fed to the antenna 58. However, any publically available information on how to reach higher power levels at RF frequencies with high efficiency using these sub-RFDACs 55, 55', 56, 56' is missing.

Note that this also holds for the previously discussed RFDAC based DTX concepts, including, Cartesian, multipolar, as well as results including Doherty, out-phasing and supply modulation (efficiency enhancement techniques).

Fig. 2 shows a block diagram of a prior art hybrid direct digital RF / analogue transmitter (see reference [6]) setup to target higher power levels that can reached with conventional RFDAC based DTX techniques. An input baseband (I, Q) signal is first transformed in a polar signal transformer 11 providing an amplitude and phase signal (ρ, φ). A digital controller 12 transforms the amplitude signal to a digital amplitude code word (ACW) 12a, which is then input in parallel operating AND gates 14 in addition to a phase-controlled output of a local oscillator (LO) 13. The combined outputs of the parallel AND gates 14 provide an analogue signal representation 15 from this digital transmitter setup, which is then fed to drive an analogue amplifier output stage 16, which can be implemented in a high-voltage output stage technology such as Gallium Nitride (GaN) or laterally-diffused metal-oxide-semiconductor (LDMOS) to generate the aimed power level.

The use of an analogue drive signal 15 for the power output stage 16 complicates the use of true switch-mode operation for this output stage. Note that the transition from linear analogue operation to the saturated switch-mode operation is a very non-linear one, which puts high demand on the digital pre-distortion applied. The use of an analogue interface makes the analogue output stage 16 also sensitive for oscillation, which will yield compromises in its design in favour of guaranteeing stability for the output stage 16. In addition, the use of an analogue interface also introduces bandwidth limitations and power scaling issues, due to very low input impedance levels in common-gate operation for a power device, which makes it very sensitive for interconnect parasitics. Or when applying a common-source FET output stage 16, the need for (analogue) input impedance matching arises, which is difficult to achieve over a large bandwidth at higher power levels. Finally, the use of an analogue output stage 16 still demands the use of quiescent current to linearize the AM-AM and AM-PM behaviour of the analogue output stage 16 to acceptable levels. The later aspect also lowers the achievable efficiency in power back-off operation, or in low-traffic scenarios. Consequently, these hybrid implementations do not fully benefit from the potential advantages of true DTX operation.

In other solution attempts, aiming for higher transmit powers, digital driver(s) are used that generate a digital output signal to drive a high-voltage GaN or LDMOS output stage(s) (see e.g. [5]). Since in these configurations the output stages are in digital operation and are fully switched at all times, additional measures are required to set and control their level of generated RF output power. E.g. in out-phasing transmitters the RF output power is controlled by a phase difference between two TX paths. As the digital drivers switch on and off the complete output stage(s) at each RF cycle, even in power back-off operation, the high-speed driver power consumption stays always the same what significantly lowers the achievable system efficiency in these power back-off conditions, or at low traffic scenarios. A similar conclusion holds when considering supply modulation concepts like envelope elimination restoration (EER) that use also switch-mode operation in their output stage.

It is noted that embodiments of the present invention can implement high performance, high power (e.g. with peak powers above 5 W), high resolution with a high number of effective bits, digital RFDAC-like transmitters (DTX). In view of this, it is also important to understand that prior art RF LDMOS/GaN technologies are all optimized for analogue RF power amplifier applications, while CMOS technologies are mostly optimized for digital low-voltage high-speed operations.

In the embodiments of the present invention, an RF transmitter is provided that comprises a gate-segmented power output stage. This output stage comprises a field-effect transistor having a plurality of gate fingers and a plurality of drain fingers that define a gate periphery, the field-effect transistor comprising a plurality of power output stage segments that each correspond to a respective part of the gate periphery and that each have a respective power output stage segment input. Furthermore, the RF transmitter comprises a digital driver having control outputs which are connected to corresponding ones of the respective power output stage segment inputs, the digital driver being configured for individually switching each of the power output stage segments between an on-mode and a cut-off mode in dependence of one or more input signals to obtain a modulated RF carrier signal at an output of the gate-segmented power output stage.

Segmentation of the power output stage, i.e. using a gate-segmented power output stage transistor is applied, rather than using separate transistors as is done in all prior-art low-power RFDACs that are entirely implemented in a single CMOS or SOI technology. This innovative approach will result in much lower parasitics and consequently a much better RF performance at higher power levels for the RF transmitter. This can be implemented by dividing the original gate periphery of a power transistor in smaller pieces, yielding isolated power output stage segments 2, each with its individual connection to the digital driver. The gate periphery can be divided by grouping one or more gate fingers 32 into gate segments 3a, wherein each power output stage segment 2 corresponds to one or more segments. Furthermore, compared to an unsegmented power transistor, the gate fingers of the unsegmented power transistor may be divided into different pieces. Each such piece forms a gate finger 32 for the segmented power transistor.

Note that it is advantageous to implement this when the drain and/or source fingers are still continuous, i.e. shared among the individual devices implementing each power output stage segment 3. The drain fingers are e.g. connected at the output terminal 7 in parallel to each other, while the source is grounded directly by a highly doped sinker or plug that extends through the optionally thinned substrate. For example, the drain fingers 31 are connected using a drain bar 33 from which they all extend, preferably in parallel. This approach yields very low additional parasitics compared to using individual small standard LDMOS transistors. In GaN implementations many vias are used to ground the source, but also here the source and drain fingers can be made best continuous. Additional shielding of the drain from the metal structures connecting the gate elements is advantageous (e.g. by adding metal shields) to reduce the Miller capacitance between the drain finger and gate connection.

Fig. 3 shows a block diagram of an embodiment of a polar RF transmitter 1 according to the present invention. Similar to the exemplary transmitter blocks of the Fig. 2 prior art example, the RF transmitter 1 receives an input baseband (I, Q) signal which is first transformed in a polar

signal transformer 11 providing an amplitude and phase signal (ρ, φ). A digital controller 12 transforms the amplitude signal to a digital amplitude code word (ACW) 12a, which is then input in parallel operating AND gates 14 in addition to a phase-controlled signal of local oscillator (LO) 13. However, in this case, the output 6 of each AND gate 14 is directly input to an associated power output stage segment input 4, i.e. (digital) RF driver output connections 10 are provided between digital driver 5 and gate-segmented power output stage 2. The plurality of AND gates 14 and further elements 11-13 form the digital driver 5, and the plurality of power output stage segments 3 form the gate-segmented power output stage 2 providing the output signal at output terminal 7. As indicated, the drains of the transistors of power output stage elements 3 are electrically connected, for example using a drain bar as described above. Connection between such drain bar and the output terminal 7 can be for example be realized using bond wires.

It is noted that International patent publication WO2011/119315 discloses a digital-to-analogue converter (DAC) having a DAC core section and a power amplifier section. In some embodiments various parts of both the DAC core section and the power amplifier section are implemented in different technologies (CMOS and III-V-technology). The characterising features of the embodiments of the present invention, wherein a digital driver 5 is combined with a gate-segmented power output stage 2 is however not disclosed nor suggested in this publication.

Until now, there was very limited RF base station RF power market demand for the solution provided by the present invention embodiments, since the currently used 4G macro cell base-stations (with peak RF output powers up to several hundred watt), do not dramatically benefit from higher integration and digitalization. This is caused by the fact that output high-power stages in their analogue power amplifiers dominate the overall TX system efficiency, while there are only a few TX line-ups in such a base station (3 to 6). This situation is drastically changed for 5G mMIMO base stations, which will have up to 64 to even 256 TX line-ups, far more than these previous 4G macro cell base stations. The high number of TX line-ups results in a much lower required output power per TX line-up. As a consequence, the overall power consumption of the total TX line-up, rather that the output stage alone, has become much more important. In addition also integration of the TX line-up has become much more important for obvious cost reasons. Both facts motivated a search for new digital transmitter (DTX) solutions.

In prior art systems, switch-mode operation using (unsegmented) power output stages at RF frequencies at large power output levels always proved to be cumbersome. When aiming for high powers, large output stage transistors are required, which have relative large input and output capacitances. In conventional analogue transmitter implementations these large capacitances of the output stage are resonated out, or absorbed within their input and output matching networks. However, when considering digital switch-mode operation, using a large (unsegmented) power device, the related large input capacitance needs to be charged and discharged every RF cycle by the preceding high-speed digital driver. This proves to be a challenging task in practical situations, due to the always present parasitic series inductances between the high-speed driver and the large input capacitance of those power devices, which effectively forms a low-pass filter with related bandwidth restrictions. Furthermore, the use of energy-efficient switch-mode operation, e.g. (inv)

class E or (inv)class-F, demands the harmonic output matching networks to absorb the output capacitance. This is increasingly more difficult at RF frequencies for larger values of the device output capacitance. Consequently, up to now, switch-mode operation for the output stage in base stations has never become popular at higher output powers or RF frequencies. All the considerations above lead to the situation of today, i.e. that the RF base station RF power market still stands on its own, and the preferred operational mode of the RF output stages is analogue (class-B) oriented.

The much smaller individual power output stage segments 3, with related much smaller input capacitances, are less restricted in operating frequency. Depending on the digital baseband data and RF carrier, these segments are also switched between an on-mode and a cut-off mode, i.e. in a digital on/off manner, by the RF driver output connections 10. In an embodiment, the on-mode of a power output stage segment 3 comprises a saturation state of the power output stage segment 3. The saturation state in this context is e.g. a maximum current handling condition of the associated power output stage segment 3, or alternatively formulated, the gate-segmented power output stage 2 is operated in a current-limited operation mode for the associated output stage segments 3. Doing so, for the resulting RF transmitter 1 excellent code word–to-output signal linearity can then be achieved. When using the well-known saturation mode for output stage FET, it is important in this configuration that the “on” level of the individual RF driver output connections 10 always reaches the same voltage level over time. Use of the current limited operation of the (LDMOS / GaN) power output stage segment 3 when it is fully switched on (overdriven at its input) is advantageous, as this will lower the sensitivity on the actual output voltage of the digital driver in its “high” condition. For such embodiment, the controlling input voltage swing may be enlarged, or the V_T of the FET used for implementing the gate-segmented power output stage 2 can be drastically lowered, such that the FET enters current-limited mode of operation even with low driver voltage swings. This can be done by the making the gate oxide thinner and engineering the doping profiles of the FET.

In a further group of embodiments, the digital driver 5 and gate-segmented power output stage 2 are implemented in different semiconductor technologies. In the exemplary embodiment shown in Fig. 3 e.g. the entire digital driver 5 part can be implemented in a different semiconductor technology than the plurality of power output stage segments 3 forming the gate-segmented power output stage 2. This allows using semiconductor technologies that are optimized for that specific part of the RF transmitter 1. E.g. the digital driver 5 comprises a CMOS digital driver, i.e. the digital driver 5 is provided in high-speed CMOS technology, enabling to provide associated signals on the RF driver output connections 10. In a further embodiment, the gate-segmented power output stage 2 comprises transistors of the laterally diffused metal-oxide-semiconductor (LDMOS) transistor type, and/or a GaN-based field-effect transistor type, allowing a high power output by the RF transmitter 1. Note that further III-V semiconductor technology may be used. Additionally or alternatively, other V_T-shifted technology allowing the transistor(s) of the power output stage elements to be driven by the signals on the high speed RF driver output connections 10 may be used.

The transistors of the gate-segmented power output stage 2 can be configured to have a threshold voltage for allowing the digital driver 5 to individually switch each of the power output stage segments 3 between an on-mode and a cut-off mode in dependence of the control outputs 6. Note that various options are available to obtain the needed V_T-shift for the power device, which as such are known to the person skilled in the art (e.g. using a different channel doping or thinner gate oxide).

As an alternative implementation, the RF transmitter 1 further comprises a plurality of level shifters connected in between the control outputs 6 of the digital driver 5 and the power output stage segment inputs 4 of the gate-segmented power output stage 2. These level shifters are particularly useful when driving a GaN implemented segmented power device. A person skilled in the art can implement such level shifters as part of the driver part 5 or as part of the gate-segmented power output stage 2.

The digital driver 5 can be provided in a first semiconductor die 8, and the gate-segmented power output stage 2 can be provided in a second semiconductor die 9, the first semiconductor die 8 being different from the second semiconductor die 9. The digital driver 5 may comprise a plurality of output terminals 8a associated with the control outputs 6, and the gate-segmented power output stage 2 may comprise a plurality of input terminals 9a associated with each power output stage segment input 4. The RF transmitter may further comprise connections 10 between respective output terminals 8a on the first semiconductor die 8 and associated input terminals 9a on the second semiconductor die 9.

Fig. 4 shows a conceptual view of a further embodiment of the RF transmitter 1 of the present invention, showing a part of the RF transmitter 1 architecture, using a gate-segmented power output stage 2 configured for edge coupling. Shown is an input (in this embodiment as a digital serial bus 12a input) which is connected to a first semiconductor die 8, implementing (part of) the digital driver 5 as discussed above. Output terminal 8a on the first semiconductor die 8 is connected to input terminals 9a on the second semiconductor die 9 by connections 10. A transmitter output terminal 7a in connection with a combiner terminal 22 is connected to segment output terminals 9b via connections 24. Typically, output terminals 9b are grouped in a drain bar. As indicated, the first semiconductor die 8 is implemented as CMOS or Silicon-on-insulator (SOI) technology, and the second semiconductor die 9 as LDMOS or GaN technology. To allow the connections 10 to be made, the output terminals 8a on the first semiconductor die 8 and the input terminals 9a on the second semiconductor die 9 are provided in an edge part of the first semiconductor die 8 and second semiconductor die 9, respectively. In this implementation, all output terminals 8a associated with the control outputs 6 are preferably located on the edge of the first semiconductor (CMOS) die 8, and the input terminals 9a associated with the power output stage segment inputs 4 are on the edge of the second semiconductor (LDMOS) die 9. Fine pitch staggered bond wires may be used to connect the dies 8, 9. Note that the bond wires may be specifically oriented in order to minimize inductive coupling. For example, the connecting bond wires 10 can be kept short (e.g. below 0.7 mm) and/or alternating bond wire shapes can be used. The

shape of the bond wires 10 can be made alternating to lower the mutual coupling that gives rise to bit-bit interactions.

As shown in the exemplary embodiment of Fig. 4, a pitch distance p_1 between the output terminals 8a on the first semiconductor die 8 is substantially equal to a pitch distance p_2 between the input terminals 9a on the second semiconductor die 9, allowing to make a significant number of direct connections between associated output terminals 8a and input terminals 9a. Note that a high number of connections allows using more output stage segments, which is beneficial for the linearity and will lower the quantisation noise.

In addition, ground connections may be provided between the first semiconductor die 8 (or digital driver 5) and the second semiconductor die 9 (gate-segmented power output stage 2/ power output stage segments 3), as part of or in addition to the connections 10. This will avoid unpredictable ground path inductances between the digital driver 5 and the to the power output stage segments 3, which otherwise could result in timing and voltage level differences when driving the various power output stage segments 3.

As an alternative, the connections 10 may comprise fine pitch interconnect film connections. (as for example can be found in reference [7]), or the connections 10 may comprise flip-chip type connections. This allows a configuration of the RF transmitter 1 with a CMOS or SOI semiconductor (controller/driver) die 8 on top of a LDMOS or GaN semiconductor die 9, as shown in the embodiment of Fig. 5, showing a conceptual view of an even further embodiment of the RF transmitter 1 of the present invention. This particular embodiment example has two output terminals 7a, 7a' (and corresponding power combiner terminals 22, 22', via connections 24), e.g. to implement a dual TX line-up structure of the RF transmitter 1 (e.g. with two separate gate-segmented power output stages 2). Such a hardware configuration could be used to implement e.g. a push-pull, a two-way Doherty, outphasing, or dual RF carrier TX configuration, e.g. to improve respectively in wideband performance, power back-off efficiency, or multiband operation. Using a flip-chip connection, many more signal ground connections between the digital driver 5 and the gate-segmented power output stage segments 3 are possible. This will also make the signal paths as short as possible and very well defined. Using a fine pitch (see the pitch p_2 shown in Fig. 5) the number of interconnects 10 can be made really large, allowing (but not necessarily restricted to) the use of segmented output stages 2 with thermometer bits only. It is advantageous in such a thermometer approach that conventional ESD protection (usually in the form of diodes near the output terminals 8a/input terminals 9a) is circumvented or drastically reduced. This will avoid too much capacitive loading of the digital driver 5 which would yield increased power consumption of the digital driver 5. In other words, the output terminals 8a and input terminals 9a are directly connected to the control outputs 6 and power output stage segment inputs 4, respectively, i.e. without normally present ESD protection circuitry.

In an even further embodiment, the RF transmitter 1 further comprises external terminals 21 provided on the second semiconductor die 9. Where necessary, one or more of these external terminals 21 are routed to the first semiconductor die 8 via the second semiconductor die 9, i.e. all external connections of the RF transmitter 1 are provided on the second semiconductor die 9.

In the embodiment shown in Fig. 5, the RF transmitter further comprises a grounded MOS capacitor component 23, connected to the second semiconductor die 9 via connections 25. This embodiment uses a gate-segmented power output stage 2 configured for flip-chip interconnect. The inductance formed by bond wires 25 can be used to resonate out the output capacitance of the segmented power device at or close to the operational frequency of the RF transmitter 1.

Fig. 6 shows a top view of an embodiment of a gate-segmented power output stage 2 as useable in embodiments of the present invention, specifically for an embodiment having two dies 8, 9 with bond wires as connections 10. The specific example of the second semiconductor die 9 shows a gate-segmented power device intended for edge connection using thermometer weighted elements only. In this example configuration each drain finger 31 of the gate-segmented power output stage 2 is embedded between two gate fingers 32 that can be each individually controlled as independent gate segment 3a. Moreover, each power output stage element 3 comprises a single respective gate segment 3a. All drain fingers 31 are connected to a drain bond bar 33 which is used to connect to an (external) matching network or power combiner. In order to obtain a compact power device layout with a sufficient number of thermometer bits, a high density edge connection with a fine pitch for the interconnect is required. Besides the gate bond pads 34 also bond pads 35 for the ground are provided in order to provide a well-defined return path for the driver current. Note that the ground bond pads 35 can be hard grounded using through-wafer vias (e.g. in GaN technology) or using highly doped through-wafer plugs as available in LDMOS technology. To achieve the highest signal quality of the digital transmitter it is beneficial to have as many thermometer weighted gate segments 3a / power output stage elements 3 as possible and to activate the gate segments 3a / power output stage elements 3 in a monotonic sequence e.g. from left to right as indicated in the Fig. 6 (arrow 36), or vise-versa from right to left. As a refinement on the use of pure thermometer weighted gate segments, one could consider the use on non-linear sizing of these segments e.g. by making the gate width of segments that are activated only at the higher amplitudes somewhat larger to compensate for the compression phenomena of the overall segmented power stage at these larger drive levels. This reduces the burden for linearization and may result in a less complex DPD or may even allow DPD free operation.

To further increase the output signal quality and lower the effective quantization noise of the proposed digital TX implementation, up-sampling, interpolation, as well as, dithering techniques can be applied. Especially, dithering based techniques proved to be very effective in the proposed TX architecture, when applied on the latest activated (thermometer) element 3a in the thermometer controlled device. By toggling this element between its on and off state in a smart manner (e.g. by using delta-sigma or pulse-density modulation), with a toggling rate than is significantly higher than the actual video bandwidth of the TX signal, on average, effectively intermediate levels in the otherwise quantized digital TX output signal can be added, which directly lowers the effective TX output quantization noise. This allows to further enhance the dynamic range of the RF transmitter 1, the digital driver 5 is arranged to implement dithering of one or more bits of the gate-segmented power output stage 2 in a further embodiment.

In addition to the segmented power device fingers (i.e. gate segments 3a), an extra shielded connection 37 (with overlying shielding 39) can be provided to pass the output signal from the drain bond bar 33 back to the controller side such that it can be monitored for its quality (through metal bond pad 38). This is very useful when also implementing a digital pre-distortion function on the digital controller chip. Doing so will provide a much higher system integration at minimal cost, compared to the current state-of-the art solutions. Note that the extra shielding 39 is needed to preserve the signal quality of the monitored output signal in this electronically harsh environment.

Fig. 7A shows a top view of an embodiment of a gate-segmented power output stage 2 as useable in embodiments of the present invention, specifically for an embodiment having two dies 8, 9 with bond wires as connections 10. Fig. 7B shows a corresponding schematic detailed view. The specific example of the second semiconductor die 9 shown has two banks (one indicated by D) of gate segments 3a / power output stage elements 3, implemented in LDMOS semiconductor technology. The configuration that is shown here uses per drain finger 31 only one control connection 34 that drives both the left and right gate finger 32 as such acting as one gate segment. In this example each bank features fifteen thermometer bits and seven binary weighted bits, the latter shown in more detail in Fig. 7B. Note that in contrast with the embodiment in Fig. 6 the gate fingers 32 left and right of a drain finger 31 share the same driver connection 34 connected to input terminal 9a. In the example built, the digital driver 5 was implemented in CMOS technology using thick-oxide transistors, facilitating a maximum output voltage swing of e.g. 2.5 V. A downwards V_T-shift has been used in the implementation of the power output stage segments 3 on the second semiconductor (LDMOS) die 9 to make them compatible with the voltage-swing of their associated CMOS drivers. In such a configuration implemented using two separate dies 8, 9, both dies 8, 9 require ESD protection, leading to extra parasitic interconnect capacitance at each side. In this example, the input capacitance of a single power output stage segment 3 is 1.1 pF. Per interconnect a total of 1.3 pF needs to be attributed to ESD protection diodes. The CMOS 2.5 V thick-oxide output drivers are dimensioned for maximum system efficiency. Further increasing their size yields faster rise and fall times, enhancing the LDMOS drain efficiency, but at the cost of increased driver capacitances and driver power dissipation, which eventually degrades the overall efficiency of RF transmitter 1. Future implementations might feature power devices with an even lower V_T, such that thin-oxide very high-speed devices (voltage swing ~1.1V) can be used to drive them, extending the operation frequency range even more. To reduce the impact of these capacitances, a practical RF transmitter 1 architecture limits its number of connections 10, favouring binary-weighted output-stage devices. Nevertheless, for linearity reasons, thermometer coding is considered more advantageous.

In the proposed dual RF transmitter 1 line-up demonstrator shown in Fig. 7A, two different coding techniques are used, namely binary coding and thermometer coding. For the most significant bits (MSBs), thermometer coding is used, whereas for the least significant bits (LSBs), binary coding is used. More in particular, in the Fig. 7A embodiment, a total LDMOS gate width (W_{gtot}) of 41.5 mm has been segmented into two banks, each bank having 15 thermometer-coded most significant bits (MSBs) (one indicated by A and the combination of MSBs denoted by 100) and 7 binary-weighted

least significant bits (LSBs) (one indicated by B and the combination of LSBs denoted by 101). In this implementation, the lowest LSBs (in the middle and denoted by 102) have been implemented twice to create some redundancy.

The power outputted by one bank of gate-segmented power output stage 2 can be computed using $Wm \times P1 + Wn \times 2^{-n} \times P1$, wherein $Wm\ (m=1\ldots15)$ represents the weight factor for the mth power output stage element 3 / gate element 3a that corresponds to the thermometer code, $Wn\ (n=1\ldots7)$ represents the weight factor for the nth power output stage element 3 / gate element 3a that corresponds to the binary code, and $P1$ the power outputted by a power output stage element 3 / gate element 3a corresponding to the thermometer coding. The factor 2^{-n} describes how the gate finger width of a power output stage element 3 / gate element 3a corresponding to binary coding should be chosen with respect to the gate finger width of a power output stage element 3 / gate element 3a corresponding to thermometer coding. Moreover, weight factors Wm and Wn can typically either be 0, corresponding to the cut-off mode, or 1, corresponding to the on-mode.

The 15 power output stage elements 3 / gate elements 3a corresponding to the thermometer coding allow 16 different values to be generated, whereas the 7 power output stage elements 3 / gate elements 3a corresponding to the binary coding allow 128 different values to be generated. Hence, in total 128 x 16 = 2048 different values can be generated, which corresponds to a binary word of 11 bits.

For the binary-weighted bits, the drain is cut in two mutually isolated parts. A first part, indicated by L1-L4, indicates the part of the drain finger that cooperates with gate fingers 32 for the purpose of generating signals. The other part, which lies in line with the first part, is connected to ground, for example using a via 103. The use of these shorted drain lines equalizes the input (gate) capacitances of all segments.

For the n^{th} LSB, the effective LDMOS gate width is 2^{-n} times that of a thermometer MSB. For example, in Fig. 7B, L4 defines the effective gate width of the gate fingers corresponding to the thermometer coding. Moreover, L4=2xL3=4xL2=8xL1.

In terms of linearity, thermometer coding is preferred as the binary coding scheme requires considerable switching of RF currents in view of the large amount of changes between sequential numbers. For example, changing between binary code 0111 and 1000 involves changing 4 bits. However, compared to binary coding, thermometer coding requires a large number of power output stage elements. The Applicant has found that combining thermometer coding for the MSBs and binary coding for the LSBs yields excellent results despite the limited number of inputs.

Furthermore, it is noted that the two resulting identical RF transmitter 1 line-ups of the realized demonstrator can operate fully independently of each other, allowing various TX-operation modes, such as, but not limited to, polar, (multi-phase) Cartesian, single-ended, push-pull, Doherty and outphasing.

The example shown in Fig. 7A has a number of features. For example, at least a part of the power output stage segments 3 has similar transistor dimensions, and the digital driver 5 comprises a thermometer bit style interface to the gate-segmented power output stage 2. This has an advantage of avoiding time alignment problems with the drivers with their unavoidable inductive

interconnects (e.g. connecting bond wires 10), since all the (capacitive) loading of each digital driver can be kept identical. In a thermometer bit style interface all power output stage segments 3 may have the same size and related loading capacitance. In embodiments in which not all power output stage segments 3 have the same size, extra loading capacitances can be added to the smaller binary bits, to equal the total capacitance of the thermometer bits. This can be implemented as discussed above in conjunction with the binary coding. It is noted that this binary coding can be optional.

With respect to the example in Fig. 4 and the implementation example shown in Fig. 6, further observations can be made. These implementations use a segmentation that is particularly applicable in an edge-connected configuration of the digital driver 5 and the power output stage segments 3 (e.g. as given in Fig. 4). Alternatively, several in-line gate fingers 32 can be used in combination with a single drain finger 31, as is depicted in the top view shown in Fig. 8. Compared with an unsegmented transistor, it can be observed that the gate fingers of the unsegmented transistor have been segmented into a plurality of gate fingers 32. These gate fingers 32 are arranged in a pattern of parallel rows. Each row extends in parallel to the drain fingers 31 and comprises a plurality of gate fingers 32. This configuration is most applicable to flip-chip approaches as discussed above with reference to Fig. 5 as more segments can be used when compared to the edge-connection of figure 7A.

In the configuration example of Fig. 8, the output stage drain fingers 31 are embedded between two source contacts 45 while being surrounded by gate fingers 32 that are electrically isolated from each other. Each gate finger 32 has a flip-chip gate bump connection 44 to the CMOS digital driver 5 on the first semiconductor die 8 which is placed on top of the second semiconductor die 9. Additional shielding plates between the drain – gate connected structures (bond pads) may be placed to lower the impact of Miller like capacitances. Due to the small dimensions of the flip-chip connections 10, both the capacitive as well as inductive interconnect parasitics per segment are minimized, allowing higher RF operating frequencies, finer segmentation and lower bit-to-bit interaction yielding better linearity. If ESD diodes can be avoided, the capacitive loading per control output 6 of digital driver 5 is drastically reduced. This combined with the fact that the individual power output stage segments 3 can be made much smaller, while still having a comparable total gate width for the entire gate-segmented power output stage 2, helps in reaching higher operating frequencies.

Since the loading capacitances per power output stage segment 3 in this case are much smaller, tapered buffers on the CMOS digital driver 5 can have less stages. This is especially true if the use of ESD diodes can be avoided or minimized) Shorter tapered buffers yield less delay variation with the driver supply voltage. This is beneficial in achieving a better quality of the spectrum of the output signal 7.

In RF power LDMOS technologies, the (continuous) sources of an output stage are hard grounded by a highly-doped through-substrate plug, as well as, the use of a thinned substrate (typically ~50um). Consequently, by using extra (source/ground) connections in the LDMOS die, better supply decoupling of the CMOS digital driver 5 components 14 can be achieved, yielding

lower supply induced variations in the output voltage on the driver control outputs 6, improving the quality of the output spectrum of the overall digital RF transmitter 1. By using in addition, high density capacitors on the power die 9 as shown in Fig. 8, in combination with additional supply contacts 47 (indicated with a V) for the driver, this can be improved even further.

In Fig 8, gate fingers 32 are positioned in line. More in particular, the gate fingers 32 directly on top of the gate oxide, are in line. Each row of in-line gate fingers 32 is associated with a single continuous active area. In Fig. 8, each drain finger 31 corresponds to two adjacent active areas.

Various activation sequences are possible for the power output stage segments 3, allowing to obtain a close to monotonic ACW to RF-output signal transfer. In view of this a row by row activation gives the best performance (as indicated by arrow 46 in Fig. 8).

In an even further embodiment, output signal observation and control (e.g. in the form of an on-chip digital pre-distortion (DPD) component) can be added, as it is possible to directly connect to the output terminal 7a to monitor the quality of the output signal 7 (e.g. through a contact 48 in Fig. 8), down sample it and feed it to a DPD component that is arranged to correct for hardware imperfections. As such a fully integrated power digital RF transmitter 1 can be established within very small dimensions. Finally to allow bonding of the drain bond bar 33 for the output matching, some distance (D) between the flip-chipped controller chip 8 (overlying the gate bump connections 44 in the Fig. 8 embodiment) and the drain bond bar 33 will be needed.

Fig. 9 shows a more detailed block diagram of an embodiment of a polar RF transmitter 1 using gate segmentation in the output stage in accordance with the invention featuring an optional feedback path and on-board digital pre-distortion (DPD), usable in embodiments of the present invention. The digital driver 5 of the RF transmitter 1 is e.g. implemented in a first semiconductor die 8, and the gate-segmented power output stage 2 in a second semiconductor die 9.

Similar to the exemplary transmitter blocks of the Fig. 1 and Fig. 2 prior art examples, the RF transmitter 1 receives an input baseband (I, Q) signal, which is pre-corrected by the DPD block 61. Next the corrected I and Q signal is up-sampled and filtered using interpolation in processing block 62. The resulting new I and Q data representation is transformed in a polar signal transformer (CORDIC) 63 providing the digital amplitude and phase representations (ρ, φ). A digital controller 64 transforms this amplitude to a digital amplitude code word (ACW) 12a, which is used as input for the in parallel operating decoders 65, (that in their simplest implementation can be implemented as logic AND gates 14, see Fig. 2) and combined with the polar phase-modulated clock signal provided by phase modulator 66. The output of the decoders 65 is fed to digital on-chip buffers 67 that are able to drive in a digital like fashion the plurality of individual power output stage segments 3.

The resulting output power of the gate-segmented power output stage 2 device is delivered to the output terminal 7 (e.g. connected to the drain bond bar 33 of the Fig. 6 embodiment of second semiconductor die 9), which in turn is connected to a matching or power combiner network, which as such is known to the person skilled in the art.

To ensure a monotonic ACW-output power relation, the activation to the power output stage segments 3 is best done in a monotonic sequential manner as indicated by arrow 36 in Fig. 9 (see

also Fig. 6). The polar phase used for the decoders 65 is originating from the external RF carrier or reference clock, which is used on-chip in the clock/phase generator 68 to create the various digital clocks for the different sub-blocks. By creating multiple phase shifted clocks in combination with the digital phase representation φ, a (low-power) Cartesian harmonic rejection RFDAC with output limiter concept (see reference [4], the relevant contents of which are incorporated herein by reference) can be used to implement the wideband phase-modulator 66 that provides the actual polar phase to the decoders 65. A fraction of the output signal present at the drain bar 33, is fed back though a shielded structure on the power die 9 via shielded metal connection 37 (and metal bond pads 38), to the CMOS / SOI implemented digital driver 5. After sampling / down conversion (in sampler/down converter block 69) this information is used to train the (on-chip) DPD 61, or (optionally) can be shared to an external DPD correction unit e.g. as baseband IQ data. This external DPD unit in turn would alter the incoming IQ baseband data stream of the controller-driver IC.

The conceptual visualisation in Fig. 9 of the interconnections 10 between the digital driver 5 and the gate-segmented power output stage 2 on the LDMOS / GaN device 9 is shown for an edge-coupled configuration similar to that of Fig. 6. Extra ground / source contacts 35 have been added to better define the current return paths and improve the bias decoupling of the digital buffers 67, both needed to lower AM-PM distortion of the digital power transmitter 1. The previously described concept can also be used for a flip-chip version (e.g. as shown in Fig. 5) using the segmentation as previously shown in Fig. 8. Note that the monitor connection (i.e. shielded metal connection 37) of the TX output signal in a flip-chip version can be done in a more direct way by a simple bump connection. Furthermore, when using a GaN gate-segmented output stage, a level shifter needs to be included in the buffer implementation, to adopt for the required negative potential of the GaN gate.

Fig. 10 shows a more detailed block diagram of an embodiment of a (multi-phase) Cartesian RF transmitter 1 in accordance with the present invention using gate-segmentation in the output stage 2 featuring an optional feedback path 37 and on-board digital pre-distortion (DPD) 61. Similar to the previously described Fig. 9 embodiment and the exemplary transmitter blocks of the Fig.1 and Fig. 2 prior art examples, the RF transmitter 1 receives an input baseband (I, Q) signal, which is pre-corrected by the DPD block 61. Next the corrected I and Q signal is up-sampled and filtered using interpolation in processing block 62. The resulting new I and Q data representation is fed to a digital encoder 71, which controls the quadrant / segment selector 72, which in turn provides/ passes the actual vector phase φ_1 and φ_2 of the active quadrant / segment (see also reference [3], the relevant contents of which are incorporated herein by reference). The digital encoder 71 provides the interleaved amplitude I'Q' code word to the decoders 73, which combine it with the proper vector phases. The output of the decoders 73 are fed to digital on-chip buffers 74 that are able to drive in a digital like fashion the plurality of individual power output stage segments 3. The resulting (vector) summed output power of the gate-segmented power output stage 2 is delivered to the output terminal 7 (e.g. connected to the drain bond bar 33 of the Fig. 6 embodiment

of second semiconductor die 9), which in turn is connected to a matching or power combiner network, which as such is known to the person skilled in the art.

To ensure a monotonic ACW-output power relation the activation to the gate segments 3a is best done in an I'Q' interleaved sequential manner as indicated by arrow 36 in Fig. 10, yielding a sequential and monotonic activation of the power output stage segments 3. The vector phases used for the decoders 73 are originating from the external RF carrier or reference clock, which is used on-chip in the clock/phase generator 75 to create the various digital clocks for the different sub-blocks. By creating multiple phase-shifted clocks (e.g. eight as in reference [3]), the quadrant / segment selector 72 can select the proper /active vector phases, based on the control provided by the digital encoder 71 that makes its decision using the interpolated IQ data. A fraction of the output signal present at the drain bar 33, is fed back though a shielded structure on the power die 9 via shielded metal connection 37 (and metal bond pads 38), to the CMOS / SOI implemented digital driver 5. After sampling / down conversion (in sampler/down converter block 69) this information is used to train the (on-chip) DPD 61 or (optionally) can be shared to an external DPD correction unit (e.g. as baseband IQ data). This external DPD unit in turn would alter the incoming IQ baseband data stream of the controller-driver IC.

The conceptual visualisation in Fig. 10 of the interconnections 10 between the digital driver 5 and the gate-segmented power output stage 2 on the LDMOS / GaN device 9 is shown for an edge-coupled configuration. Extra ground / source contacts 35 have been added to better define the current return paths and improve the bias decoupling of the digital buffers 67, both needed to lower AM-PM distortion of the digital power transmitter 1. The previously described concept can also be used for a flip-chip version (e.g. as shown in Fig. 5) using a segmentation as previously shown in Fig. 8. Note that the monitor connection (i.e. shielded metal connection 37) of the TX output signal in a flip-chip version can be done in a more direct way by a simple bump connection. Furthermore, when using a GaN gate-segmented output stage, a level shifter needs to be included in the buffer implementation, to adopt for the required negative potential of the GaN gate.

Fig. 11 shows a high-level diagram of the previously described techniques in a more energy-efficiency embodiment of the proposed RF transmitter 1 using multiple gate-segmented power output stages 2 with an optional feedback path 37 and on-board digital pre-distortion (DPD), according to the present invention. Note that such a configuration can be used to implement a (N-way) Doherty (similar as is done for low powers in reference [4]) or (N-way) Outphasing digital RFDAC-like transmitter configuration, which provides improved efficiency in power back-off operation when working with complex modulated signals as is the case of base station applications.

Similar to the previously described Fig. 9 and the exemplary transmitter blocks of Fig. 1 and Fig. 2 prior-art examples, the overall RF transmitter receives an input baseband (I, Q) signal and an RF carrier/ RF clock reference, which is fed to a digital controller 81 implemented in high-speed CMOS/SOI technology (first semiconductor die 8), that handles the activation and control of the various DTX drivers 5 with proper phase relations to control a plurality of gate-segmented power output stages 2 implemented on a LDMOS or GaN power die 9. These power output stages 2 are connected to a power combining network 91 (on or off-chip) which provides the transmitter signal

to output terminal 7, and as such, with the proper digital control, can provide energy efficient Doherty or (N-way) out-phasing operation or a mixture of both. When using a single gate-segmented power output stage 2, supply modulation can be used as energy efficiency enhancement technique. Optionally a baseband IQ representation of the actual generated TX signal can be provided off-chip for use in an external DPD.

Fig. 12 gives a detailed conceptual implementation of a two-way digital Doherty RF transmitter 1 using two gate-segmented power output stages 2 (indicated by the dashed boxed contours) in a flip-chip mounting configuration with a high-speed CMOS/SOI digital driver 5 that is placed on top of an LDMOS / GaN power die 9 according to an further embodiment of the present invention. In this particular embodiment, since the CMOS digital driver 5 is flip-chip connected, all bias supplies, RF clocks, IQ data connections and RF output matching / power combiner connections need to be routed over the LDMOS / GaN power die 9.

This particular embodiment features two differential high-speed serial data interfaces (e.g. SerDes, or LVDS), of which one is used to provide baseband IQ signal (connections 82 DX1+, DX1-) to the digital RF transmitter 1, and one is used to extract a down converted IQ representation of the generated digital TX output signal and feed it to an external DPD unit (connections 83 DX2+, DX2-). The RF carrier / RF clock reference is also fed to the digital controller chip (first die 8), which is implemented in high-speed CMOS/SOI technology, using the differential connections 84 RFC+, RFC-. In addition, four control lines 85-88 are provided; C1, C2, C3, and C4 that are used to reset, load data in controlling registers (via e.g. SPI) and/or put the RF transmitter 1 in complete off-mode. Furthermore the positive supply voltages for the digital driver 5 (V_{cont}) and drivers / buffers (V_{driv}) are provided over the power die 9. This is done at multiple points as shown in Fig. 12 to allow for the best possible AC decoupling of these voltages. All the ground connections (S), extra driver supply connections (V) and contacts for the segmented gates (G) as previously given in Fig. 8 are also used to connect to the first semiconductor die 8, but are not explicitly shown in this Fig. 12. The same holds for high density bias decoupling capacitors (for V_{drive} and V_{cont}) that can be implemented in the power die 9 MMIC, also not shown to maintain the readability of this Fig. 12. The gate-segmented power output stages 2 use a bond wire array 92 connected to the drain bond bar 33, in combination with a high-density capacitor 93 on the LDMOS die 9 to provide AC choke inductors to resonate out the output capacitance of the gate-segmented power output stages 2. The same connection is used to provide the drain supply to the gate-segmented power output stages 2. The RF output signal of the main device ($RF_{outmain}$ 94), as well as the RF output signal of the peak device ($RF_{outpeak}$ 95), can be fed to an external power combiner (e.g. one that is implemented on the PCB for configurations that target relative low TX operating frequencies), to obtain the desired output signal RF out. Alternatively, one can use also “long” bond wires 96 to connect the $RF_{outmain}$ 94 with $RF_{outpeak}$ 95 to implement a “lumped” Doherty power combiner, this later configuration is particular useful when targeting higher operating frequencies. When aiming to use different voltage potentials for the main and peak device, e.g. to extend the high efficiency power back-off range, these bond wires 96 should be connected to the $RF_{outmain\_AC}$, which provides DC isolation through the use of

the capacitor 97. Note that some distance between the boundaries of the CMOS controller (first die 8) and the actual bonding locations will be needed in practical implementations (indicated by D).

The above described configuration offers a highly integrated, highly-efficient digital high power transmitter 1 with a large functionally and re-configurability, and offers several advantages over current-state of the art transmitters. Extended versions of the described configuration, based on the use of segmented power devices are possible and can related to: 3-way or N-way Doherty configurations, inverted Doherty configurations, mixed-mode out-phasing configurations, supply modulation concepts, as well as, push-pull variations of these concepts that aim to enhance on bandwidth or spectral purity.

The present invention embodiments can also be described by the following numbered and interrelated embodiment clauses:

Embodiment 1. An RF transmitter (1), comprising:

a gate-segmented power output stage (2) comprising a field-effect transistor having a plurality of gate fingers (32) and a plurality of drain fingers (31) that define a gate periphery, the field-effect transistor comprising a plurality of power output stage segments (3) that each correspond to a respective part of the gate periphery and that each have a respective power output stage segment input (4); and

a digital driver (5) having control outputs (6) which are connected to corresponding ones of the respective power output stage segment inputs (4), the digital driver (5) being configured for individually switching each of the power output stage segments (3) between an on-mode and a cut-off mode in dependence of one or more input signals to obtain a modulated RF carrier signal at an output (7) of the gate-segmented power output stage (2).

Embodiment 2. The RF transmitter (1) according to embodiment 1, wherein one or more adjacently arranged gate fingers (32) are grouped into a respective gate segment (3a), wherein each power output stage segment (3) corresponds to one or more gate segments (3a).

Embodiment 3. The RF transmitter (1) according to embodiment 1 or 2, wherein the one or more gate fingers (32) are arranged in a pattern consisting of parallel rows, wherein at least one row comprises a plurality of gate fingers (32), wherein the gate fingers (32) in the at least one row are aligned such that their width directions are in line.

Embodiment 4. The RF transmitter (1) according to embodiment 3, wherein each row is associated with an active area that is continuous in the width direction such that a single active area is provided for each row, wherein the active area corresponds to all gate fingers (32) in that row.

Embodiment 5. The RF transmitter (1) according to any one of embodiments 1-4, wherein adjacent power output stage segments (3) share a drain finger (31).

Embodiment 6. The RF transmitter (1) according to any one of embodiments 1-5, wherein all drain fingers (31) extend from a drain bar (33).

Embodiment 7. The RF transmitter (1) according to embodiment 6, wherein an operational frequency of the RF transmitter (1) ranges from 1 GHz to 50 GHz, and for which an absolute phase difference for signals propagating via adjacent power output stage segments (3) from the respective power output stage segment input (4) to the drain bar (33) is less than 5 degrees at the operational frequency for each pair of adjacent power output stage segments (3).

Embodiment 8. The RF transmitter according to any one of embodiments 1-7, wherein the on-mode of a power output-stage segment (3) comprises a saturation state of the power output-stage segment (3).

Embodiment 9. The RF transmitter according to any one of embodiments 1-8, wherein the digital driver (5) and gate-segmented power output stage (2) are implemented in different semiconductor technologies.

Embodiment 10. The RF transmitter according to embodiment 9, wherein the digital driver (5) comprises a CMOS or SOI implemented digital driver.

Embodiment 11. The RF transmitter according to embodiment 9 or 10, wherein the gate-segmented power output Embodiment stage (2) comprises transistors of a laterally diffused metal-oxide-semiconductor (LDMOS) transistor type, and/or a GaN-based field-effect transistor type.

Embodiment 12. The RF transmitter according to embodiment 11, wherein the transistors of the gate-segmented power output stage (2) are configured to have a threshold voltage for allowing the digital driver (5) to individually switch each of the power output stage segments (3) between the on-mode and cut-off mode in dependence of the control outputs (6).

Embodiment 13. The RF transmitter according to any one of embodiments 1-12, further comprising a plurality of level shifters connected in between the control outputs (6) of the digital driver (5) and the power output stage segment inputs (4) of the gate-segmented power output stage (2).

Embodiment 14. The RF transmitter according to any one of embodiments 1-13, wherein the digital driver (5) is provided in a first semiconductor die (8), and the gate-segmented power output stage (2) is provided in a second semiconductor die (9), the first semiconductor die (8) being different from the second semiconductor die (9),

the digital driver (5) comprising a plurality of output terminals (8a) associated with the control outputs (6),

the gate-segmented power output stage (2) comprising a plurality of input terminals (9a) associated with each power output stage segment input (4),

further comprising connections (10) between respective output terminals (8a) on the first semiconductor die (8) and associated input terminals (9a) on the second semiconductor die (9).

Embodiment 15. The RF transmitter according to embodiment 14, wherein the output terminals (8a) on the first semiconductor die (8) and the input terminals (9a) on the second

semiconductor die (9) are provided in an edge part of the first semiconductor die (8) and second semiconductor die (9), respectively.

Embodiment 16. The RF transmitter according to embodiment 14 or 15, wherein the connections (10) comprise bond wires.

Embodiment 17. The RF transmitter according to embodiment 14 or 15, wherein the connections (10) comprise interconnect film connections.

Embodiment 18. The RF transmitter according to embodiment 14 or 15, wherein the connections (10) comprise flip-chip type connections.

Embodiment 19. The RF transmitter according to any one of embodiments 14-18, wherein the connections (10) further comprise a plurality of ground connections between the first semiconductor die (8) and second semiconductor die (9).

Embodiment 20. The RF transmitter according to any one of embodiments 14-19, wherein the output terminals (8a) and input terminals (9a) are directly connected to the control outputs (6) and power output stage segment inputs (4), respectively.

Embodiment 21. The RF transmitter according to any one of embodiments 14-20, wherein a pitch distance (p_1) between the output terminals (8a) on the first semiconductor die (8) is substantially equal to a pitch distance (p_2) between the input terminals (9a) on the second semiconductor die (9).

Embodiment 22. The RF transmitter according to any one of embodiments 14-21, further comprising external terminals (21) provided on the second semiconductor die (9).

Embodiment 23. The RF transmitter according to any one of embodiments 1-22, wherein at least a part of the power output stage segments (3) has similar transistor dimensions, and the digital driver (5) comprises a thermometer bit style interface to the gate-segmented power output stage (2).

Embodiment 24. The RF transmitter according to embodiment 23, wherein a further part of the power output stage segments (3) has unequal transistor dimensions, and the digital driver (5) comprises a binary bit word style interface to the gate-segmented power output stage (2).

Embodiment 25. The RF transmitter according to embodiment 23 or 24 wherein the digital driver (5) is arranged to implement dithering of one or more bits of the gate-segmented power output stage (2).

The present invention has been described above with reference to a number of exemplary embodiments as shown in the drawings. Modifications and alternative implementations of some parts or elements are possible, and are included in the scope of protection as defined in the appended claims. In summary, various embodiments of a high-power digital RF transmitter 1 (DTX) concept are provided and described above and in the attached claims, targeting e.g. low-cost, highly-integrated and energy-efficient mMIMO base stations. The present invention embodiments bridge the historical gap between low-voltage high-speed digital devices and high-voltage high-

power RF devices. The resulting combination allows for a complete replacement of the traditional transmitter line-up, which includes signal-generation, up-conversion, and analogue pre-drivers and power amplifier (PA), facilitating drastic energy savings. The aimed RF transmitter embodiments are provided by combining a digital driver 5 (data-controller with high-speed digital drivers) that control the individual gate-segments of RF power transistors (power output stage segments 3) implemented in high-voltage breakdown technology like LDMOS or GaN. The power output stage segments 3 are V_T-shifted to make them compatible with the voltage swings that can be provided by the (low-voltage) high-speed devices in the digital driver 5 in CMOS/SOI technologies. The presented configurations with gate-segmented power output stage 2 with power output stage segments 3, advantageously use thermometer weighted segments to limit differential non-linearity (DNL) errors which arise due to current redistribution effects, among others. Consequently, a relative large number of CMOS/SOI drivers (in digital driver 5) and their associated RF-power transistor segments (power output stage segments 3), with related connections are required in order to be able to meet the spectral requirements of wireless standards. For binary weighted segments (if any are still added to increase the resolution) timing and/or phase errors are reduced by equalizing their loading conditions to the digital driver 5 compared to the thermometer bits. Furthermore, further adjustments to the power output stage segments 3 were described to optimize RF transmitter 1 operation, including gate segmentation, drain and source finger sharing, as well as, improved connection schemes and decoupling for edge and flip-chip oriented high-power DTX implementations.

References

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[2] Mohsen Hashemi, Yiyu Shen, Mohammadreza Mehrpoo, Morteza S. Alavi, Leo C. N. de Vreede, "An Intrinsically Linear Wideband Polar Digital Power Amplifier", IEEE Journal of Solid-State Circuits, Year: 2017, Volume: 52, Issue: 12, Pages: 3312 – 3328.

[3] High efficiency transmitter, patent US20130058435A1 https://patents.google.com/patent/US20130058435A1/en

[4] Yiyu Shen, Mohammadreza Mehrpoo, Mohsen Hashemi, Michael Polushkin, Lei Zhou, Mustafa Acar, Rene van Leuken, Morteza S. Alavi, Leo de Vreede, Fully-Integrated Digital-Intensive Polar Doherty Transmitter, 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Year: 2017, Pages: 196 – 199.

[5] M. P. van der Heijden et al., "A 19W high-efficiency wide-band CMOS-GaN class-E Chireix RF outphasing power amplifier," in 2011 IEEE MTT-S IMS, June 2011, pp. 1–4.

[6] V. Diddi et al., "Broadband digitally-controlled power amplifier based on CMOS / GaN combination," in 2016 IEEE RFIC, May 2016, pp. 258–261.

[7] Ayad Ghannam, Niek van Haare, Julian Bravin, Elisabeth Brandl, Birgit Brandstätter, Hannes Klingler, Benedikt Auer, Philippe Meunier, Sebastiaan Kersjes, Ultra-thin QFN-Like 3D Package with 3D Integrated Passive Devices, 2019 IEEE 69th Electronic Components and Technology Conference (ECTC).

Conclusies

1. HF zender (1), omvattend:

een gate-gesegmenteerde vermogenuitgangstrap (2) omvattend een veldeffecttransistor met een veelvoud gate-vingers (32) en een veelvoud drain-vingers (31) die een gate-omgevingsgebied definiëren, waarbij de veldeffecttransistor een veelvoud vermogenuitgangstrapsegmenten (3) omvat die elk overeenstemmen met een respectief deel van het gate-omgevingsgebied en die elk een respectieve vermogenuitgangstrapsegmentingang (4) hebben; en

een digitale aansturing (5) met besturingsuitgangen (6) die verbonden zijn met overeenkomstige van de respectieve vermogenuitgangstrapsegmentingangen (4), waarbij de digitale aansturing (5) is ingericht voor het afzonderlijk schakelen van elk van de vermogenuitgangstrapsegmenten (3) tussen een aan-modus en een afsnijmodus in afhankelijkheid van één of meer ingangssignalen om een gemoduleerd HF draaggolfsignaal te verkrijgen op een uitgang (7) van de gate-gesegmenteerde vermogenuitgangstrap (2).

2. HF zender volgens conclusie 1, waarbij één of meer naast elkaar liggende gate-vingers (32) gegroepeerd zijn in een respectieve gate-segment (3a), waarbij elk vermogenuitgangstrapsegment (3) overeenstemt met één of meer gate-segmenten (3a).

3. HF zender volgens conclusie 1 of 2, waarbij de één of meer gate-vingers (32) ingericht zijn een een patroon dat bestaat uit parallelle rijen, waarbij ten minste één rij een veelvoud gate-vingers (32) omvat, waarbij de gate-vingers (32) in de ten minste ene rij uitgelijnd zijn zodat hun breedterichtingen in lijn liggen.

4. HF zender volgens conclusie 3, waarbij elke rij behoort bij een actief gebied dat continu is in de breedterichting zodat een enkel actief gebied wordt voorzien voor elke rij, waarbij het actieve gebied overeenkomt met alle gate-vingers (32) in die rij.

5. HF zender volgens één van de conclusies 1-4, waarbij naast elkaar liggende vermogenuitgangstrapsegmenten (3) een drain-vinger (31) delen.

6. HF zender volgens één van de conclusies 1-5, waarbij alle drain-vingers (31) zich utstrekken vanaf een drain-balk (33).

7. HF zender volgens conclusie 6, waarbij een bedrijfsfrequentie van de HF zender (1) loopt van 1 GHz tot 50 GHz, en waarvoor een absoluut faseverschil voor signalen die zich voortplanten via naast elkaar liggende vermogenuitgangstrapsegmenten (3) vanaf de vermogenuitgangstrapsegmentingang (4) naar de drain-balk (33) minder is dan 5 graden bij de bedrijfsfrequentie voor elk paar van naast elkaar liggende vermogenuitgangstrapsegmenten (3).

8. HF zender volgens één van de conclusie 1-7, waarbij de aanmodus van een vermogenuitgangstrapsegment (3) een verzadigingsstatus van het vermogenuitgangstrapsegment (3) omvat.

9. HF zender volgens één van de conclusies 1-8, waarbij de digitale aansturing (5) en gate-gesegmenteerde vermogenuitgangstrap (2) zijn geïmplementeerd in verschillende halfgeleidertechnologieën.

10. HF zender volgens conclusie 9, waarbij de digitale aansturing (5) een in CMOS of als SOI geïmplementeerde digitale aansturing omvat.

11. HF zender volgens conclusie 9 of 10, waarbij de gate-gesegmenteerde vermogenuitgangstrap (2) transistoren omvat van een lateraal gediffundeerd metaal-oxide-halfgeleider (LDMOS) transistor type, en/of een op GaN gebaseerd veld-effecttransistor type.

12. HF zender volgens conclusie 11, waarbij de transistoren van de gate-gesegmenteerde vermogenuitgangstrap (2) zijn ingericht om een drempelspanning te hebben die de digitale aansturing (5) in staat stelt om afzonderlijk elk van de vermogenuitgangstrapsegmenten (3) te schakelen tussen een aanmodus en een afsnijmodus in afhankelijkheid van de besturingsuitgangen (6).

13. HF zender volgens één van de conclusies 1-12, verder omvattend een veelvoud nivoverschuivers die verbonden zijn met de besturingsuitgangen (6) van de digitale aansturing (5) en de vermogenuitgangstrapsegmentingangen (4) van de gate-gesegmenteerde vermogenuitgangstrap (2).

14. HF zender volgens één van de conclusies 1-13, waarbij de digitale aansturing (5) is voorzien in een eerste halfgeleiderchip (8), en de gate-gesegmenteerde vermogenuitgangstrap (2)

is voorzien in een tweede halfgeleiderchip (9), waarbij de eerste halfgeleiderchip (8) verschillend is van de tweede halfgeleiderchip (9),

waarbij de digitale aansturing (5) een veelvoud uitgangsaansluitingen (8a) omvat behorend bij de besturingsuitgangen (6),

waarbij de gate-gesegmenteerde vermogenuitgangstrap (2) een veelvoud ingangsaansluitingen (9a) omvat behorend bij elke vermogenuitgangstrapsegmentingang (4),

verder omvattend verbindingen (10) tussen respectieve uitgangsaansluitingen (8a) op de eerste halfgeleiderchip (8) en bijbehorende ingangsaansluitingen (9a) op de tweede halfgeleiderchip (9).

15. HF zender volgens conclusie 14, waarbij de uitgangsaansluitingen (8a) op de eerste halfgeleiderchip (8) en de ingangsaansluitingen (9a) op de tweede halfgeleiderchip (9) voorzien zijn in een randgedeelte van de eerste halfgeleiderchip (8), respectievelijk tweede halfgeleiderchip (9).

16. HF zender volgens conclusie 14 of 15, waarbij de verbindingen (10) verbindingsdraden omvatten.

17. HF zender volgens conclusie 14 of 15, waarbij de verbindingen (10) tussenverbindingsfilm-verbindingen omvatten.

18. HF zender volgens conclusie 14 of 15, waarbij de verbindingen (10) flip-chip type verbindingen omvatten.

19. HF zender volgens één van de conclusies 14-18, waarbij de verbindingen (10) verder een veelvoud aardeverbindingen omvatten tussen de eerste halfgeleiderchip (8) en de tweede halfgeleiderchip (9).

20. HF zender volgens één van de conclusies 14-19, waarbij de uitgangsaansluitingen (8a) en ingangsaansluitingen (9a) direct verbonden zijn met de besturingsuitgangen (6), respectievelijk vermogenuitgangstrapsegmentingangen (4).

21. HF zender volgens één van de conclusies 14-20, waarbij een steekafstand (p1) tussen de uitgangsaansluitingen (8a) op de eerste halfgeleiderchip (8) in hoofdzaak gelijk is aan een steekafstand (p2) tussen de ingangsaansluitingen (9a) op de tweede halfgeleiderchip (9).

22. HF zender volgens één van de conclusies 14-21, verder omvattend externe aansluitingen (21) die voorzien zijn op de tweede halfgeleiderchip (9).

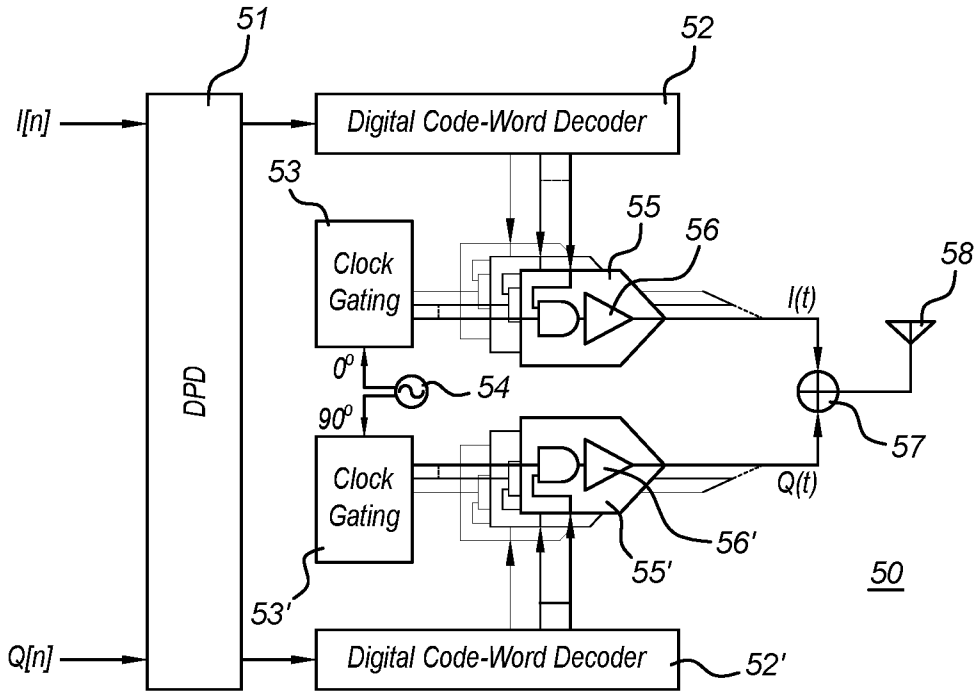
23. HF zender volgens één van de conclusies 1-22, waarbij het minste een deel van de vermogenuitgangstrapsegmenten (3) gelijksoortige transistordimensies heeft, en de digitale aansturing (5) een thermometer-bitstijl interface heeft met de gate-gesegmenteerde vermogenuitgangstrap (2).

24. HF zender volgens conclusie 23, waarbij een verder deel van de vermogenuitgangstrapsegmenten (3) ongelijke transistordimensies heeft, en de digitale aansturing (5) een binair-bitwoordstijl heeft met de gate-gesegmenteerde vermogenuitgangstrap (2).

25. HF zender volgens conclusie 23 of 24, waarbij de digitale aansturing (5) is ingericht om dithering van één of meer bits van de gate-gesegmenteerde vermogenuitgangstrap (2) uit te voeren.

****

Fig. 1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Digital Code-Word Decoder
53
55
56
58
Clock Gating
I(t)
0°
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90°
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DPD
Clock Gating
Q(t)
56'
55'
50
53'
Q[n]
Digital Code-Word Decoder
52'

Fig. 2

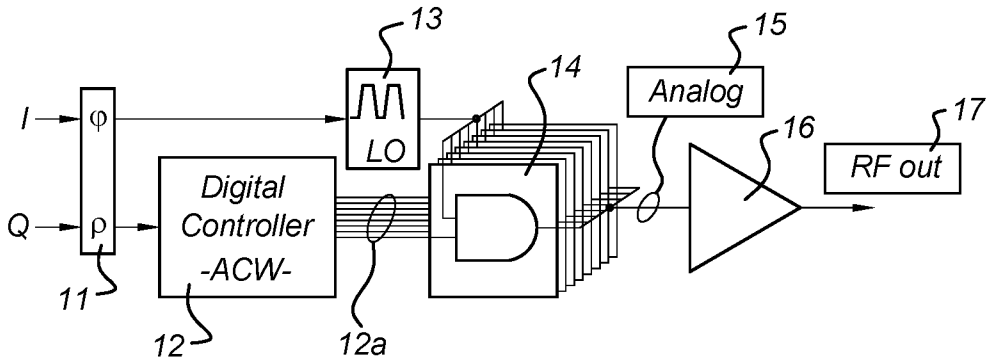
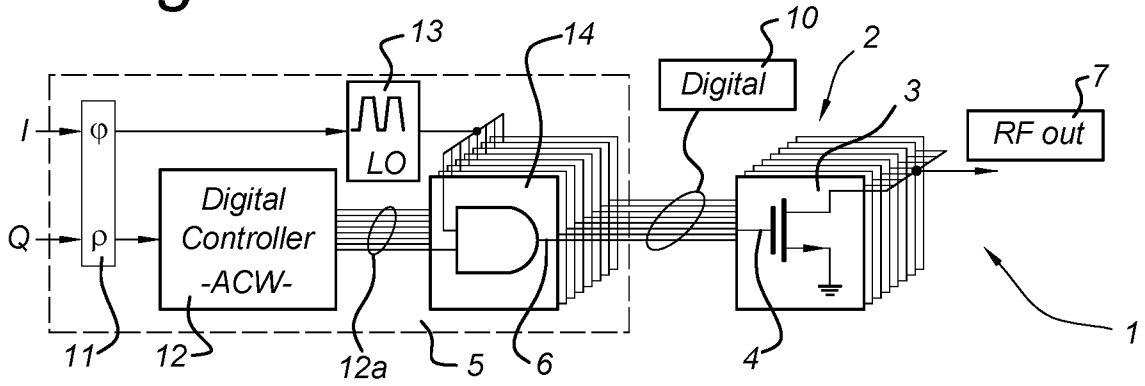

13
15
14
Analog
17
16
I
φ
LO
RF out
Digital Controller -ACW-
Q
ρ
11
12
12a

Fig. 3



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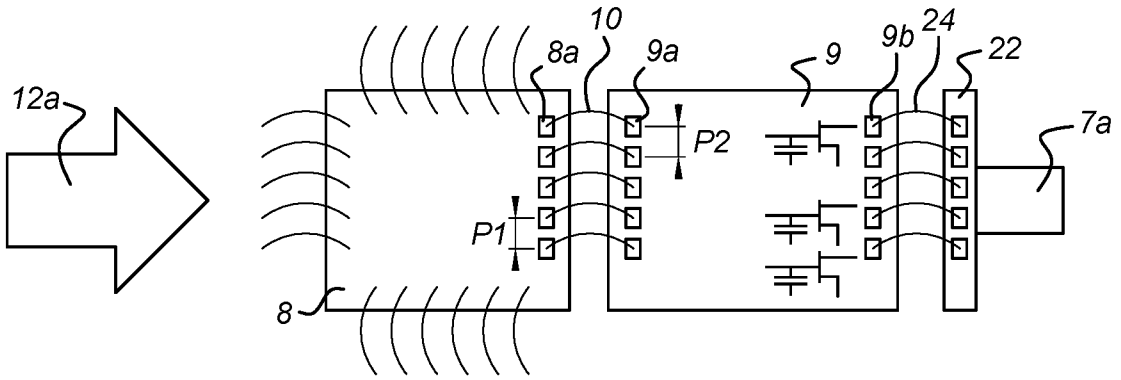

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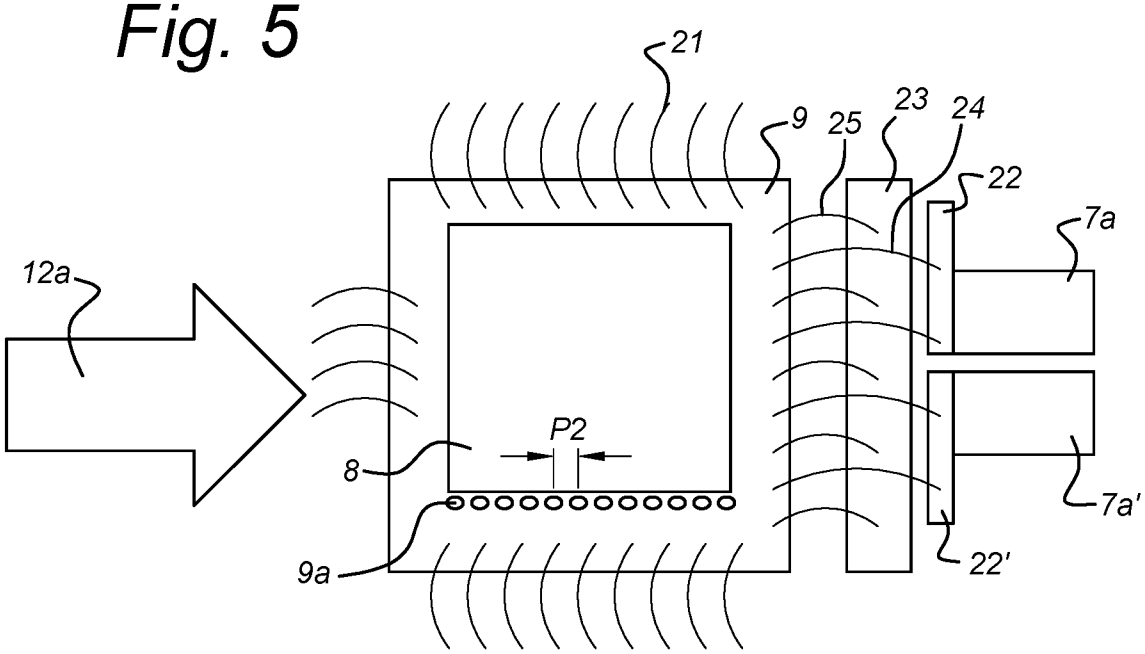


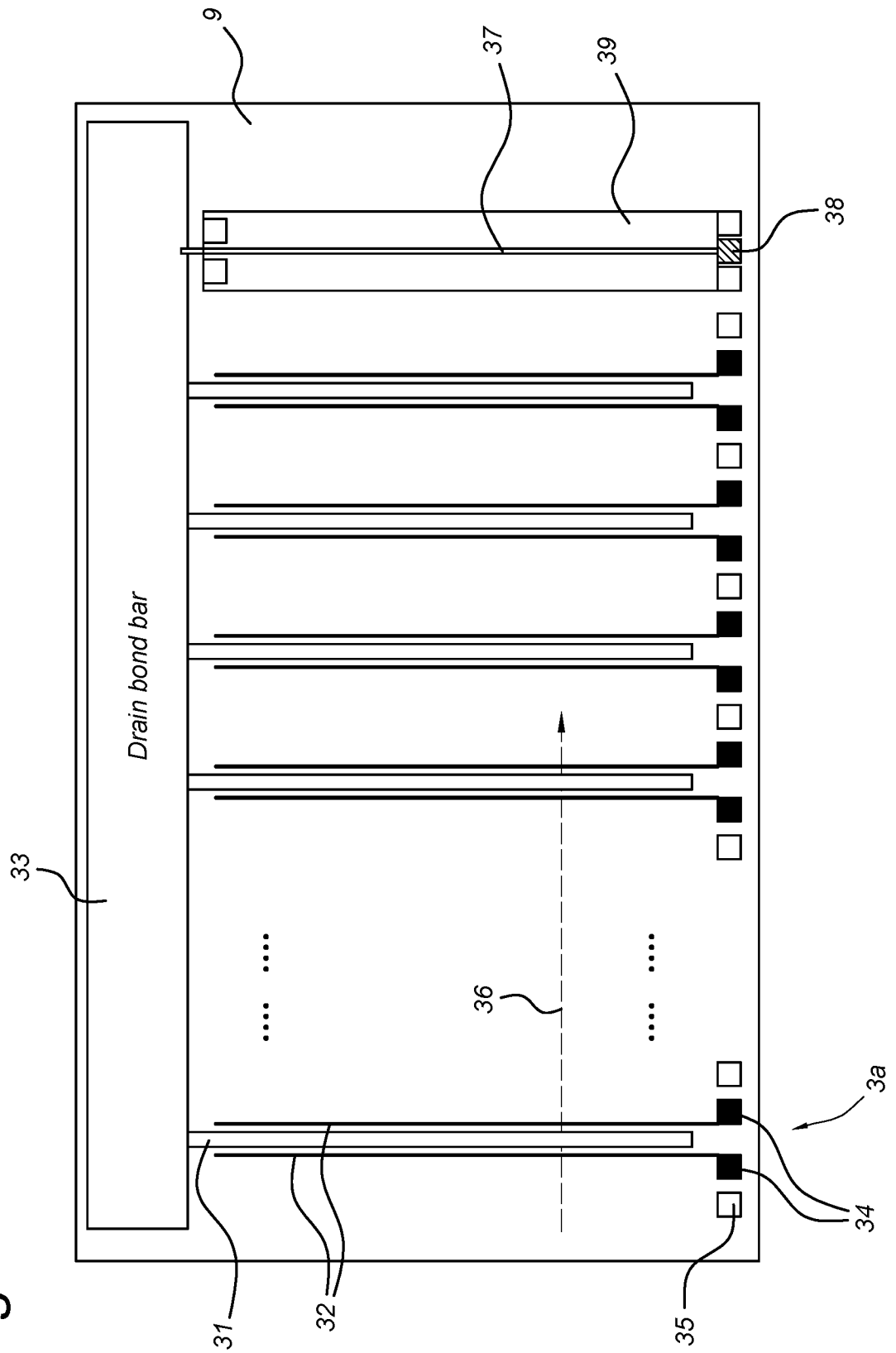


Fig. 6

Fig. 7A

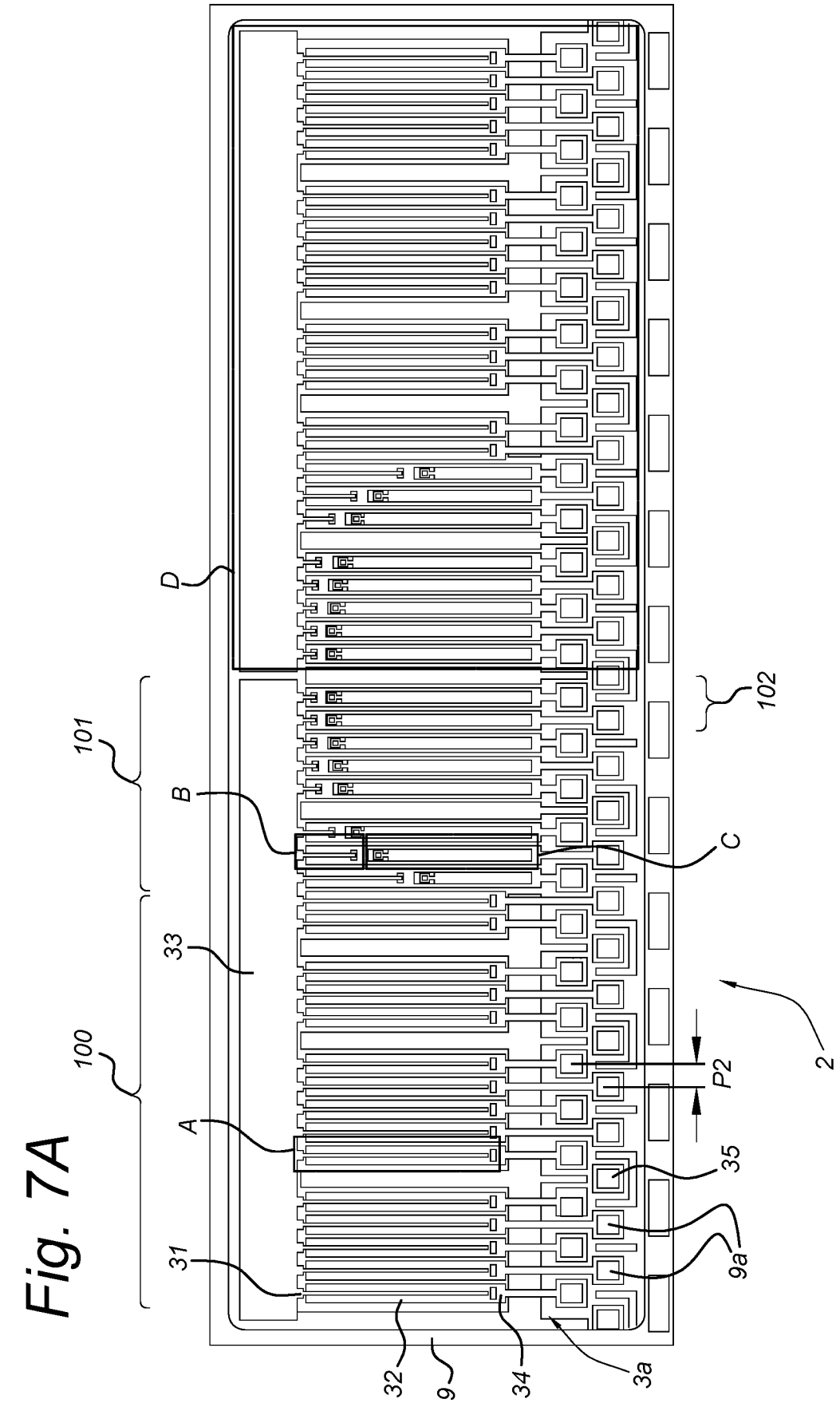
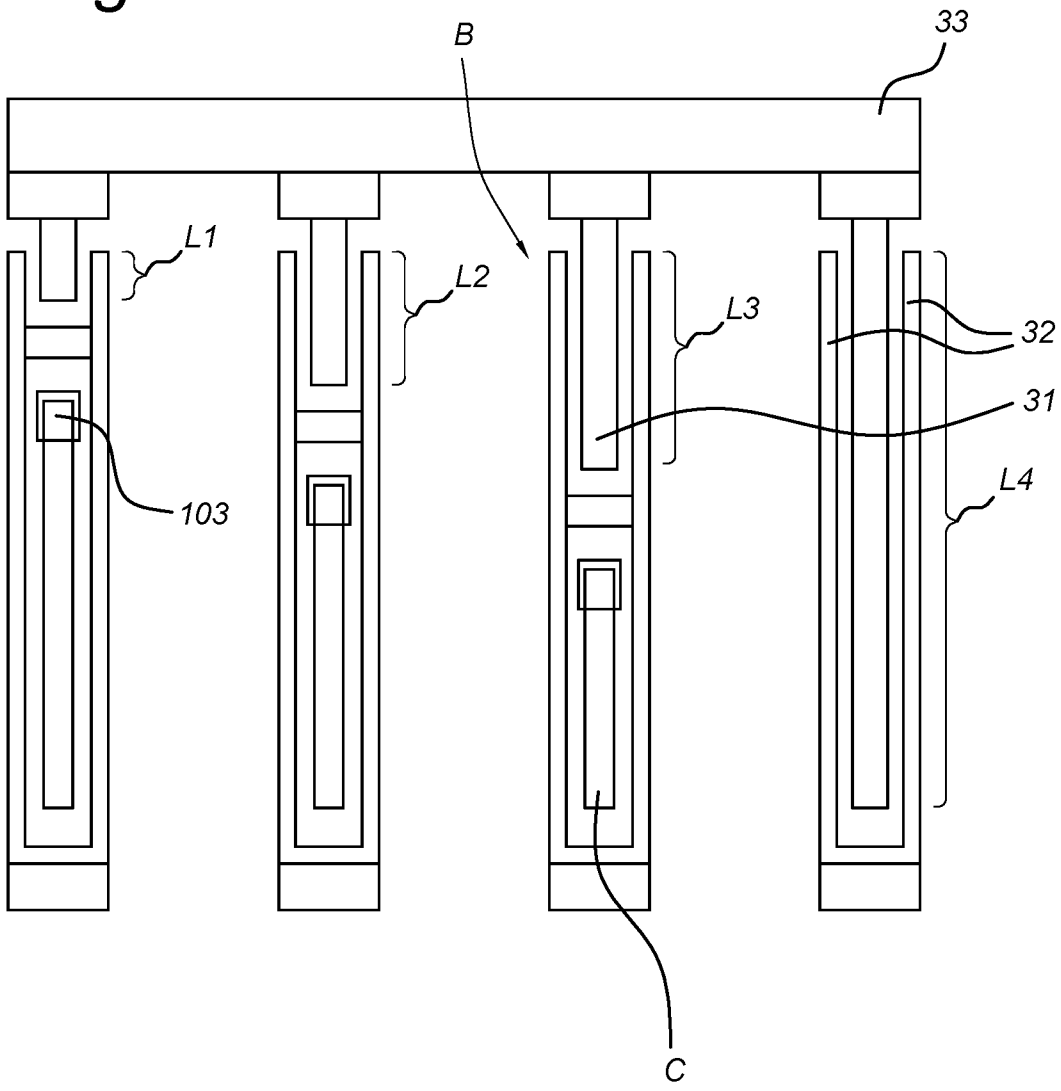
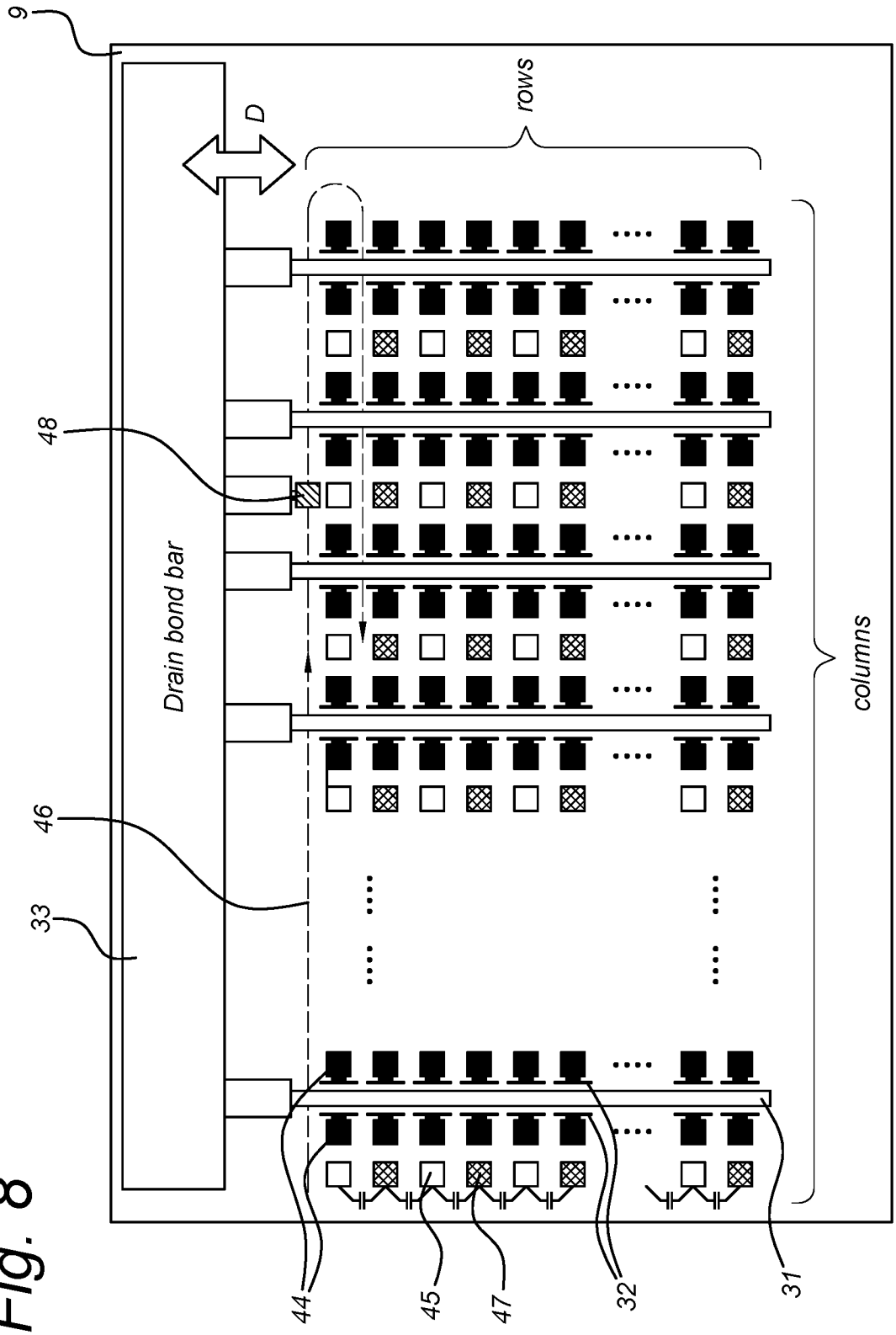


Fig. 7B





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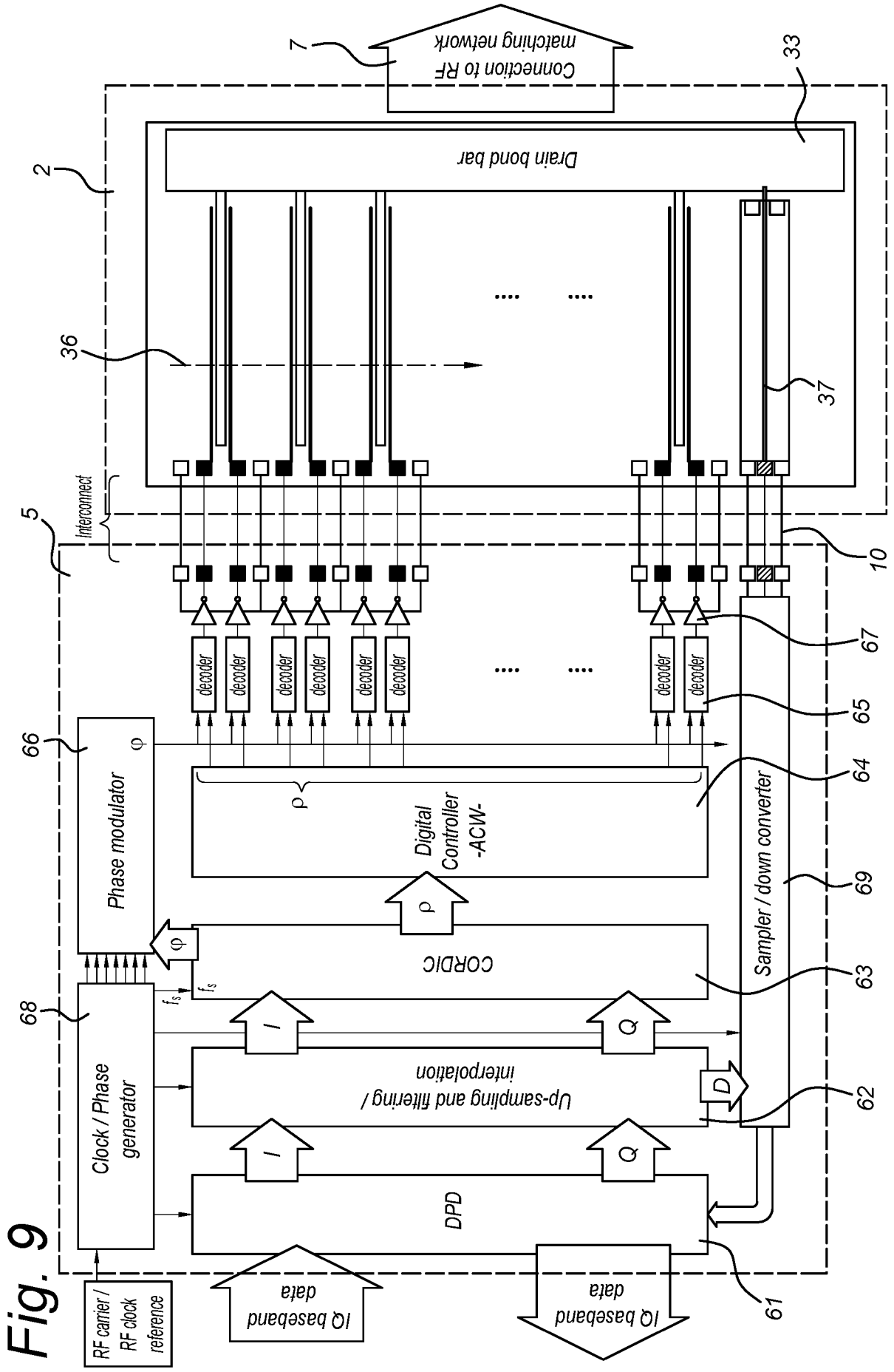
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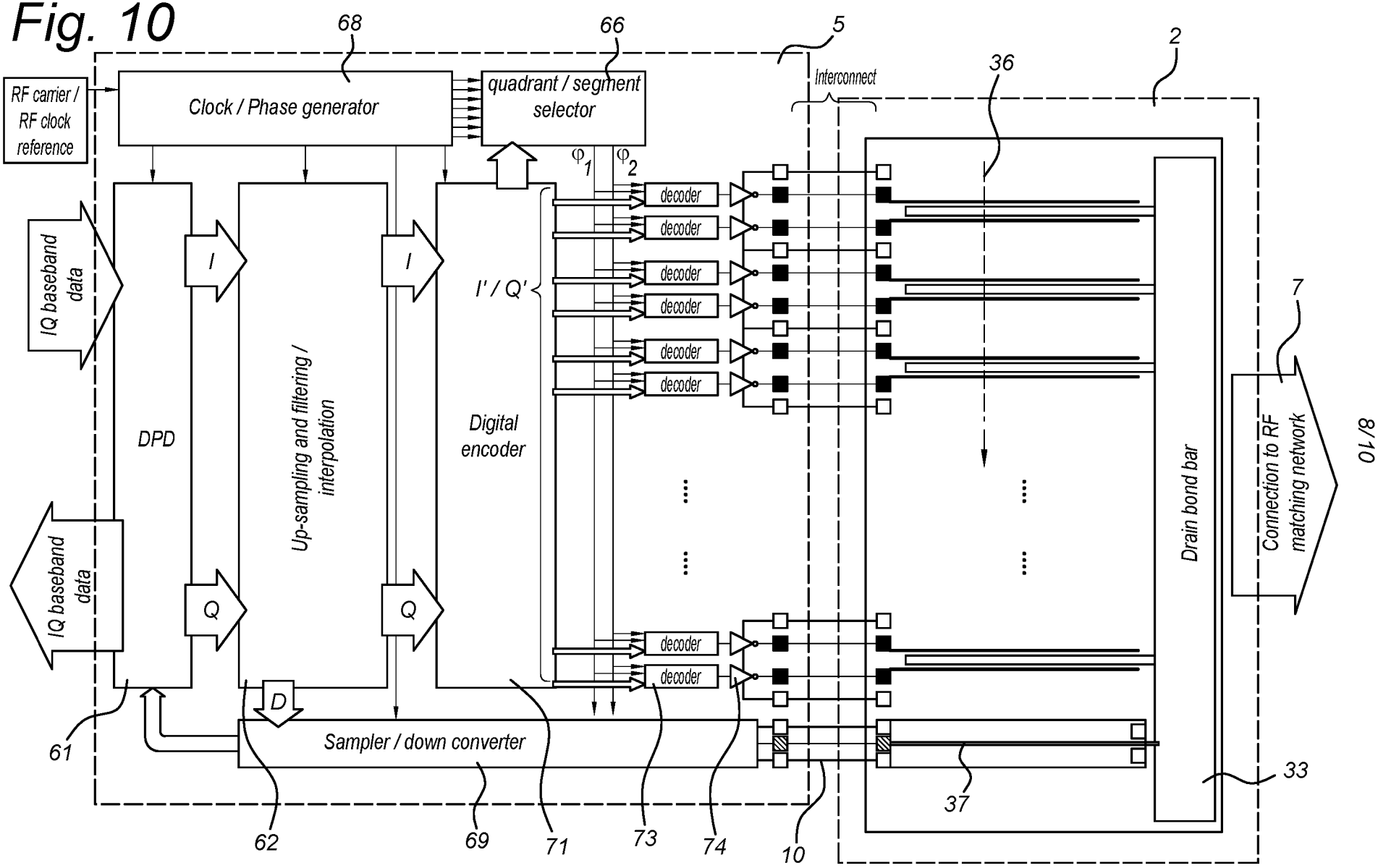
33
Drain bond bar
2
36
37
Interconnect
5
10
decoder
67
65
66
Phase modulator
φ
ρ
Digital Controller -ACW-
64
ρ
φ
CORDIC
63
Sampler / down converter
69
68
Clock / Phase generator
f_s
I
Q
D
Up-sampling and filtering / interpolation
62
DPD
61
IQ baseband data
IQ baseband data
RF carrier / RF clock reference

Fig. 9

Fig. 10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5
2
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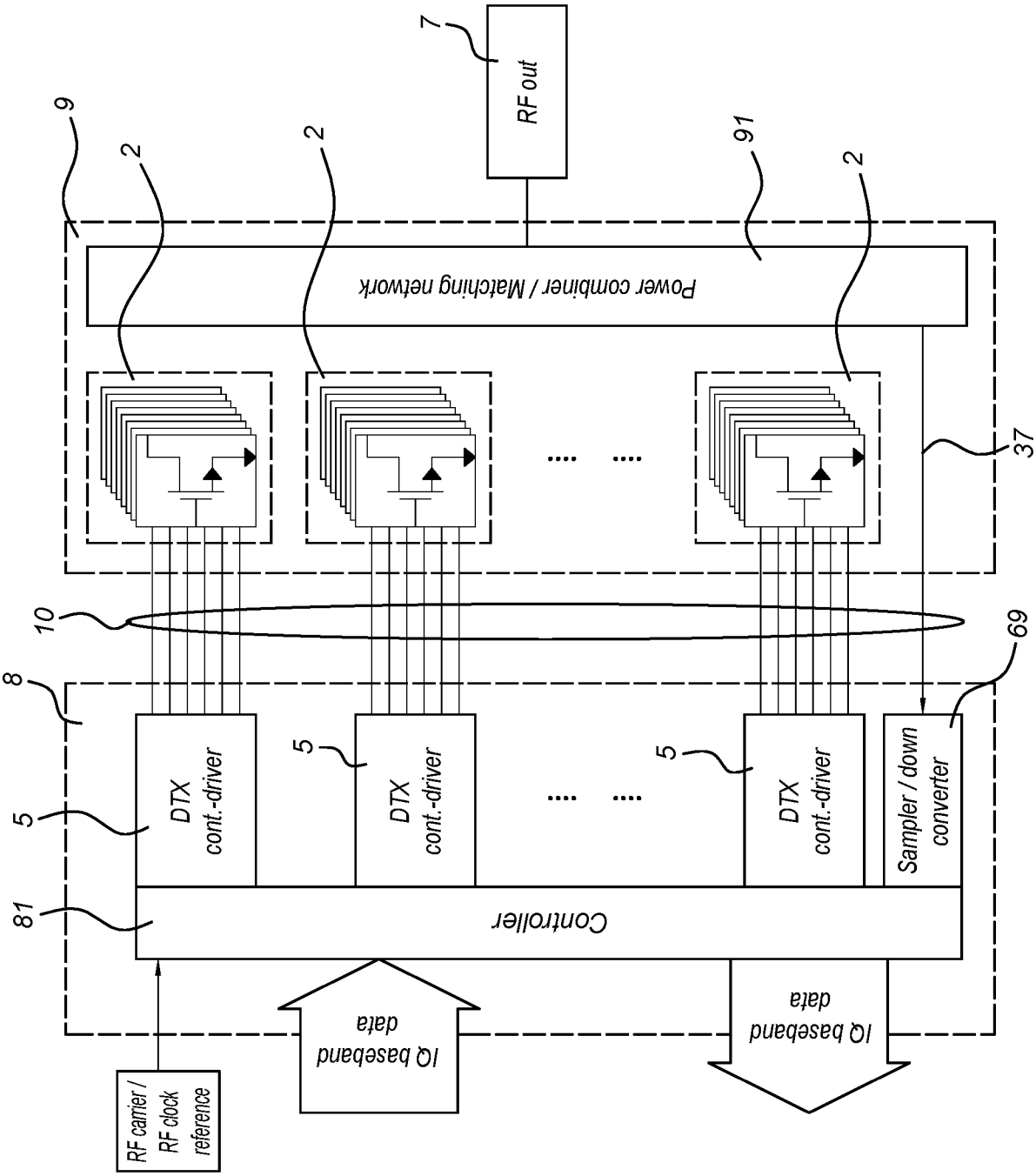
Interconnect
RF carrier / RF clock reference
Clock / Phase generator
quadrant / segment selector
φ1
φ2
IQ baseband data
I
I
I' / Q'
decoder
DPD
Up-sampling and filtering / interpolation
Digital encoder
Drain bond bar
7
Connection to RF matching network
IQ baseband data
Q
Q
D
Sampler / down converter
61
62
69
71
73
74
10
37
33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DTX cont.-driver
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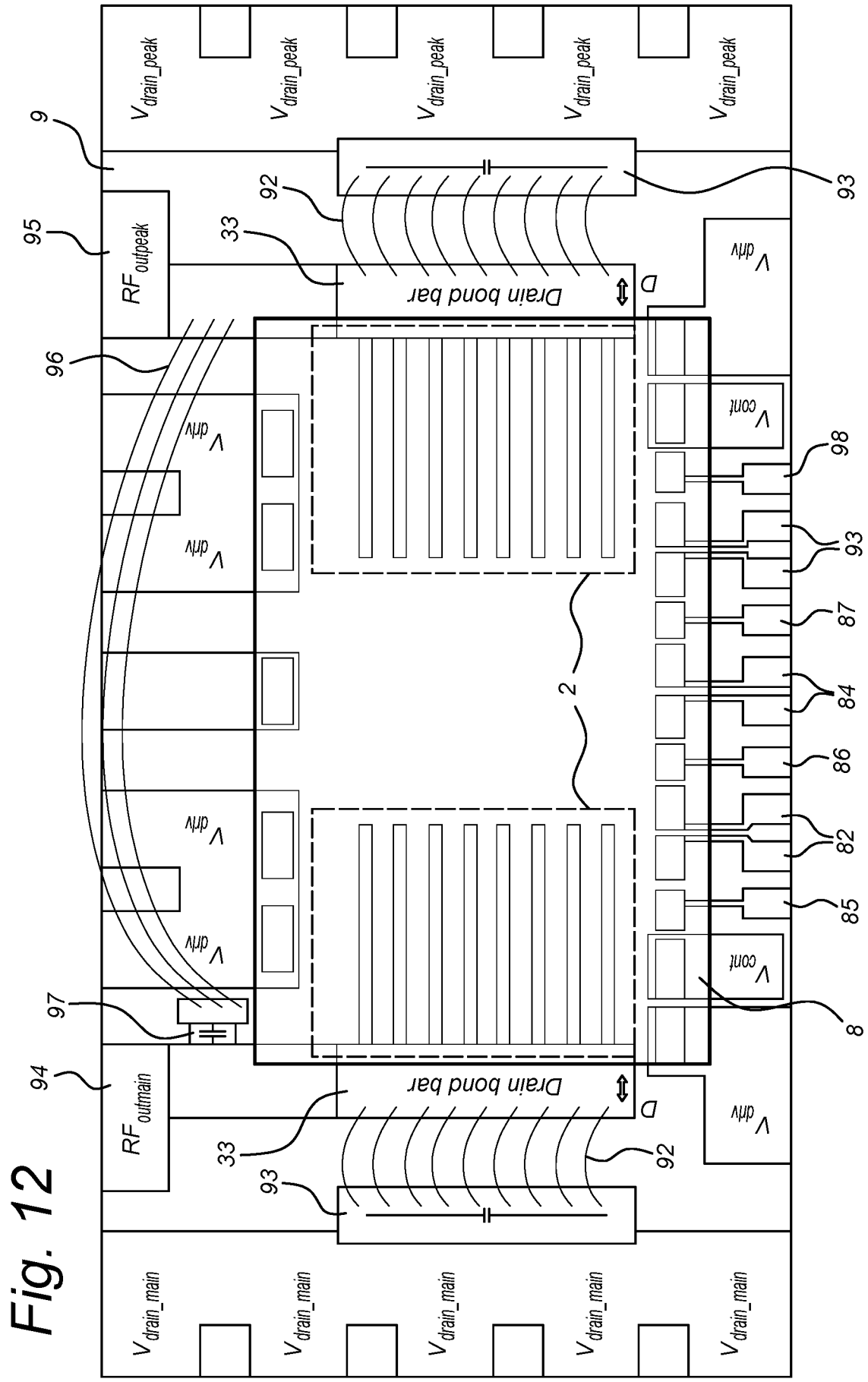
DTX cont.-driver
5
DTX cont.-driver
Sampler / down converter
81
Controller
IQ baseband data
IQ baseband data
RF carrier / RF clock reference

Fig. 11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V_{drain_peak}
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9
92
93
95
$RF_{outpeak}$
33
Drain bond bar
D
V_{drv}
96
V_{cont}
98
V_{drv}
93
V_{drv}
87
2
84
86
V_{drv}
82
V_{drv}
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$RF_{outmain}$
Drain bond bar
D
V_{drv}
33
92
93
V_{drain_main}
V_{drain_main}
V_{drain_main}
V_{drain_main}
V_{drain_main}

Fig. 12

SAMENWERKINGSVERDRAG (PCT)

RAPPORT BETREFFENDE NIEUWHEIDSONDERZOEK VAN INTERNATIONAAL TYPE

IDENTIFICATIE VAN DE NATIONALE AANVRAGE	KENMERK VAN DE AANVRAGER OF VAN DE GEMACHTIGDE
	P6090217NL
Nederlands aanvraag nr. **2024903**	Indieningsdatum **14-02-2020**
	Ingeroepen voorrangsdatum
Aanvrager (Naam) **TECHNISCHE UNIVERSITEIT DELFT**	
Datum van het verzoek voor een onderzoek van internationaal type **11-04-2020**	Door de Instantie voor Internationaal Onderzoek aan het verzoek voor een onderzoek van internationaal type toegekend nr. **SN75968**

I. CLASSIFICATIE VAN HET ONDERWERP (bij toepassing van verschillende classificaties, alle classificatiesymbolen opgeven)

Volgens de internationale classificatie (IPC)

Zie onderzoeksrapport

II. ONDERZOCHTE GEBIEDEN VAN DE TECHNIEK

Onderzochte minimumdocumentatie

Classificatiesysteem	Classificatiesymbolen
IPC	**Zie onderzoeksrapport**

Onderzochte andere documentatie dan de minimum documentatie, voor zover dergelijke documenten in de onderzochte gebieden zijn opgenomen

III. ☐ **GEEN ONDERZOEK MOGELIJK VOOR BEPAALDE CONCLUSIES** (opmerkingen op aanvullingsblad)

IV. ☐ **GEBREK AAN EENHEID VAN UITVINDING** (opmerkingen op aanvullingsblad)

ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2024903

A. CLASSIFICATIE VAN HET ONDERWERP
INV. H03F3/195 H03F3/213 H03F3/24
ADD.

Volgens de Internationale Classificatie van octrooien (IPC) of zowel volgens de nationale classificatie als volgens de IPC.

B. ONDERZOCHTE GEBIEDEN VAN DE TECHNIEK

Onderzochte miminum documentatie (classificatie gevolgd door classificatiesymbolen)
H03F

Onderzochte andere documentatie dan de mimimum documentatie, voor dergelijke documenten, voor zover dergelijke documenten in de onderzochte gebieden zijn opgenomen

Tijdens het onderzoek geraadpleegde elektronische gegevensbestanden (naam van de gegevensbestanden en, waar uitvoerbaar, gebruikte trefwoorden)
EPO-Internal, WPI Data

C. VAN BELANG GEACHTE DOCUMENTEN

Categorie °	Geciteerde documenten, eventueel met aanduiding van speciaal van belang zijnde passages	Van belang voor conclusie nr.
A	WO 2018/132006 A1 (UNIV DELFT TECH [NL]; TECH STW [NL]) 19 juli 2018 (2018-07-19) * alinea [0055] - alinea [0057]; figuur 9 *	1-25

☐ Verdere documenten worden vermeld in het vervolg van vak C.

☒ Leden van dezelfde octrooifamilie zijn vermeld in een bijlage

° Speciale categorieën van aangehaalde documenten

"A" niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft

"D" in de octrooiaanvrage vermeld

"E" eerdere octrooi(aanvrage), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven

"L" om andere redenen vermelde literatuur

"O" niet-schriftelijke stand van de techniek

"P" tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur

"T" na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvrage, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding

"X" de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur

"Y" de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht

"&" lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie

Datum waarop het onderzoek naar de stand van de techniek van internationaal type werd voltooid	Verzenddatum van het rapport van het onderzoek naar de stand van de techniek van internationaal type
29 september 2020	

Naam en adres van de instantie	De bevoegde ambtenaar
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wienema, David

Formulier PCT/ISA/201 (tweede blad) (Januari 2004)

ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE

Informatie over leden van dezelfde octrooifamilie

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2024903

In het rapport genoemd octrooigeschrift	Datum van publicatie	Overeenkomend(e) geschrift(en)	Datum van publicatie
WO 2018132006 A1	19-07-2018	CN 110679081 A	10-01-2020
		EP 3568912 A1	20-11-2019
		US 2019386690 A1	19-12-2019
		US 2020244293 A1	30-07-2020
		WO 2018132006 A1	19-07-2018

WRITTEN OPINION

File No.	Filing date *(day/month/year)*	Priority date *(day/month/year)*	Application No.
SN75968	14.02.2020		NL2024903

International Patent Classification (IPC)
INV. H03F3/195 H03F3/213 H03F3/24

Applicant
TECHNISCHE UNIVERSITEIT DELFT

This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the application
- ☒ Box No. VIII Certain observations on the application

	Examiner
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Application number

WRITTEN OPINION

NL2024903

Box No. I Basis of this opinion

1. This opinion has been established on the basis of the latest set of claims filed before the start of the search.

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ on paper

   ☐ in electronic form

   c. time of filing/furnishing:

   ☐ contained in the application as filed.

   ☐ filed together with the application in electronic form.

   ☐ furnished subsequently for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty	Yes:	Claims	1-25
	No:	Claims	
Inventive step	Yes:	Claims	1-25
	No:	Claims	
Industrial applicability	Yes:	Claims	1-25
	No:	Claims	

2. Citations and explanations

see separate sheet

WRITTEN OPINION

Box No. VII Certain defects in the application

see separate sheet

Box No. VIII Certain observations on the application

see separate sheet

1 **Re Item V**

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following document:

D1 WO 2018/132006 A1 (UNIV DELFT TECH [NL]; TECH STW [NL]) 19 juli 2018 (2018-07-19)

1.1 **Novelty & Inventive step**

It appears that the present application meets the criteria of patentability, because the subject-matter of claims 1 to 25 is novel and involves an inventive step with respect to **D1** which appears to represent the closest prior art. Reasons are as follows:

1.1.1 **Claim 1**:

D1 discloses:

HF zender (see Fig. 9), omvattend:

een ~~**gate-**~~gesegmenteerde vermogenuitgangstrap (see Fig. 9, Seg. 1, Seg. 2, ..., Seg. N) omvattend een veldeffecttransistor met een veelvoud gate-vingers en een veelvoud drain-vingers die een gate-omgevingsgebied definiëren (see Fig. 9, implicit), ~~**waarbij de veldeffecttransistor een veelvoud vermogenuitgangstrapsegmenten omvat die elk overeenstemmen met een respectief deel van het gate-omgevingsgebied en die elk een respectieve vermogenuitgangstrapsegmentingang hebben; en**~~

een digitale aansturing (see Fig. 9, the plurality of NAND gates) met besturingsuitgangen (see Fig. 9, the outputs of the plurality of NAND gates) ~~**die verbonden zijn met overeenkomstige van de respectieve vermogenuitgangstrapsegmentingangen, waarbij de digitale aansturing is ingericht voor het afzonderlijk schakelen van elk van de vermogenuitgangstrapsegmenten tussen een aan-modus en een afsnijmodus in afhankelijkheid van één of meer ingangssignalen om een gemoduleerd HF draaggolfsignaal te verkrijgen op een uitgang van de gate-gesegmenteerde vermogenuitgangstrap**~~.

The subject-matter of claim 1 differs from the disclosure in **D1** in the features that have been marked in bold and struck through.

The technical effect achieved is that due to the reduction in parasitic components a better efficiency versus output power trade-off can be struck.

The objective technical problem to be solved could therefore be regarded as how to adapt the circuit of **D1**, Fig. 9 in order to be able to increase the output power while maintaining a good efficiency.

Starting **D1** while taking into account common general knowledge or the teachings of documents cited by the Applicant in the description**,** respectively, the man skilled in the art would not have any hint or suggestion that would prompt him to implement all of the above-mentioned distinguishing technical features in order to solve the problem.

Segmentation of the power output stage, i.e. using a gate-segmented power output stage transistor is applied, rather than using separate transistors as is done in the cited prior art documents in which the circuits are entirely implemented in a single CMOS or SOI technology.

The invention of the application under review will result in much lower parasitics and consequently a much better RF performance at higher power levels for the RF transmitter. The original gate periphery of a power transistor is divided in smaller pieces, yielding isolated power output stage segments, each with its individual connection to the digital driver.

The subject-matter of independent apparatus claim 1 therefore comprises an inventive step with respect to **D1**, which is considered to represent the closest prior art, alone or in combination with the other cited prior art documents and common general knowledge.

2 **Re Item VII**

Certain defects in the international application

2.1 Contrary to the requirements, the relevant background art disclosed in **D1** cited in the search report is not mentioned in the description, nor is this document identified therein.

3 **Re Item VIII**

The subject-matter of claim 1 is not clear for the following reasons.

3.1 **Claim 1**

It is clear from the description on page 6, line 27 to 37, and from Figs. 6 to 10 and corresponding passages in the description that in order to reduce the parasitic components, the drain and source fingers should be shared, and the drain fingers should be parallel to each other and connected to a common drain bar. These features are considered as essential to the definition of the invention.

Since independent claim 1 does not contain these features it does not meet the requirement of clarity that any independent claim must contain all the technical features essential to the definition of the invention.