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(54) Title: PACKAGED SEMICONDUCTOR DEVICE WITH A PARTICLE ROUGHENED SURFACE

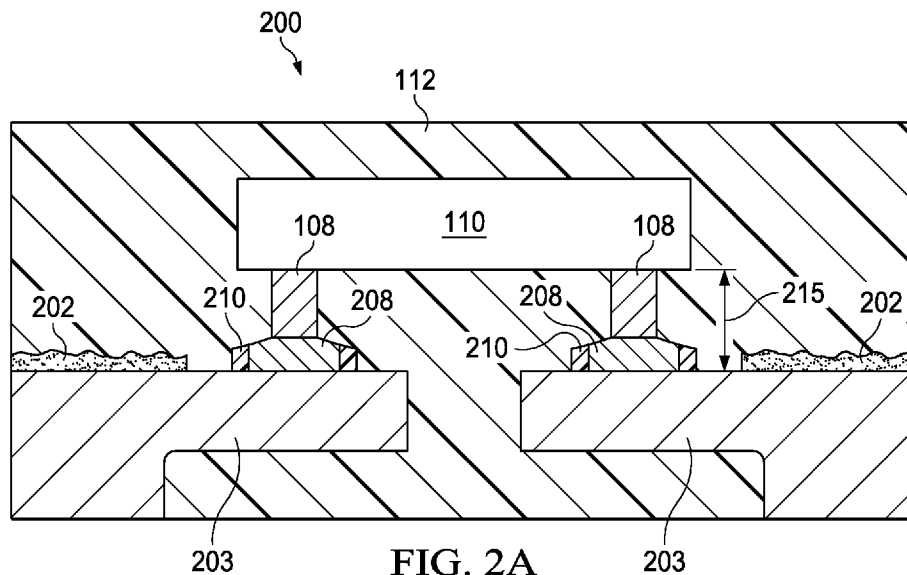


FIG. 2A

(57) Abstract: A packaged semiconductor device (200) with a particle roughened surface (202) on a portion of the lead frame (203) that improves adhesion between the molding compound (112) and the lead frame (203). A packaged semiconductor device (200) with a particle roughened surface (202) on a portion of the lead frame (203) that improves adhesion between the molding compound (112) and the lead frame (203) and with a reflow wall (210) that surrounds a portion of the solder joint (208) that couples the semiconductor device (110) to the lead frame (203). A packaged semiconductor device (200) with a reflow wall (210) that surrounds a portion of a solder joint (208) that couples a semiconductor device (110) to a lead frame (203).



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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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PACKAGED SEMICONDUCTOR DEVICE WITH A PARTICLE ROUGHENED SURFACE

[0001] This disclosure relates to the field of packaged semiconductor devices. More particularly, this disclosure relates to packaged semiconductor devices with improved adhesion between the molding compound and lead frame.

SUMMARY

[0002] The following presents a simplified summary in order to provide a basic understanding of one or more aspects of the disclosure. This summary is not an extensive overview of the disclosure, and is neither intended to identify key or critical elements of the disclosure, nor to delineate the scope thereof. Rather, the primary purpose of the summary is to present some concepts of the disclosure in a simplified form as a prelude to a more detailed description that is presented later.

[0003] A packaged semiconductor device with a particle roughened surface on a portion of the lead frame with molding compound. A packaged semiconductor device with a particle roughened surface on a portion of the lead frame with molding compound, with a reflow wall that surrounds a portion of a solder joint that couples the semiconductor device to the lead frame. The particle roughened surface may aid in adhesion between the molding compound and the lead frame.

[0004] A packaged semiconductor device with a lead frame and a semiconductor device. A solder joint is coupled between the lead frame and a terminal on the semiconductor device. A reflow wall is on a portion of the lead frame and in contact with the solder joint. Molding compound covers portions of the semiconductor device, the lead frame, the solder joint, and the reflow wall.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1A is a cross-section of a packaged semiconductor device.

[0006] FIG. 1B is a top view of the lead frame in the packaged semiconductor device in FIG. 1A.

[0007] FIGS. 2A and 2B are cross-sections of packaged semiconductor devices with a lead frame, having a reflow wall and a particle roughened surface area.

[0008] FIGS. 3A and 3B are views of reflow walls.

[0009] FIG. 4 is a top view of a lead frame having a reflow wall and a particle roughened surface.

[0010] FIGS. 5A and 5B are cross section views of a lead frame and a semiconductor device illustrating the attachment of the semiconductor device to a lead frame.

[0011] FIG. 6 is a cross section view of a lead frame with a particle roughened surface.

[0012] FIGS. 7A and 7B are cross section views of lead frames with printed circuit board solder pads on the bottom side of the lead frame.

[0013] FIGS. 8A, 8B, and 8C are cross section views of a lead frame with reflow walls formed in accordance with embodiments.

[0014] FIGS. 9A, 9B, and 9C, are cross section views of packaged semiconductor devices with particle roughened surfaces, reflow walls, and printed circuit board solder pads on the bottom side formed.

[0015] FIG. 10 is a cross section view illustrating a packaged semiconductor device with particle roughened surfaces and a solder pad on the top side of the lead frame and with a printed circuit board solder pad on the bottom side of the packaged semiconductor device.

[0016] FIGS. 11A through 11C are cross section views illustrating the major manufacturing steps in forming particle roughened surfaces and reflow walls using ink jet printing.

[0017] FIGS. 12A and 12B are cross section views illustrating the major manufacturing steps in forming printed circuit board solder pads on the bottom side of the lead frame using ink jet printing.

[0018] FIGS. 13A through 13C are cross section views illustrating the major manufacturing steps in forming particle roughened surfaces and reflow walls using screen printing.

[0019] FIGS. 14A and 14B are cross sections illustrating the major manufacturing steps in forming printed circuit board solder pads on the bottom side of a lead frame using screen printing.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] Embodiments of the disclosure are described with reference to the attached figures. The figures are not drawn to scale and they are provided merely to illustrate the disclosure. Several aspects of the embodiments are described below with reference to example applications for illustration. It should be understood that numerous specific details, relationships, and methods

are set forth to provide an understanding of the disclosure. One skilled in the relevant art, however, will readily recognize that the disclosure can be practiced without one or more of the specific details or with other methods. In other instances, well-known structures or operations are not shown in detail to avoid obscuring the disclosure. The embodiments are not limited by the illustrated ordering of acts or events, as some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a method.

[0021] A packaged semiconductor device 100 is illustrated in the cross section in FIG. 1A. A semiconductor device 110 may be any semiconductor device, for example an integrated circuit, transistor, or diode. The semiconductor device 110 is attached to a lead frame 105 and covered with molding compound 112 to form the packaged semiconductor device 100. The semiconductor device package may be any package form, for example a dual in line package (DIP), a quad flat no lead (QFN) package or a flip chip small outline transistor (FCSOT) package or a radial package. A top view of the lead frame 105 in the packaged semiconductor device 100 is shown in FIG. 1B. The lead frame 105 is comprised of a number of leads 102 on which solder pads 104 are formed. The semiconductor device 110 is bonded to the lead frame 105 with solder joints 107 formed between metal posts 108 connected to input/output pads on the semiconductor device 110 and the solder pads 104. The number of leads 102 with solder pads 104 in a lead frame 105 may vary depending upon the number of solder joints 107 needed to mount the semiconductor device 110.

[0022] Another embodiment directly connects the solder pads 104 of the lead frame to input/output pads on the semiconductor device.

[0023] The cross section of the lead frame 105 in FIG. 1A is along the dashed line over the top view in FIG. 1B.

[0024] In the cross section of the packaged semiconductor device 100 in FIG. 1A, solder pads 104 are made of a material that solder easily wets. Solder joints 107 are formed between the solder pads 104 and metallic posts 108 that are connected to input/output (I/O) terminals of the semiconductor device 109. The metallic posts 108 typically are made of a conductive material such as copper, gold, or solder. Portions of this assembly is covered with molding compound 112 to form the packaged semiconductor device 100. Packaged semiconductor device 110 reliability failures may occur when the molding compound 112 delaminates from the lead frame 105 due to

poor adhesion. To improve adhesion portions of the surface of the lead frame 105 may be roughened using wet chemical etching, for example.

[0025] The semiconductor device 110 is mounted on the first side (top side) of lead frame 105 as described above. Printed circuit board (PCB) solder pads 106 may be formed on the second side (bottom side) of the lead frame 105 to facilitate soldering the packaged semiconductor device 100 to leads on an underlying PCB.

[0026] The solder 104 pads on the topside of the lead frame 105 and the PCB solder pads 106 on the bottom side of the lead frame 105 are typically formed at additional cost by electroplating solderable metals such as palladium coated nickel using a masking process during the manufacture of the lead frame 105.

[0027] Cross sections of a packaged semiconductor device 200 with a semiconductor device 110 attached to a lead frame 203 with solder joints, 208, are illustrated in FIGS. 2A and 2B. A reflow wall 210 which either partially or completely surrounds the solder joint 208 restricts the lateral reflow of the solder during the formation of the solder joint 208 and consequently forms a taller solder joint 208. The solder joint 208 forms electrical connection between the lead frame 203 and the copper post 108 connected to an input/output (I/O) terminal on the overlying semiconductor device 110. The particle roughened surface 202 formed adjacent to the reflow wall 210 on the surface of the lead frame 203 is formed by bonding a particle containing polymeric material to the surface of the lead frame 203. The lead frame 203, reflow wall 210, solder joint 208, copper post 108, particle roughened surface 202, and semiconductor device 110 assembly are covered with molding compound 112 to form the packaged semiconductor device 200.

[0028] A top view of the lead frame 203 is shown in FIG. 4. The lead frame 203 is comprised of number of leads 205 with particle roughened surfaces 202. Reflow walls 210 may also be formed on the leads 205 adjacent to the particle roughened surfaces 202.

[0029] The particle roughened surfaces 202 may be a particle containing polymeric material that is ink jet printed or screen printed onto a portion of the surface of lead frame 203 that is adjacent to the solder joints 208. The polymeric material may be a polyimide or epoxy resin. In one example, the particle roughened surface 202 includes an ink residue having polymeric material. The ink residue is formed in response to printing ink having polymeric material from an inkjet printer which is subsequently cured to form the ink residue having polymeric material. The

particles that formed the particle roughened surface 202 are typically nonmetallic to avoid forming shorts. Particle sizes may range from nanometers to microns. Larger size particles may be used for screen printing pastes than may be used for ink jet printable inks. The particles may be regularly shaped such as spheres or ovals or may have irregular shapes.

[0030] The particle roughened surface 202 provides for improved adhesion between the molding compound 112 and the lead frame 203. The improved adhesion significantly reduces or eliminates packaged semiconductor device 200 failures due to delamination of the molding compound 112 from the lead frame 203.

[0031] As is illustrated in FIGS. 3A and 3B, reflow walls 210 may completely surround the solder joint 208 or may confine the solder reflow on at least two sides. The inside surface 214 of solder wall 210 restricts the lateral flow of solder when the solder joint 208 is formed resulting in a taller solder joint 208. The taller solder joint 208 increases the distance 215 between the semiconductor device 210 and the lead frame 203. The increased distance reduces stress on the solder joint 208 as a result of the mismatch in thermal expansion (coefficient of thermal expansion (CTE) mismatch) between the semiconductor device 110 and the underlying lead frame 203 to which it is attached. Under some circumstances, particularly temperature extremes, mismatches in thermal expansion can lead to solder joint failure.

[0032] The reflow wall 210 may be formed of a polymeric material such as a polyimide, polyester, or epoxy or may be formed of a polymeric material containing nonmetallic or metallic particles. Particles embedded in the polymer reinforce the reflow wall 210. When the particles are formed of a solderable metal, the solder in the solder joint 208 may bond to the particles and increase the strength of the solder joint 208. The stronger solder joint 208 may reduce the failure rate of the solder joints 208 due to mechanical or thermal stress. A solderable metal may be a metal such as copper, silver, gold, platinum, nickel, palladium, brass, or alloys thereof that is easily wetted by molten solder during reflow.

[0033] Perspective views of example reflow walls 210 are shown in FIGS. 3A and 3B. Reflow walls have a thickness 219. Although circular and rectangular reflow walls 210 are depicted in FIGS. 3A and 3B other shapes such as ovals, octagons, squares, and other shapes may be used. The reflow walls 210 may completely surround the solder joint as shown in FIG. 3A in a circular shape or may confine the solder joint 208 on four sides of a rectangle as shown in FIG. 3B. The

cross section of the reflow wall 210 in FIGS. 2A, and 2B are taken along the dashed line, 2A and 2B, in FIGS. 3A and 3B.

[0034] Figure 5A and 5B are cross sections illustrating the formation of solder joints between a semiconductor device 110 and a lead frame 203. As is illustrated in FIG. 5A, solder caps 111 on top of copper posts 108 that project downward from I/O's on the semiconductor device 110 may be positioned inside the reflow wall 210 prior to reflowing the solder and forming the solder joints 208 between the copper posts 108 and the surface of the lead frame 203. In a first alternative process as shown in FIG. 5B, the cavity between the reflow walls 210 may first be filled with a solder paste 113 and the top of the copper post 108 brought into contact with the solder paste 113 prior to reflowing the solder paste 113 and forming the solder joint 208. In a second alternative process the cavity between the reflow walls 210 may be filled with a solder paste 113 and a copper post 108 with a solder cap 111 may brought into contact with the solder paste 113 prior to reflowing the solder paste 113 and forming the solder joint 208.

[0035] The volume of solder in the solder cap 111 or the volume of the solder paste 113 inside the cavity between the reflow walls 210 is chosen so the solder joint 208 is at least as tall as the solder wall 210. The volume of the solder 111, 113 is preferably chosen so that the height of the solder joint is greater than the height of the solder wall. The height of the solder joint 208 may be increased by increasing the height of the reflow wall 210. Increased height of the solder joint 208 may improve solder joint reliability.

[0036] The particle roughened surface 202 in FIG. 6 may be formed using ink jet printing to dispense a particle containing ink onto the surface of the lead frame 603. The ink may be comprised of particles 605 dispersed in a resin 604 such as a polyimide or epoxy resin. After the ink is dispensed onto the surface, the ink may be thermally cured at a temperature in the range of about 80 °C to 300 °C to drive off solvent forming the particle roughened surface 202.

[0037] Alternatively screen printing may be used to apply a screen print paste to the surface of the lead frame 603. The screen print paste may be formed of particles 203 dispersed in a resin 604 such as a polyimide or epoxy resin. After the screen print paste is dispensed onto the surface it may be thermally cured at a temperature in the range of about 180 C to 300 C to drive off solvent forming the particle roughened surface 202.

[0038] As is illustrated in FIGS. 7A and 7B, PCB solder pads 702 and 705 may be formed on the bottom side of the lead frame 703. FIG. 7A shows a PCB solder pad 702 formed using solder

paste 704. Shown in FIG. 9A is a packaged semiconductor device 900 with a PCB solder pad 702 formed on the bottom side of the packaged semiconductor device 900 using solder paste 704. FIG. 7B shows a PCB solder pad 705 on the bottom side of the lead frame 703 formed using a solder paste 704 in which solderable particles 708 are dispersed. Shown in FIG. 9B is a packaged semiconductor device 901 with a PCB solder pad 705 formed on the bottom side using solder paste 704 in which solderable particles 708 are dispersed. The solderable particles 708 may be formed of metals such as silver, gold, platinum, nickel, palladium, brass, or alloys thereof. The solderable particles 708 add reinforcement to solder joints formed between the PCB solder pad 705 on the bottom side of the lead frame 703 and an electrical lead on a printed circuit board. Forming PCB solder pads 702 and 705 on the bottom side of the lead frame 903 using ink jet printing or screen printing eliminates the expensive step of electroplating these pads during lead frame 903 manufacture.

[0039] FIGS. 8A, 8B, and 8C illustrate a few reflow sidewall 810 options. FIG. 8A shows a reflow sidewall 810 that is composed of a polymeric material 802 such as polyimide, epoxy or polyester. Shown in FIG. 9A is a packaged semiconductor device 900 with a reflow sidewall 810 composed of a polymeric material 802. FIG. 8B shows a reflow sidewall 810 that is composed of solderable particles 804 dispersed in a polymeric material 802. FIG. 9B shows a packaged semiconductor device 901 with a reflow sidewall 810 composed of solderable particles 804 dispersed in a polymeric material 802. FIG. 8C shows a reflow sidewall 810 that is composed of solderable particles 804 dispersed in a polymeric material 802. A solder pad 806 that is composed of solderable particles 809 dispersed in solder flux 811 is formed on the surface of the lead frame 903 between the reflow walls 810. FIG. 9C shows a packaged semiconductor device 905 with a reflow sidewall 810 composed of solderable particles 804 dispersed in a polymeric material 802 and with a solder pad 806 that is composed of solderable particles 809 dispersed in solder flux 811 on the surface of the lead frame 903 between the reflow walls 810. In one example, the solderable particles 804 dispersed in solder flux 811 is deposited on the surface prior to attaching the solder joint 208.

[0040] As is illustrated in FIG. 10, solder pads 910 may be formed on the topside of the lead frame 903 where the semiconductor device 110 is mounted to form packaged semiconductor device 907. These topside solder pads 910 may be formed using the same material and process as is used to form the PCB solder pads, 702 and 705, on the bottom side of the lead frame 903.

[0041] The major steps for forming particle roughened surface areas 202 and reflow walls 810 are described in cross sections in FIGS. 11A through 11C and FIGS. 13A through 13C.

[0042] A first method for forming reflow walls 809 and a particle roughened surface 202 on a lead frame 903 using ink jet printing is illustrated in FIGS. 11A through 11C.

[0043] In FIG. 11A the reflow wall 809 is printed onto the surface of the lead frame 903 using an ink jet printer 174.

[0044] FIG. 11B illustrates the deposition of a particle roughened surface 162 on the lead frame 903 using an ink jet printer 176. The ink may be the same ink used to print the reflow wall 810 or it may be a different ink.

[0045] FIG. 11C shows the structure after sintering at a temperature in the range of about 80 °C and about 300 °C to form the particle roughened surface 202 and to form the reflow wall 810.

[0046] A second method for forming a particle roughened surface 202 and reflow walls 810 on a lead frame 903 using screen printing is illustrated in FIGS. 13A through 13C.

[0047] In FIG. 13A a first stencil 180 is positioned on the surface of the lead frame 903 and a first paste 182 is applied to areas where a particle roughened surface 202 is to be formed. The first stencil 180 is removed after the first paste 182 is applied.

[0048] In FIG. 13B a second stencil 184 is positioned on the surface of the lead frame 903 and a second paste 186 is applied to areas where the reflow walls 810 are being formed. The second stencil 184 is removed after the second paste 184 is applied.

[0049] FIG. 13C shows the lead frame 903 after the pastes are sintered at a temperature in the range of about 80 °C and about 300 °C to form the reflow wall 810 and the particle roughened surface 202.

[0050] The method illustrated in FIG.13A through 13C, enables the reflow wall 810 and particle roughened surface 202 to be formed with different thicknesses and to be formed using different pastes. Alternatively, one stencil with openings for both reflow walls 810 and for particle roughened surface 202 may be utilized. In this case the same paste may be used to form both the reflow walls 810 and the particle roughened surface 202. This method may be used to reduce manufacturing cost.

[0051] The major steps for forming PCB solder pads 705 on the backside of the lead frame 903 are described in cross sections in FIGS. 12A and 12B, and in FIGS. 14A and 14B.

[0052] FIG. 12A and 12B illustrate steps in the formation of the PCB solder pads 705 on the bottom side of the lead frame 903 using ink jet printing. As is illustrated in FIG. 12A, the PCB solder pads 701 are printed using an ink jet printer 178. FIG. 12B shows PCB solder pads 705 after the ink is sintered at a temperature in the range of about 80 °C and about 300 °C to drive off solvent and to cure the ink resin.

[0053] FIGS. 14A and 14B illustrate the formation of PCB solder pads 705 on the backside of the lead frame 903 using screen printing.

[0054] In FIG. 14A a stencil 190 is applied to the bottom side of the lead frame 903 with openings where the PCB solder pads 705 are to be formed. The stencil 190 is removed after the paste 704 is applied.

[0055] FIG. 14B shows the lead frame 903 after the paste 192 is sintered at a temperature in the range of about 80 °C and about 300 °C to form the PCB solder pads 705 on the bottom side of the lead frame 903.

[0056] In various example embodiments, terms such as top, bottom, and the like are used in a relative sense to describe a positional relationship of various components. These terms are used with reference to the position of components shown in the drawings, and not in an absolute sense with reference to a field of gravity. For example, the top side of the lead frame 105 would still be properly referred to as the top side of the lead frame, even if the packaged semiconductor devices are placed in an inverted position with respect to the position shown in the drawings.

[0057] While various embodiments of the present disclosure have been described above, it should be understood that they have been presented by way of example only and not limitation. Numerous changes to the disclosed embodiments can be made in accordance with the disclosure herein without departing from the spirit or scope of the disclosure. Thus, the breadth and scope of the present disclosure should not be limited by any of the above described embodiments. Rather, the scope of the disclosure should be defined in accordance with the following claims and their equivalents.

CLAIMS

What is claimed is:

1. A packaged semiconductor device comprising:
 - a lead frame;
 - a semiconductor device;
 - a solder joint coupled between the lead frame and a terminal on the semiconductor device;
 - a particle roughened surface on a portion of a surface of the lead frame and comprised of a first polymer containing first particles; and
 - molding compound covering portions of the semiconductor device, the lead frame, and the particle roughened surface.
2. The packaged semiconductor device of claim 1, in which the first polymer is selected from a group consisting of a polyimide, epoxy, and polyester polymer.
3. The packaged semiconductor device of claim 1, in which the first particles are nonmetallic particles.
4. The packaged semiconductor device of claim 1, in which the particle roughened surface covers portions of the surface of the lead frame adjacent to the solder joint.
5. The packaged semiconductor device of claim 1, comprising:
 - a reflow wall that surrounds the solder joint in which the reflow wall is a second polymer selected from the group consisting of polyimide, epoxy, and polyester.
6. The packaged semiconductor device of claim 5, in which the reflow wall surrounds the solder joint on at least two opposing sides of the solder joint.
7. The packaged semiconductor device of claim 5, in which the reflow wall completely surrounds the solder joint.
8. The packaged semiconductor device of claim 5, comprising of a second polymer containing second particles.
9. The packaged semiconductor device of claim 5, in which a height of the solder joint is at least as high as a height of the reflow wall.
10. The packaged semiconductor device of claim 1, comprising a printed circuit board solder pad on a bottom side of the packaged semiconductor device.

11. The packaged semiconductor device of claim 10, in which the printed circuit board solder pad is solder paste.
12. The packaged semiconductor device of claim 10, in which the printed circuit board solder pad is a solder paste containing solderable particles formed of a metal selected from the group consisting of silver, copper, nickel, palladium, platinum, tin, gold and alloys thereof.
13. The packaged semiconductor device of claim 1 further comprising metallic post coupled between the solder joint and the terminal.
14. A packaged semiconductor device comprising:
 - a lead frame;
 - a semiconductor device;
 - a solder joint coupled between the lead frame and a terminal on the semiconductor device;
 - a particle roughened surface, on a portion of a surface of the lead frame, comprised of a first polymer containing first particles;
 - a reflow wall surrounding the solder joint and comprised of second polymer containing second particles; and
 - molding compound covering portions of the semiconductor device, the lead frame, the metallic post, the reflow wall, and the particle roughened surface.
15. The packaged semiconductor device of claim 14, in which the first polymer and the second polymer are selected from the group consisting of polyimide, epoxy, and polyester polymers.
16. The packaged semiconductor device of claim 14, in which the first polymer and the second polymer are selected from the group consisting of polyimide, epoxy, and polyester polymers and wherein the first and second particles are nonmetallic particles.
17. The packaged semiconductor device of claim 14, in which the first polymer and the second polymer are the same polymer and in which the first particles and the second particles are the same nonmetallic particles.
18. The packaged semiconductor device of claim 14, in which the first polymer and the second polymer are selected from the group consisting of polyimide, epoxy, and polyester polymers and in which the first particles are nonmetallic particles and in which the second

particles are metal particles composed of a solderable metal selected from the group consisting of silver, copper, nickel, palladium, platinum, tin, gold and alloys thereof.

19. The packaged semiconductor device of claim 14, in which the reflow wall surrounds at least two opposing sides of the solder joint.

20. The packaged semiconductor device of claim 14, comprising a printed circuit board solder pad comprised of solder paste on a bottom side of the packaged semiconductor device.

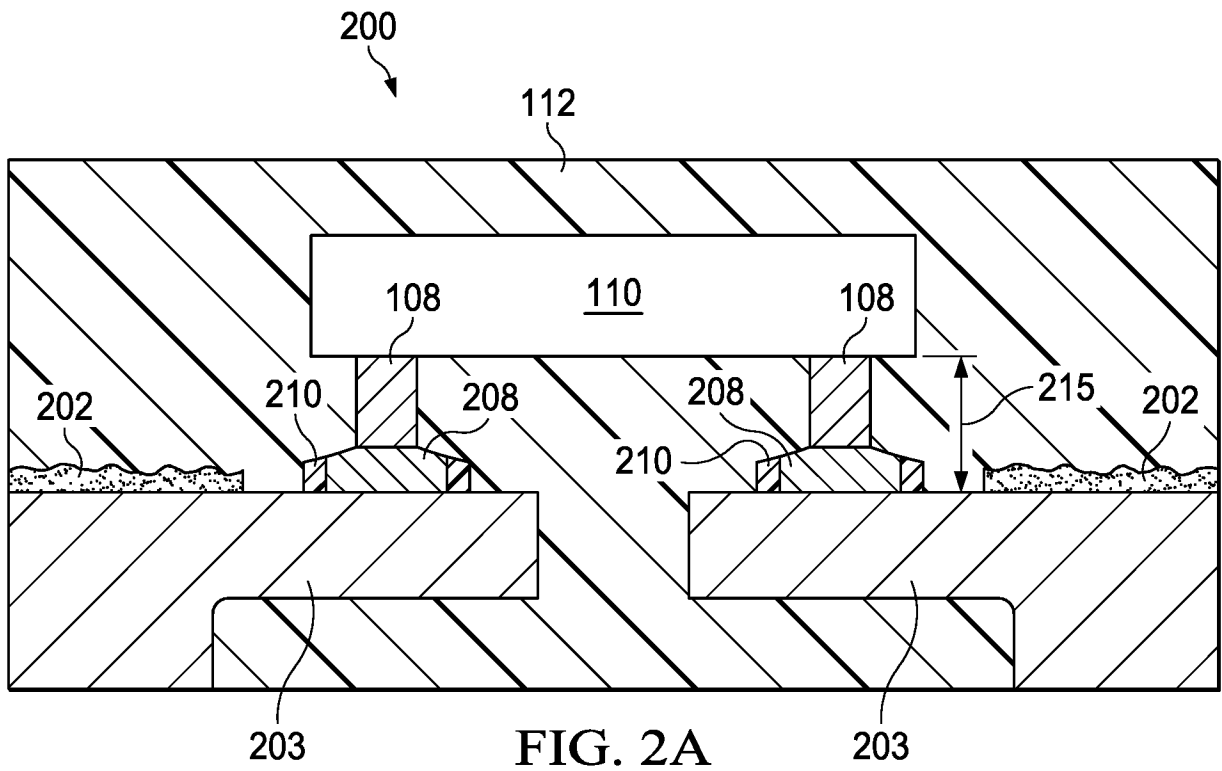


FIG. 2A

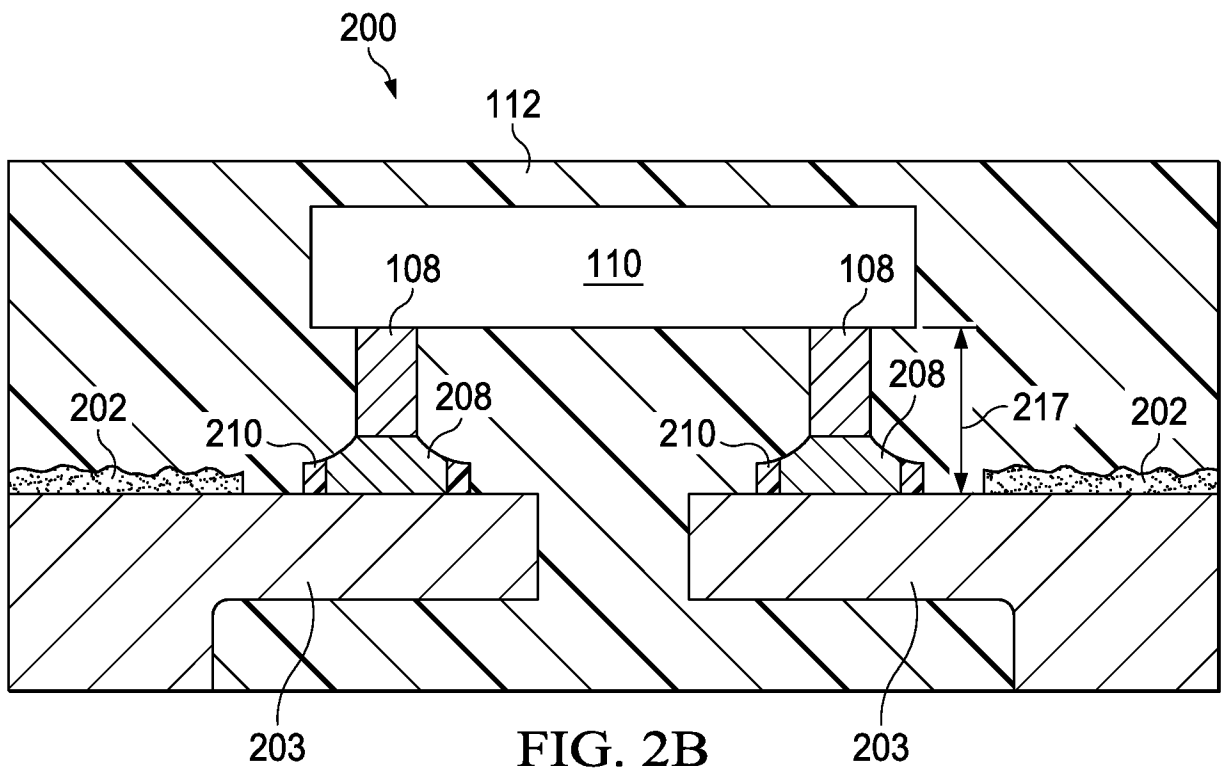


FIG. 2B

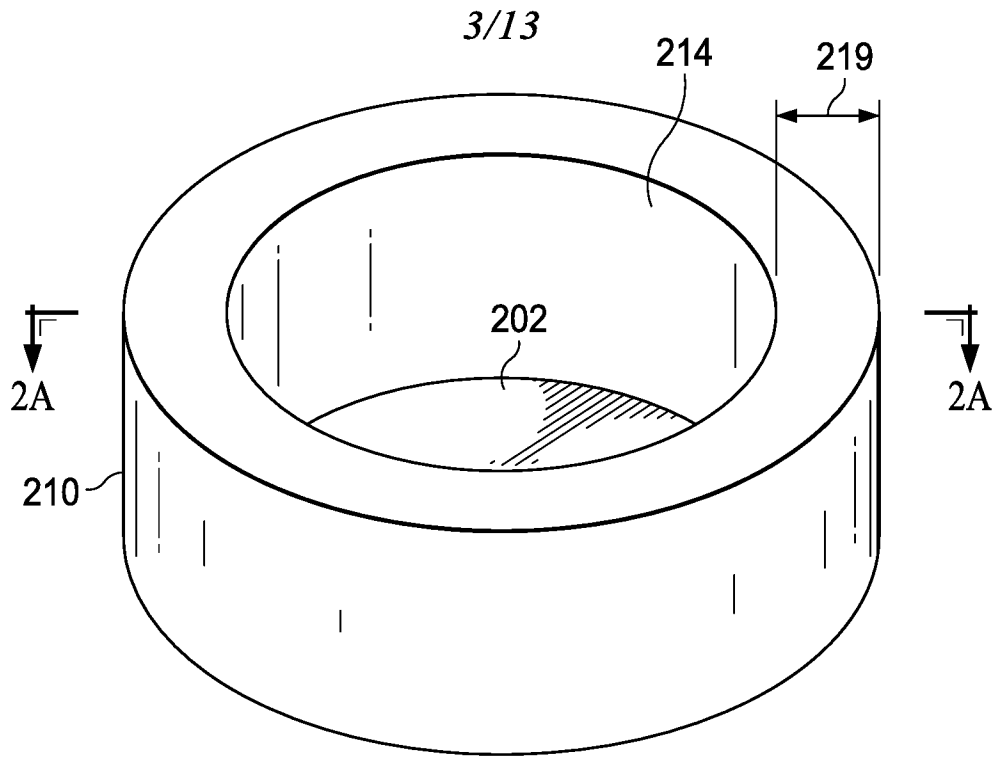


FIG. 3A

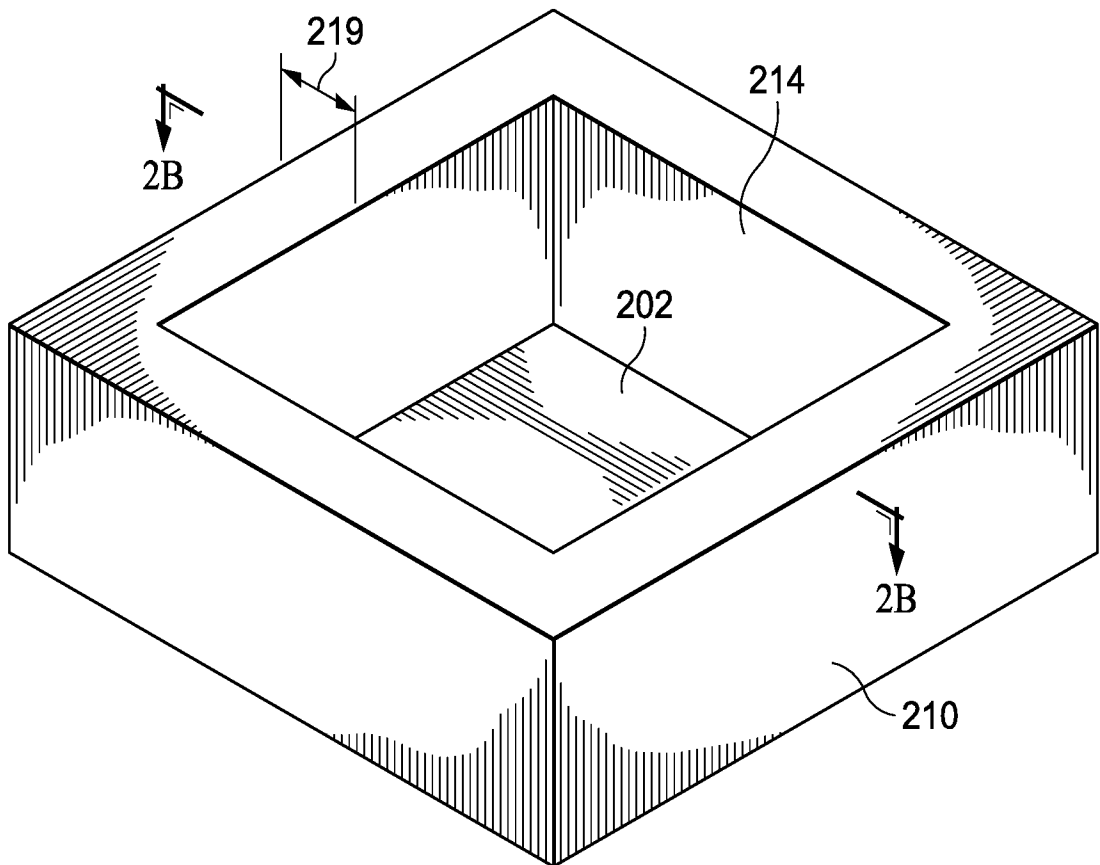


FIG. 3B

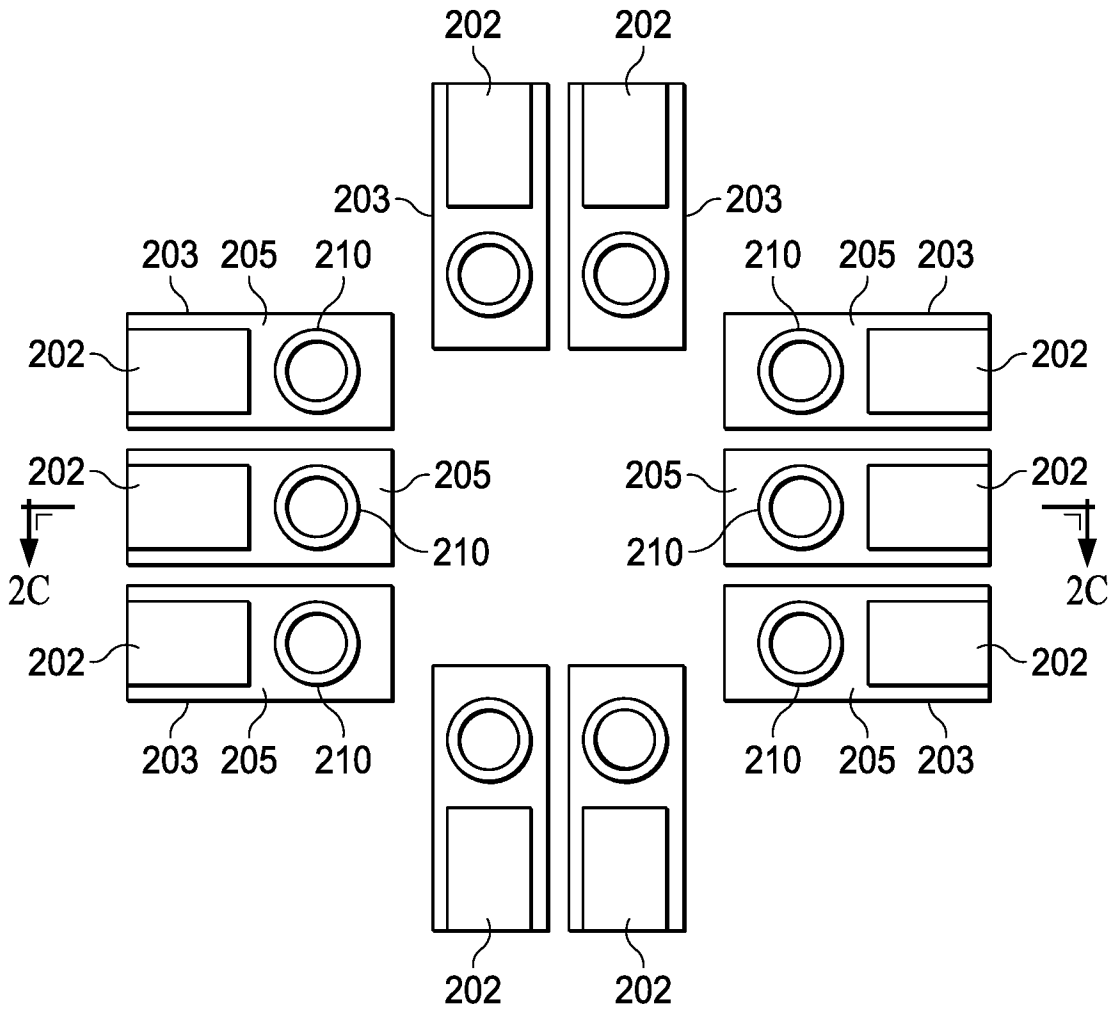


FIG. 4

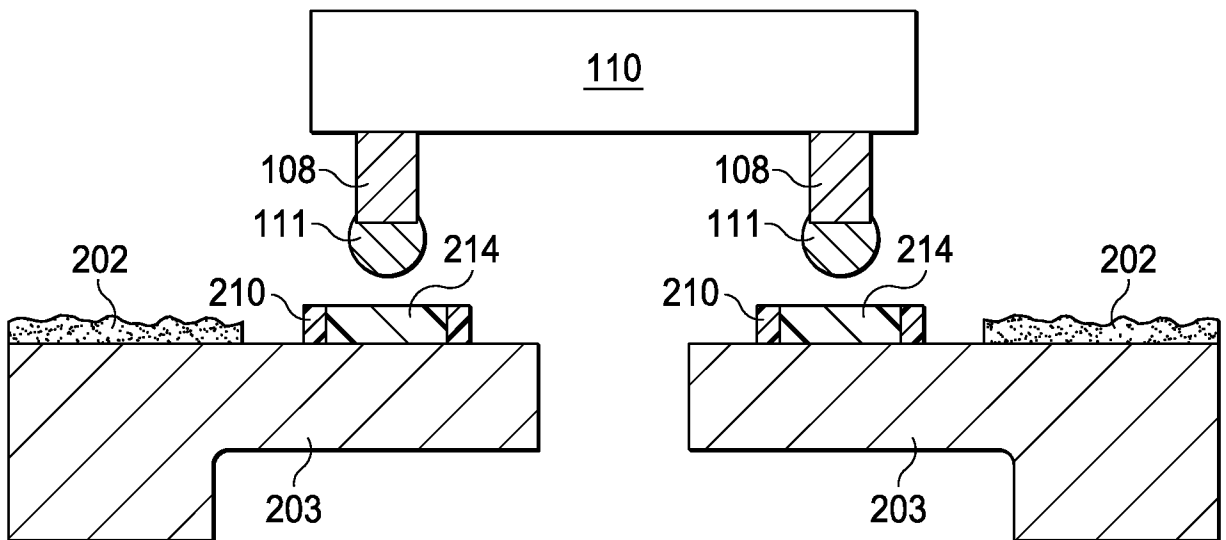


FIG. 5A

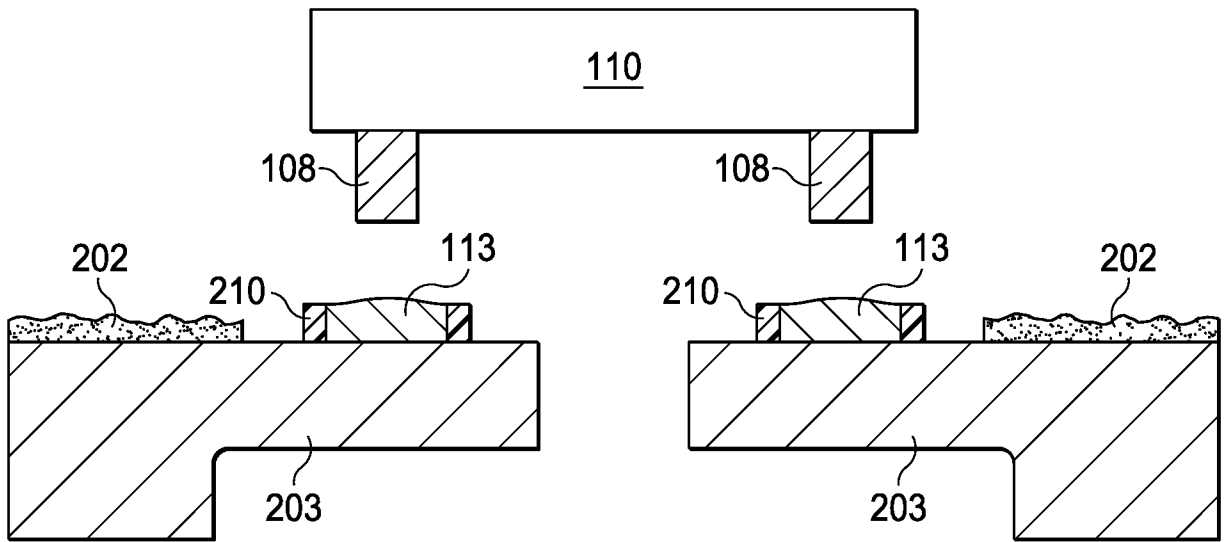


FIG. 5B

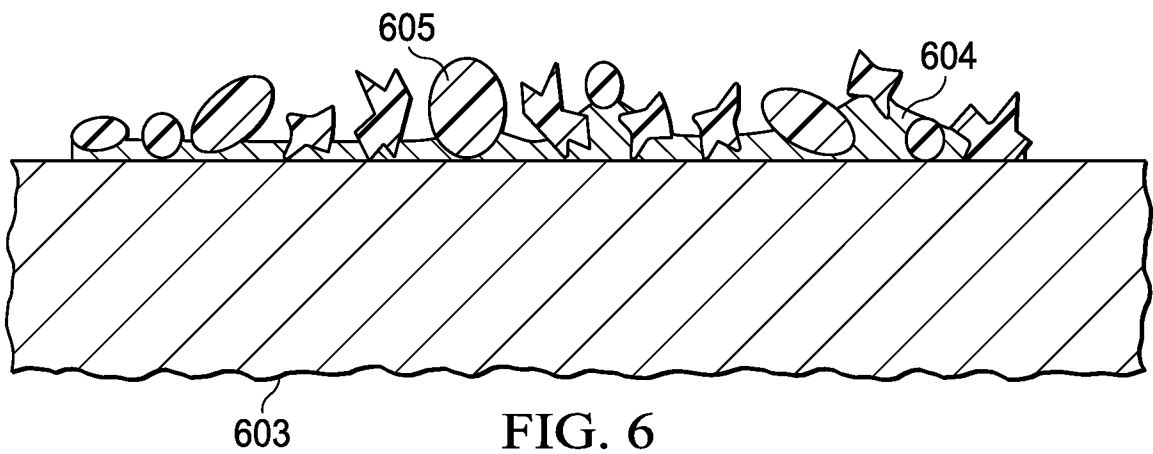
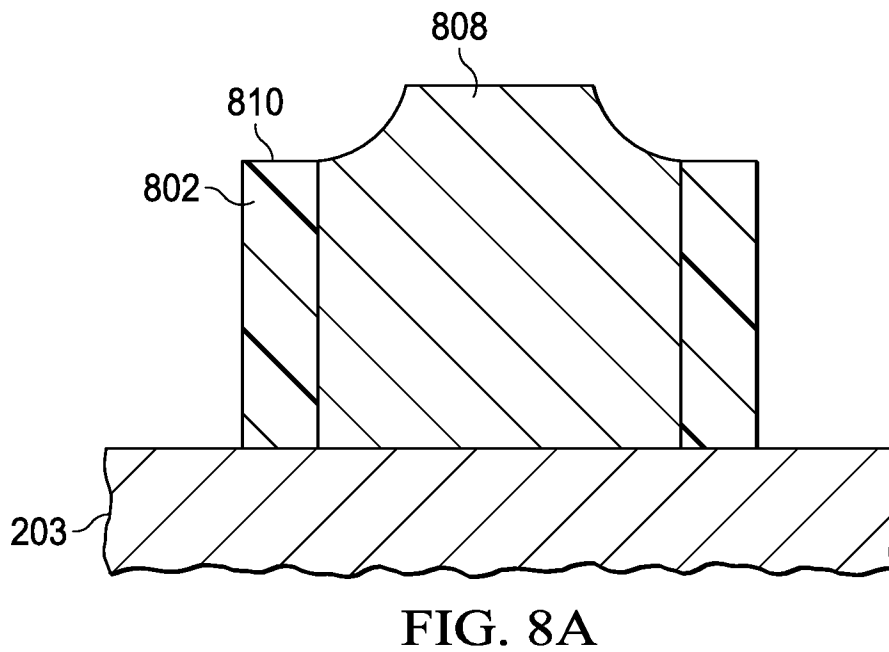
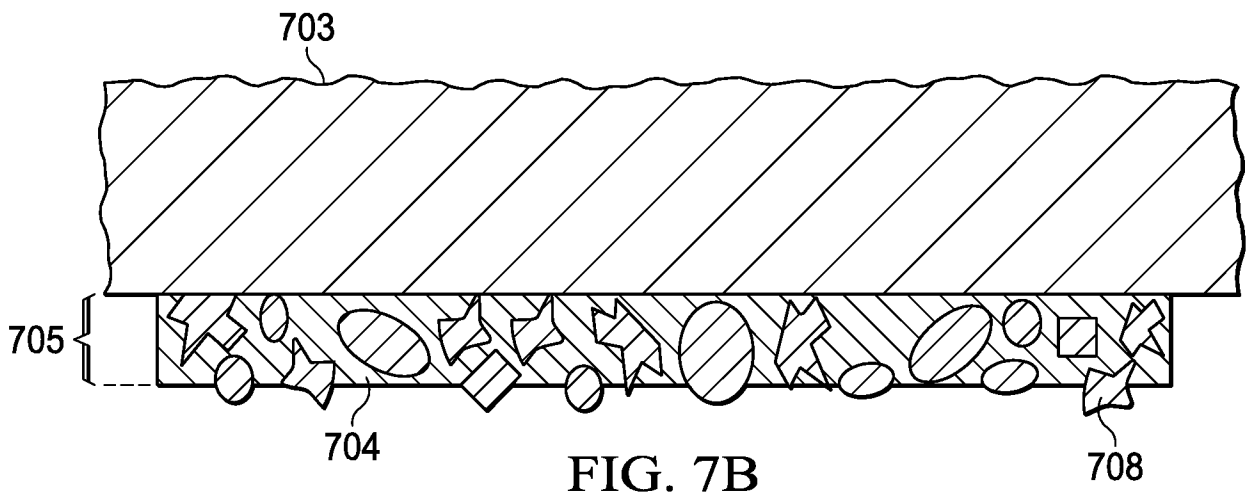
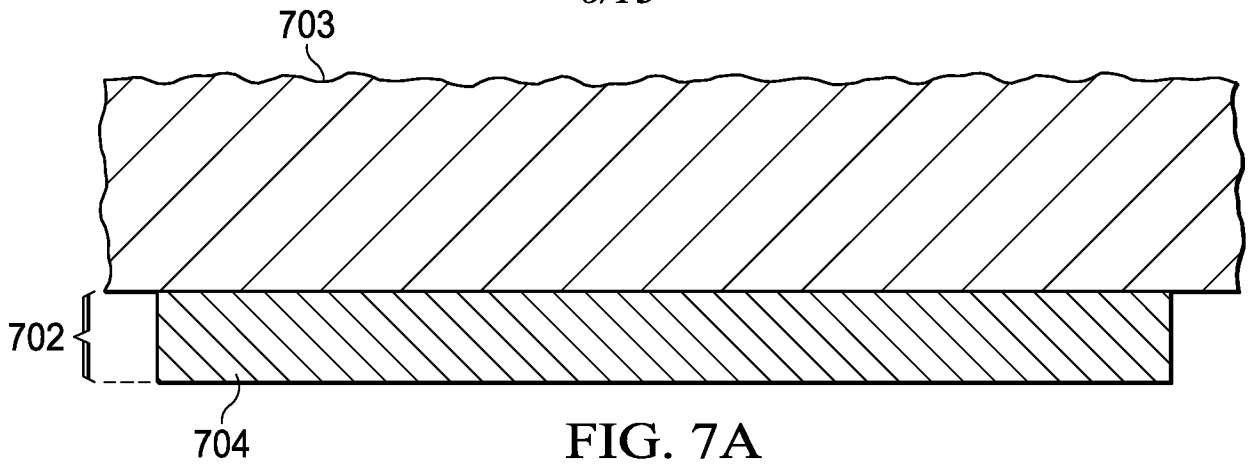


FIG. 6

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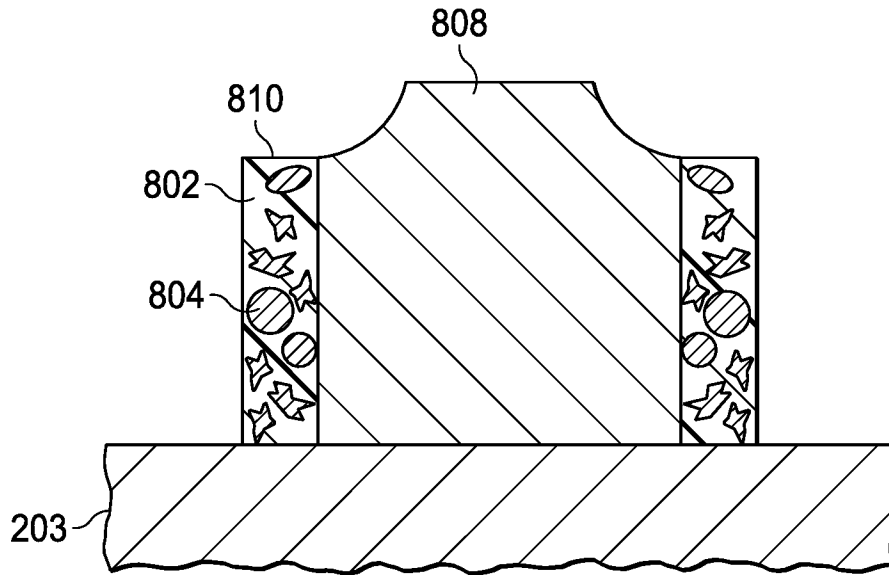


FIG. 8B

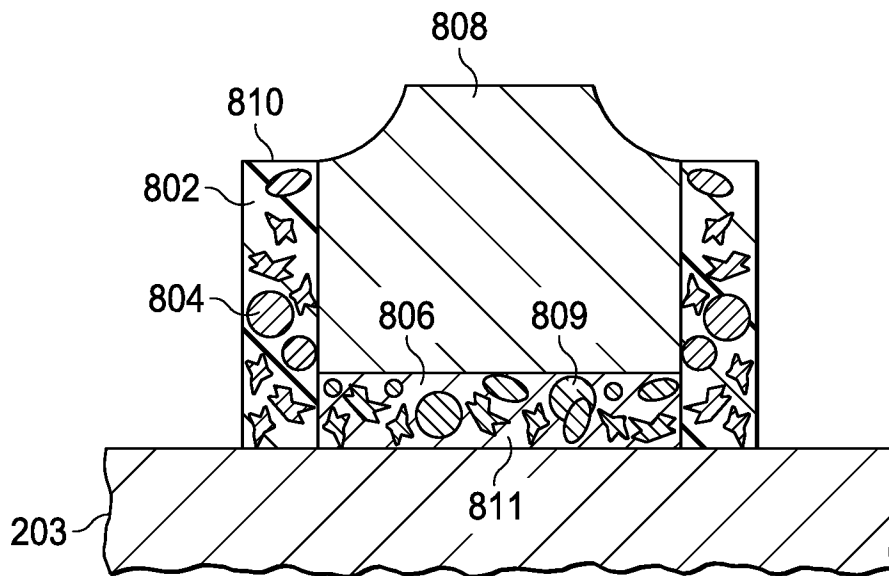


FIG. 8C

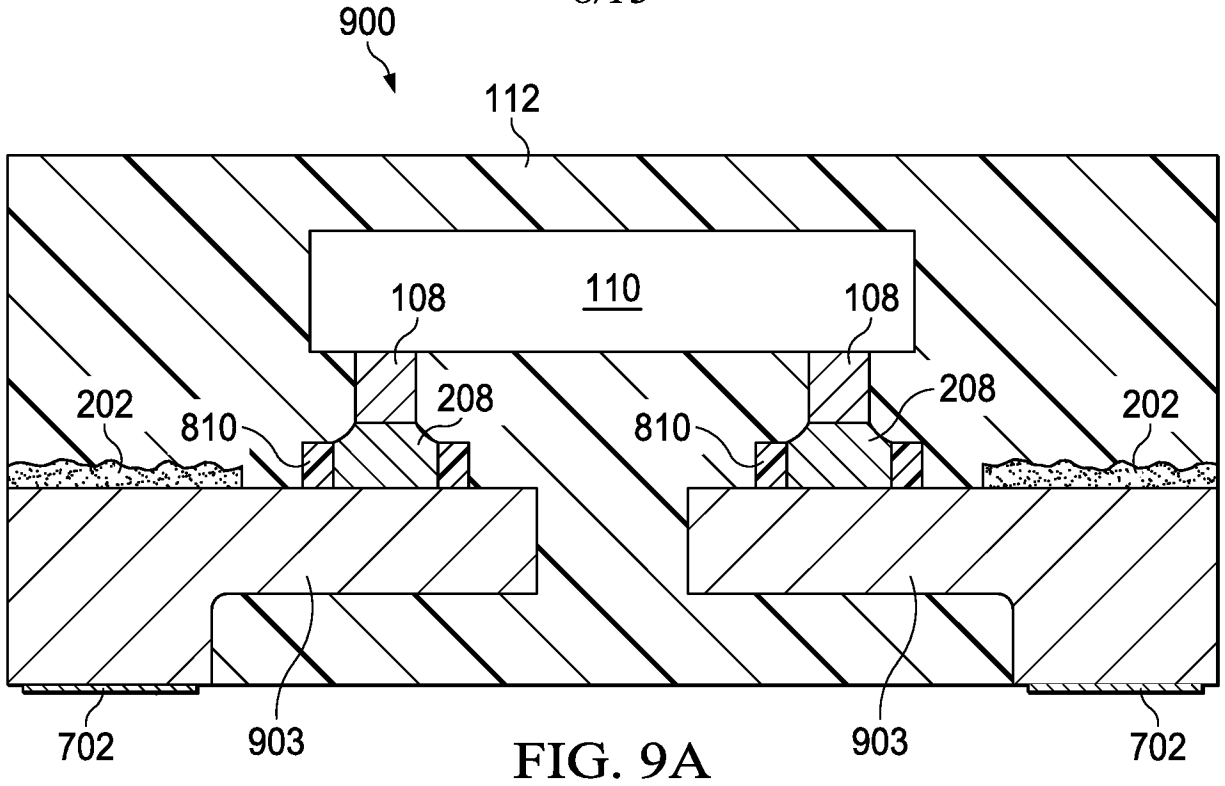


FIG. 9A

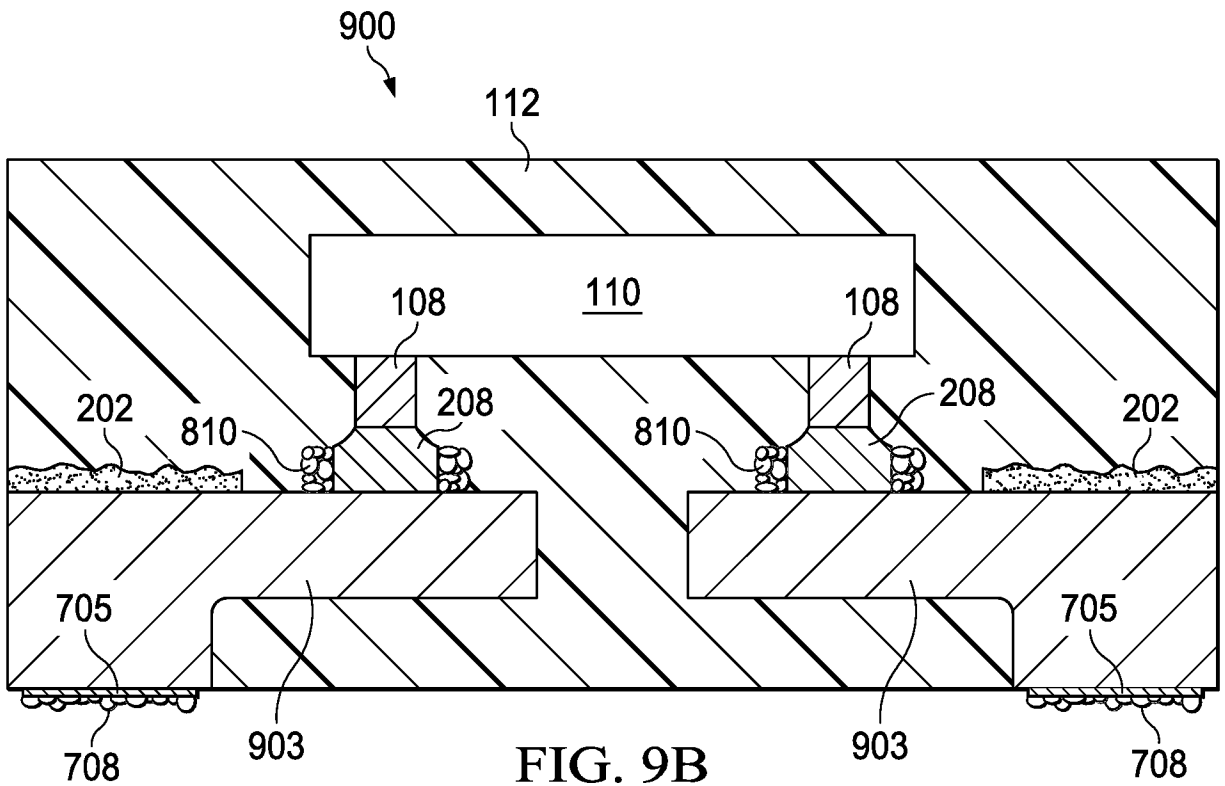


FIG. 9B

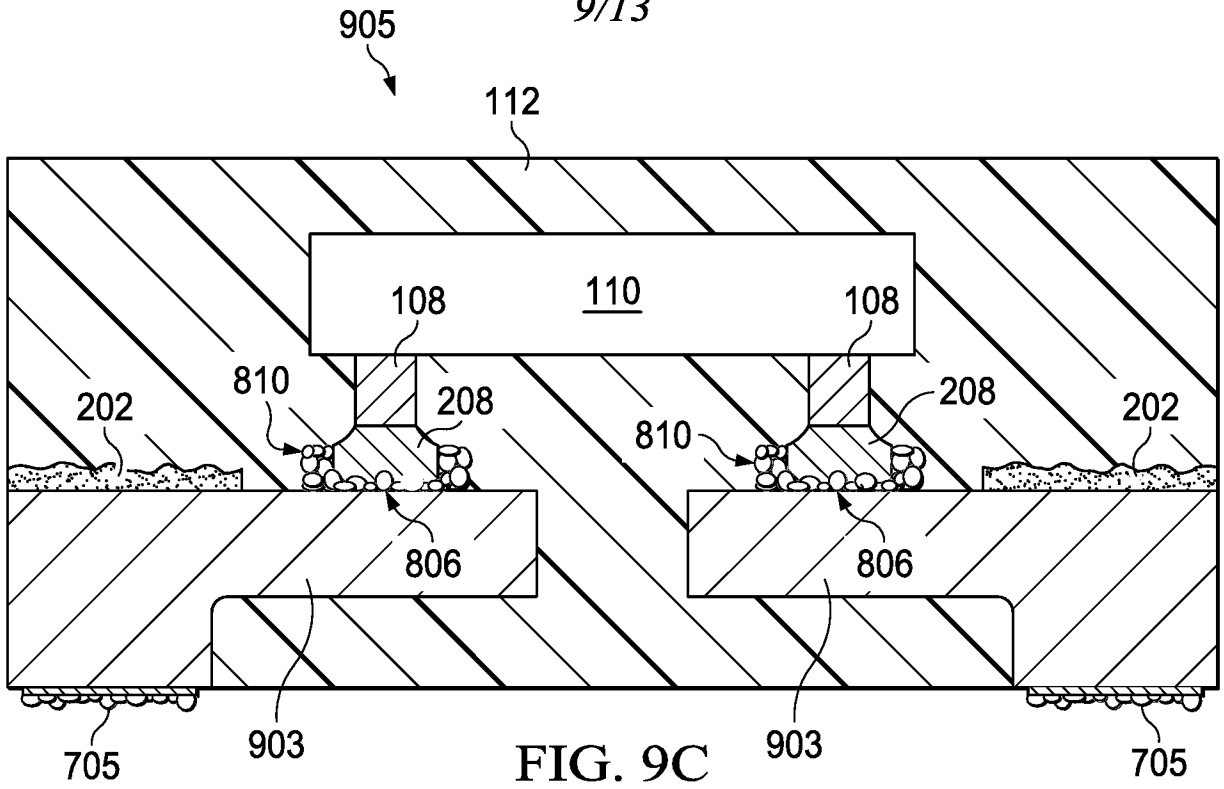


FIG. 9C

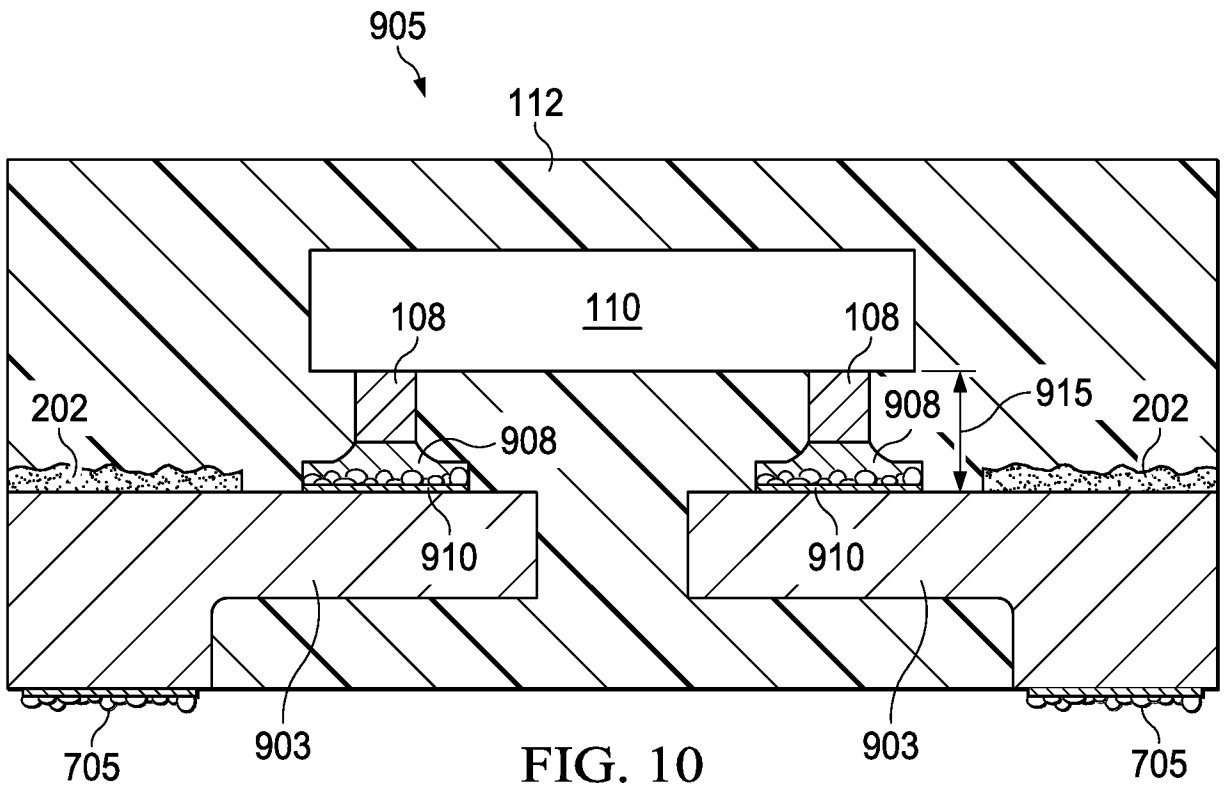


FIG. 10

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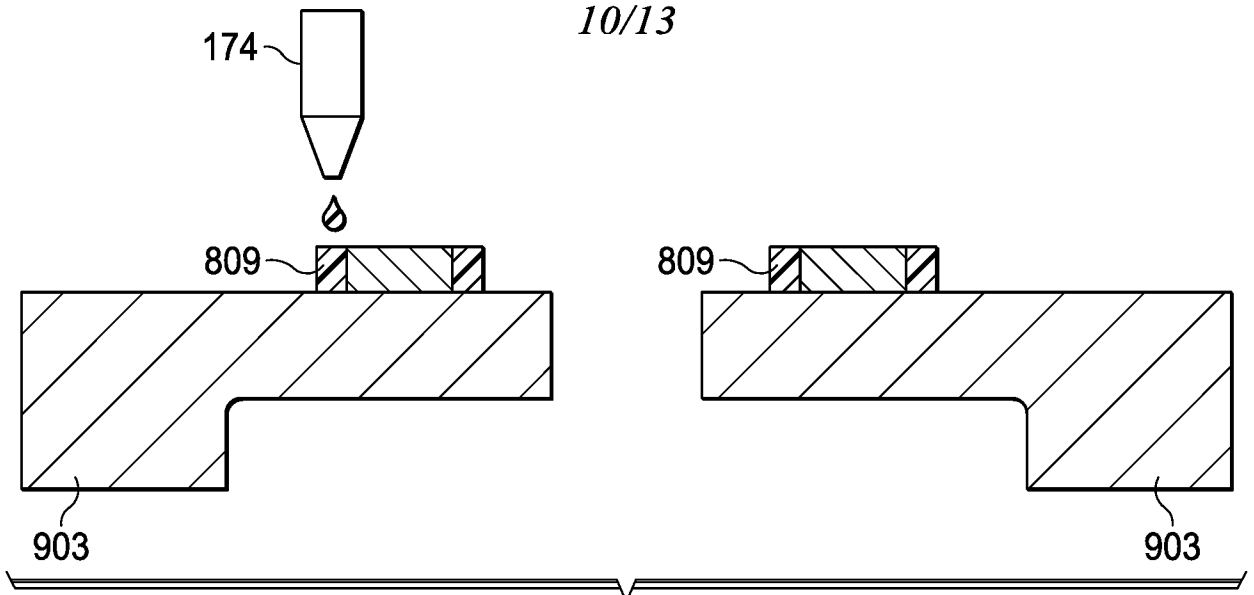


FIG. 11A

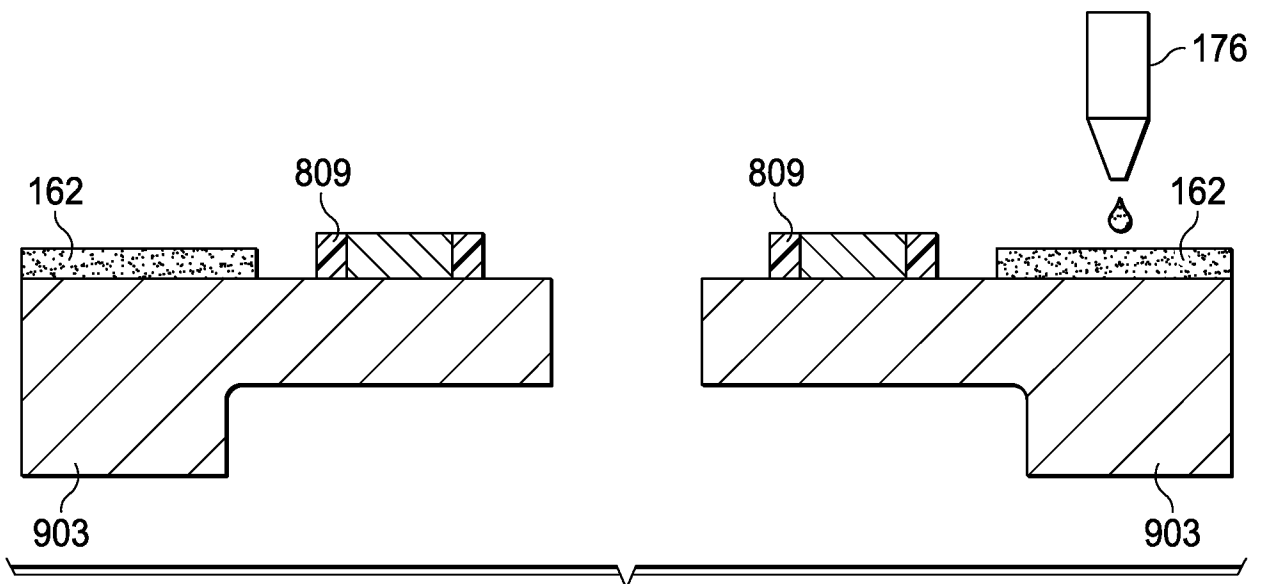


FIG. 11B

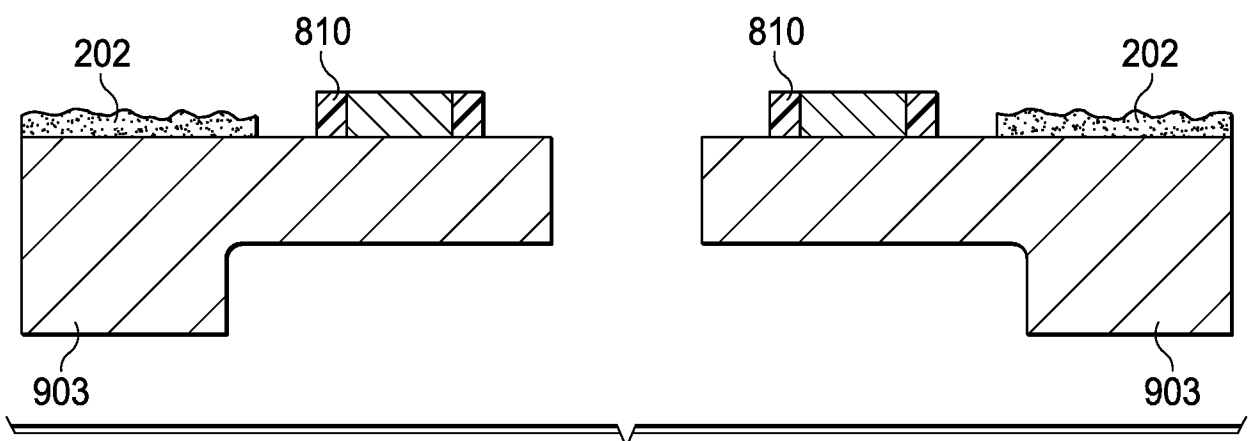


FIG. 11C

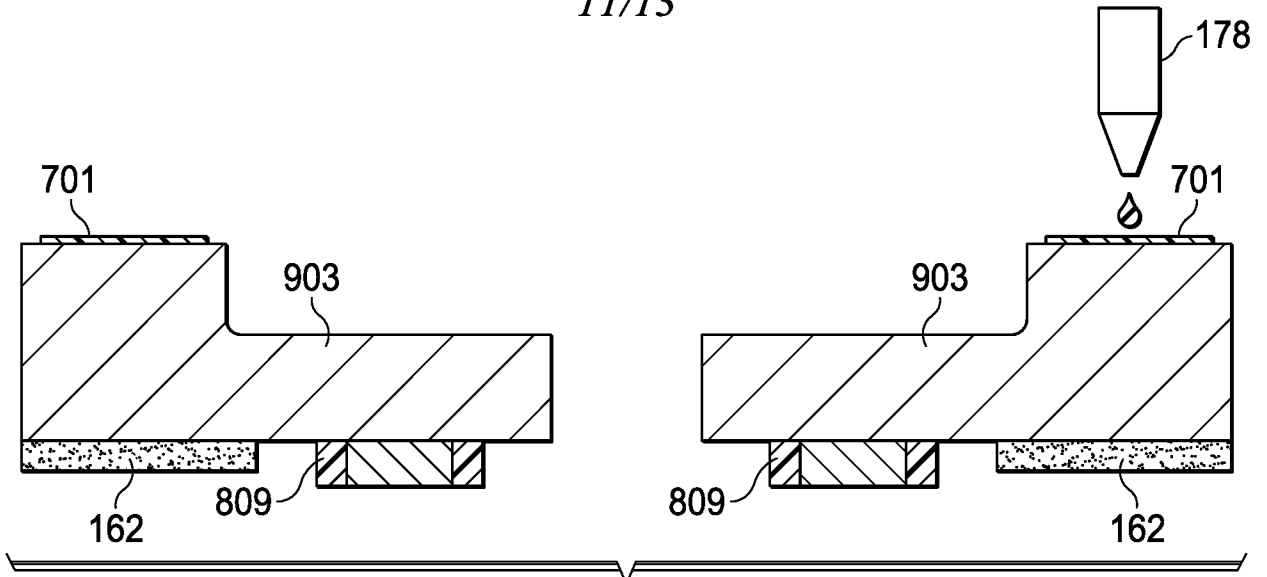


FIG. 12A

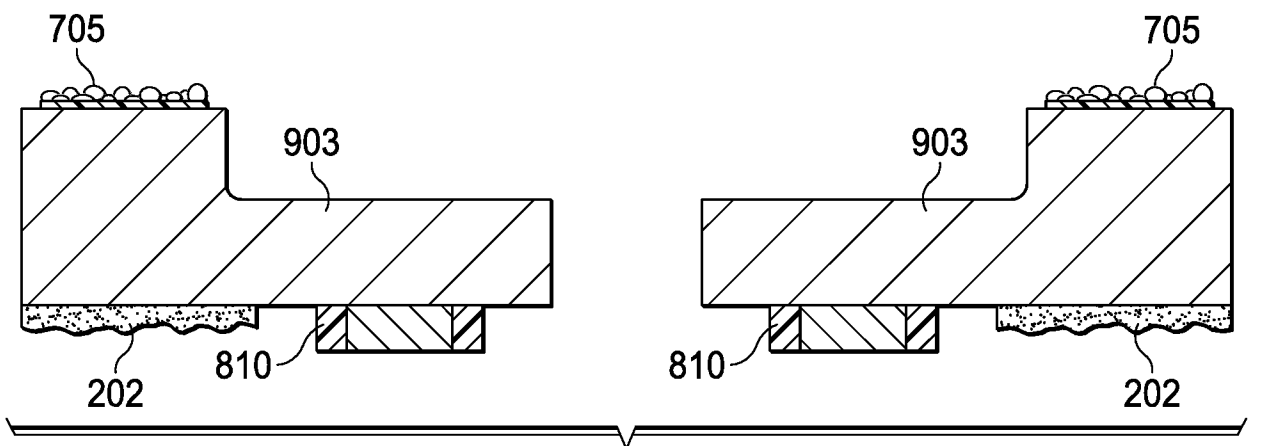


FIG. 12B

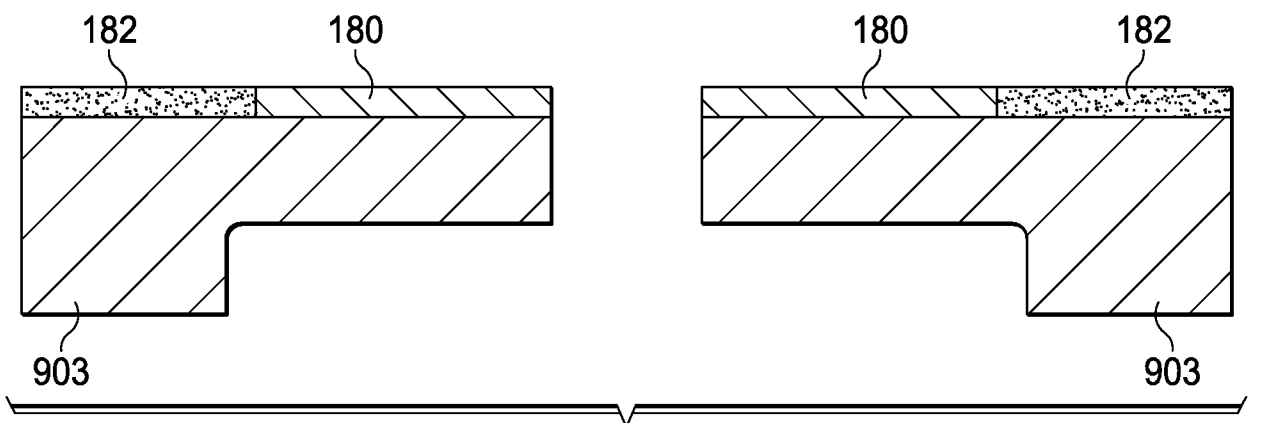


FIG. 13A

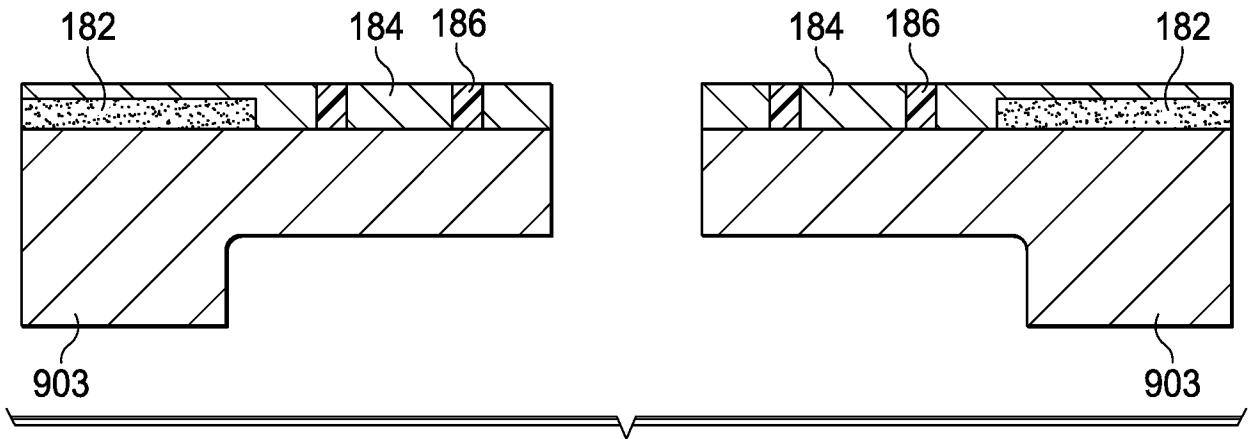


FIG. 13B

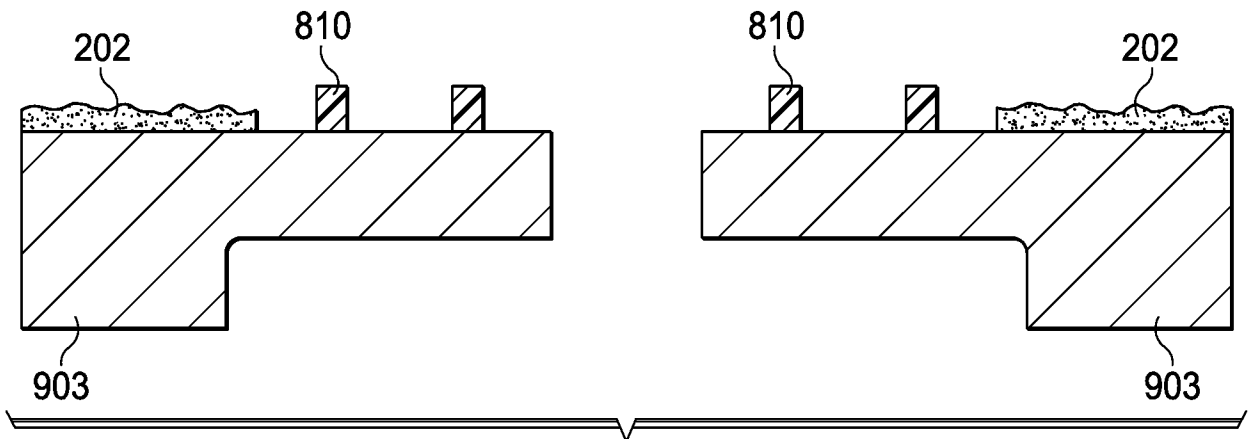


FIG. 13C

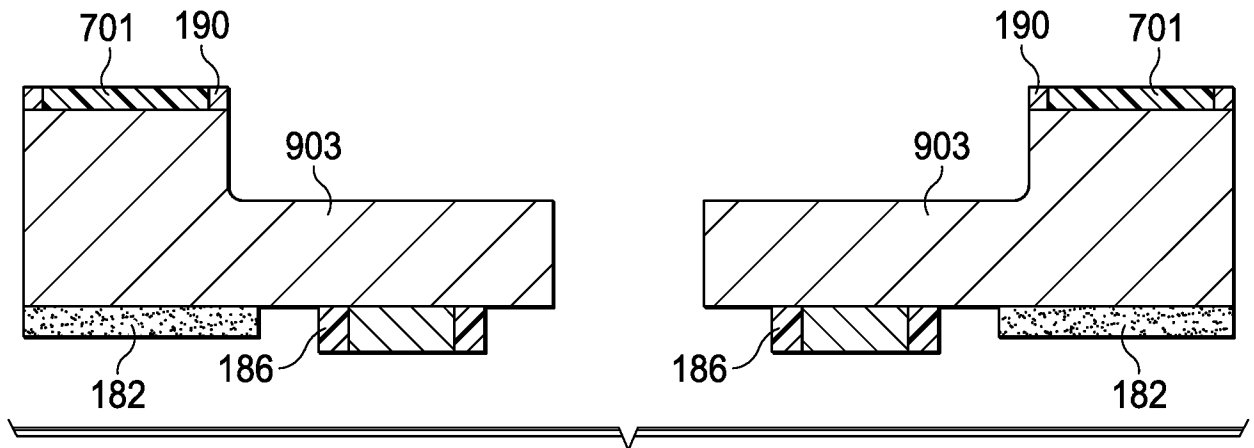


FIG. 14A

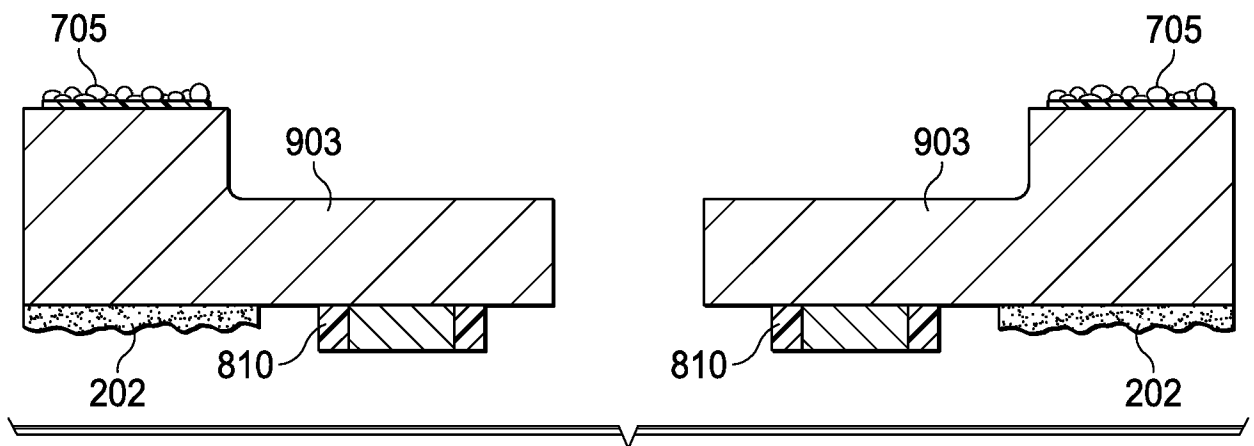


FIG. 14B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/068761

A. CLASSIFICATION OF SUBJECT MATTER		
<i>H01L 23/495 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L 23/48, 23/495, H05K 03/30, 03/32, 03/34, B23K 35/36, C09K 03/10		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/0130397 A1 (CHEE KIANG YEW et al.) 19.09.2002, fig.2, 4, [0033], [0011], [0043]	1-4, 10-13
A		5-9, 14-20
Y	US 2013/0292684 A1 (INFINEON TECHNOLOGIES AG) 26.05.2015, [0039]	1-4, 10-13
Y	RU 2438845 C1 (ОТКРЫТОЕ АКЦИОНЕРНОЕ ОБЩЕСТВО "АВАНГАРД") 10.01.2012, page 7, lines 2-6 from bottom, page 8, lines 11-14 from bottom	11-12
Y	WO 2012/164437 A2 (KONINKLIJKE PHILIPS ELECTRONICS N.V) 06.12.2016, page 12, lines 14-17	13
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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"A" document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document but published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search	Date of mailing of the international search report	
01 March 2018 (01.03.2018)	22 March 2018 (22.03.2018)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer V. Karsanova Telephone No. (499) 240-25-91	