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(74) Agents: KING, Robert L. et al.; 7700 W. Parmer Lane,  
MD:PL02, Austin, Texas 78729 (US).

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(71) Applicant (for all designated States except US):  
FREESCALE SEMICONDUCTOR INC. [US/US];  
6501 William Cannon Drive West, Austin, Texas 78735  
(US).

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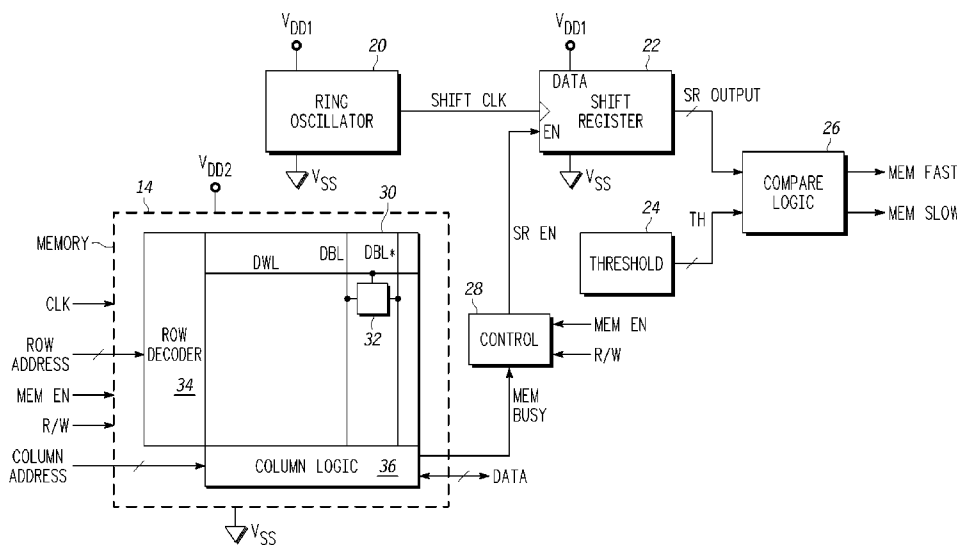
(72) Inventors; and

(75) Inventors/Applicants (for US only): QURESHI, Qadeer  
A. [US/US]; 394 Steamboat Crossing, Dripping Springs,  
Texas 78620 (US). BURNETT, James D. [US/US]; 3804  
Laurel Ledge Lane, Austin, Texas 78731 (US). HIGMAN,  
Jack M. [US/US]; 14024 Timberline Trail, Austin, Texas  
78737 (US). JEW, Thomas [US/US]; 4020 Idalia, Austin,  
Texas 78749 (US).

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(54) Title: APPARATUS AND METHOD FOR ADJUSTING AN OPERATING PARAMETER OF AN INTEGRATED CIRCUIT



(57) Abstract: A method for adjusting an operating parameter of an integrated circuit having a memory (14) and logic (12), where the logic includes a timing circuit, includes accessing the memory, determining a relative speed of the memory access with respect to a speed of the timing circuit, and selectively adjusting the operating parameter based on the relative speed. In one embodiment, an integrated circuit may include a ring oscillator (20), a shift register (22) having a clock input coupled to an output of the ring oscillator, and compare logic (26) coupled to an output of the shift register. The shift register is enabled in response to initiating a memory access to a memory (14) and disabled in response to completing the memory access. The compare logic (26) provides a relative speed indicator representative of a relative speed of the memory.

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## INTERNATIONAL SEARCH REPORT

International application No.

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## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G01R 31/28 (2007.10)

USPC - 714/731

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC - 714/731; 713/300; 324/76.11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 714/731; 713/300; 324/76.11

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST (USPT, PGPB, EPAB, JPAB); DialogPRO (Engineering); Google Scholar

Search term: ring oscillator, shift register, memory, compare logic, integrated circuit, timing circuit, data processing.

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2005/0283630 A1 (SHIKATA) 22 December 2005 (22.12.2005), entire document especially fig 1	1-6, 10, 12-13 and 15-20 ----- 7-9, 11 and 14
Y	US 2002/0191446 A1 (MAKI) 19 December 2002 (14.12.2002), abstract, para [0016]	7-8 and 14
Y	US 2005/0078120 A1 (KONDO et al.) 14 April 2005 (14.04.2005), fig 4, para [0014]	9 and 11

 Further documents are listed in the continuation of Box C.

## \* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

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Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents  
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Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300  
PCT OSP: 571-272-7774