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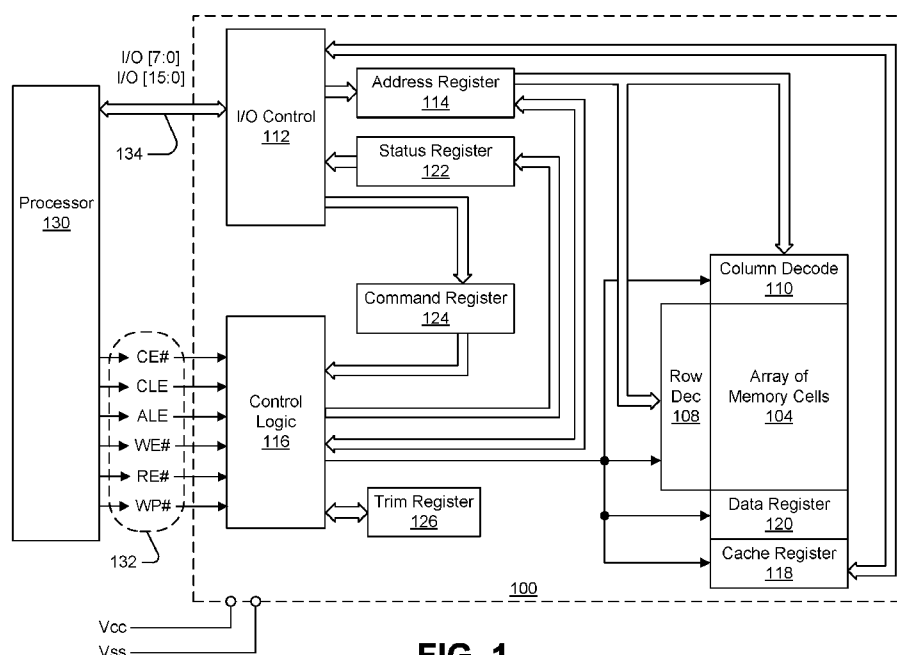


FIG. 1

(57) Abstract: Apparatus and methods of operating such apparatus include applying a first voltage level to a source connected to a first end of a string of series-connected memory cells, applying a second voltage level to a data line connected to a second end of the string of series-connected memory cells, and applying a third voltage level to a first access line coupled to a first memory cell of the string of series-connected memory cells concurrently with applying the first and second voltage levels, wherein the magnitude of the third voltage level is greater than the magnitude of both the first voltage level and the second voltage level, and wherein a polarity and the magnitude of the third voltage level are expected to decrease a threshold voltage of the first memory cell when concurrently applying the first, second and third voltage levels.

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ERASING MEMORY CELLS

TECHNICAL FIELD

[0001] The present disclosure relates generally to memory and, in particular, in one or more embodiments, the present disclosure relates to erasing memory cells.

BACKGROUND

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuit devices in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and flash memory.

[0003] Flash memory has developed into a popular source of non-volatile memory for a wide range of electronic applications. Flash memory typically use a one-transistor memory cell that allows for high memory densities, high reliability, and low power consumption. Changes in threshold voltage (V_t) of the memory cells, through programming (which is often referred to as writing) of charge storage structures (e.g., floating gates or charge traps) or other physical phenomena (e.g., phase change or polarization), determine the data state (e.g., data value) of each memory cell. Common uses for flash memory and other non-volatile memory include personal computers, personal digital assistants (PDAs), digital cameras, digital media players, digital recorders, games, appliances, vehicles, wireless devices, mobile telephones, and removable memory modules, and the uses for non-volatile memory continue to expand.

[0004] A NAND flash memory is a common type of flash memory device, so called for the logical form in which the basic memory cell configuration is arranged. Typically, the array of memory cells for NAND flash memory is arranged such that the control gate of each memory cell of a row of the array is connected together to form an access line, such as a word line. Columns of the array include strings (often termed NAND strings) of memory cells connected together in series between a pair of select gates, e.g., a source select transistor and a drain select transistor. Each source select transistor may be connected to a source, while each drain select transistor may be connected to a data line, such as column bit line. Variations using more than

one select gate between a string of memory cells and the source, and/or between the string of memory cells and the data line, are known.

[0005] Memory cells are typically erased before they are programmed to a desired data state. For example, memory cells of a particular block of memory cells may first be erased and then selectively programmed. For a NAND array, a block of memory cells is typically erased by grounding all of the access lines (e.g., word lines) in the block and applying an erase voltage to the channels of the memory cells (e.g., through data lines and source connections) in order to remove charges that might be stored on charge storage structures (e.g., floating gates or charge traps) of the block of memory cells. Typical erase voltages might be on the order of 25V before completion of an erase operation. For programming of these memory cells, one or more programming pulses are typically applied to a selected access line connected to a control gate of each memory cell associated with that selected access line. Typical programming pulses might start at or near 15V and may increase in magnitude during each subsequent programming pulse application. Programming pulses on the order of 25V might be experienced before completion of a programming operation. While the programming pulse is applied to the selected access line, a ground potential might be applied to the channels of the memory cells, resulting in a charge transfer from the channel to the charge storage structures of memory cells targeted (e.g., selected) for programming.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a simplified block diagram of a memory in communication with a processor as part of an electronic system, according to an embodiment.

[0007] Figures 2A-2B are schematics of portions of an array of memory cells as could be used in a memory of the type described with reference to Figure 1.

[0008] Figure 3 is a cross-sectional view of a portion of an array of memory cells as could be used in a memory of the type described with reference to Figure 1.

[0009] Figure 4A is a schematic of a portion of an array of memory cells as could be used in a memory device of the type described with reference to Figure 1.

[0010] Figure 4B is a cross-sectional view of a block select transistor of Figure 4A.

[0011] Figures 5A-5B are flowcharts of methods of operating a memory device according to embodiments.

DETAILED DESCRIPTION

[0012] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments. In the drawings, like reference numerals describe substantially similar components throughout the several views. Other embodiments may be utilized and structural, logical and electrical changes may be made without departing from the scope of the present disclosure. The following detailed description is, therefore, not to be taken in a limiting sense.

[0013] Figure 1 is a simplified block diagram of a first apparatus, in the form of a memory (e.g., memory device) 100, in communication with a second apparatus, in the form of a processor 130, as part of a third apparatus, in the form of an electronic system, according to an embodiment. Some examples of electronic systems include personal computers, personal digital assistants (PDAs), digital cameras, digital media players, digital recorders, games, appliances, vehicles, wireless devices, cellular telephones and the like. The processor 130, e.g., a controller external to the memory device 100, may be a memory controller or other external host device.

[0014] Memory device 100 includes an array of memory cells 104 logically arranged in rows and columns. Memory cells of a logical row are typically connected to the same access line (commonly referred to as a word line) while memory cells of a logical column are typically selectively connected to the same data line (commonly referred to as a bit line). A single access line may be associated with more than one logical row of memory cells and a single data line may be associated with more than one logical column. Memory cells (not shown in Figure 1) of at least a portion of array of memory cells 104 are capable of being programmed to one of at least two data states.

[0015] A row decode circuitry 108 and a column decode circuitry 110 are provided to decode address signals. Address signals are received and decoded to access the array of memory cells 104. Memory device 100 also includes input/output (I/O) control circuitry 112 to manage input of commands, addresses and data to the memory device 100 as well as output of data and status information from the memory device 100. An address register 114 is in communication

with I/O control circuitry 112 and row decode circuitry 108 and column decode circuitry 110 to latch the address signals prior to decoding. A command register 124 is in communication with I/O control circuitry 112 and control logic 116 to latch incoming commands. A trim register 126 may be in communication with the control logic 116 to store trim data. Although depicted as a separate storage register, trim register 126 may represent a portion of the array of memory cells 104.

[0016] A controller (e.g., control logic 116 internal to the memory device 100) controls access to the array of memory cells 104 in response to the commands and generates status information for the external processor 130, i.e., control logic 116 is configured to perform access operations (e.g., read operations, program operations and/or erase operations) in accordance with embodiments described herein. The control logic 116 is in communication with row decode circuitry 108 and column decode circuitry 110 to control the row decode circuitry 108 and column decode circuitry 110 in response to the addresses.

[0017] Control logic 116 is also in communication with a cache register 118. Cache register 118 latches data, either incoming or outgoing, as directed by control logic 116 to temporarily store data while the array of memory cells 104 is busy writing or reading, respectively, other data. During a program operation (e.g., write operation), data is passed from the cache register 118 to data register 120 for transfer to the array of memory cells 104; then new data is latched in the cache register 118 from the I/O control circuitry 112. During a read operation, data is passed from the cache register 118 to the I/O control circuitry 112 for output to the external processor 130; then new data is passed from the data register 120 to the cache register 118. A status register 122 is in communication with I/O control circuitry 112 and control logic 116 to latch the status information for output to the processor 130.

[0018] Memory device 100 receives control signals at control logic 116 from processor 130 over a control link 132. The control signals might include a chip enable CE#, a command latch enable CLE, an address latch enable ALE, a write enable WE#, a read enable RE#, and a write protect WP#. Additional or alternative control signals (not shown) may be further received over control link 132 depending upon the nature of the memory device 100. Memory device 100 receives command signals (which represent commands), address signals (which represent

addresses), and data signals (which represent data) from processor 130 over a multiplexed input/output (I/O) bus 134 and outputs data to processor 130 over I/O bus 134.

[0019] For example, the commands are received over input/output (I/O) pins [7:0] of I/O bus 134 at I/O control circuitry 112 and are written into command register 124. The addresses are received over input/output (I/O) pins [7:0] of I/O bus 134 at I/O control circuitry 112 and are written into address register 114. The data are received over input/output (I/O) pins [7:0] for an 8-bit device or input/output (I/O) pins [15:0] for a 16-bit device at I/O control circuitry 112 and are written into cache register 118. The data are subsequently written into data register 120 for programming the array of memory cells 104. For another embodiment, cache register 118 may be omitted, and the data are written directly into data register 120. Data are also output over input/output (I/O) pins [7:0] for an 8-bit device or input/output (I/O) pins [15:0] for a 16-bit device.

[0020] Memory device 100 may be configured to receive a supply voltage V_{cc} and a reference potential (e.g., ground or 0V) V_{ss} . The supply voltage V_{cc} may represent a lowest positive supply voltage received by the memory device 100 relative to a voltage level of the reference potential V_{ss} .

[0021] It will be appreciated by those skilled in the art that additional circuitry and signals can be provided, and that the memory device 100 of Figure 1 has been simplified. It should be recognized that the functionality of the various block components described with reference to Figure 1 may not necessarily be segregated to distinct components or component portions of an integrated circuit device. For example, a single component or component portion of an integrated circuit device could be adapted to perform the functionality of more than one block component of Figure 1. Alternatively, one or more components or component portions of an integrated circuit device could be combined to perform the functionality of a single block component of Figure 1.

[0022] Additionally, while specific I/O pins are described in accordance with popular conventions for receipt and output of the various signals, it is noted that other combinations or numbers of I/O pins may be used in the various embodiments.

[0023] Figure 2A is a schematic of a portion of an array of memory cells 200A as could be used in a memory of the type described with reference to Figure 1, e.g., as a portion of array of

memory cells 104. Memory array 200A includes access lines, such as word lines 202₀ to 202_N, and a data line, such as bit line 204. The word lines 202 may be connected to global access lines (e.g., global word lines), not shown in Figure 2A, in a many-to-one relationship. For some embodiments, memory array 200A may be formed over a semiconductor that, for example, may be conductively doped to have a conductivity type, such as a p-type conductivity, e.g., to form a p-well, or an n-type conductivity, e.g., to form an n-well.

[0024] Memory array 200A might be arranged in rows (each corresponding to a word line 202) and columns (each corresponding to a bit line 204). Each column may include a string of series-connected memory cells, such as one of NAND strings 206₀ to 206_M. Each NAND string 206 might be connected (e.g., selectively connected) to a common source 216 and might include memory cells 208₀ to 208_N. The memory cells 208 may represent non-volatile memory cells for storage of data. The memory cells 208 of each NAND string 206 might be connected in series between a select gate 210 (e.g., a field-effect transistor), such as one of the select gates 210₀ to 210_M (e.g., that may be source select transistors, commonly referred to as select gate source), and a select gate 212 (e.g., a field-effect transistor), such as one of the select gates 212₀ to 212_M (e.g., that may be drain select transistors, commonly referred to as select gate drain). Select gates 210₀ to 210_M might be commonly connected to a select line 214, such as a source select line, and select gates 212₀ to 212_M might be commonly connected to a select line 215, such as a drain select line. Although depicted as traditional field-effect transistors, the select gates 210 and 212 may utilize a structure similar to (e.g., the same as) the memory cells 208. The select gates 210 and 212 might represent a plurality of select gates connected in series, with each select gate in series configured to receive a same or independent control signal.

[0025] A source of each select gate 210 might be connected to common source 216. The drain of each select gate 210 might be connected to a memory cell 208₀ of the corresponding NAND string 206. For example, the drain of select gate 210₀ might be connected to memory cell 208₀ of the corresponding NAND string 206₀. Therefore, each select gate 210 might be configured to selectively connect a corresponding NAND string 206 to common source 216. A control gate of each select gate 210 might be connected to select line 214.

[0026] The drain of each select gate 212 might be connected to the bit line 204 for the corresponding NAND string 206. For example, the drain of select gate 212₀ might be connected

to the bit line 204₀ for the corresponding NAND string 206₀. The source of each select gate 212 might be connected to a memory cell 208_N of the corresponding NAND string 206. For example, the source of select gate 212₀ might be connected to memory cell 208_N of the corresponding NAND string 206₀. Therefore, each select gate 212 might be configured to selectively connect a corresponding NAND string 206 to the common bit line 204. A control gate of each select gate 212 might be connected to select line 215.

[0027] The memory array in Figure 2A might be a three-dimensional memory array, e.g., where NAND strings 206 may extend substantially perpendicular to a plane containing the common source 216 and to a plane containing a plurality of bit lines 204 that may be substantially parallel to the plane containing the common source 216.

[0028] Typical construction of memory cells 208 includes a data-storage structure 234 (e.g., a floating gate, charge trap, etc.) that can determine a data state of the memory cell (e.g., through changes in threshold voltage), and a control gate 236, as shown in Figure 2A. The data-storage structure 234 may include both conductive and dielectric structures while the control gate 236 is generally formed of one or more conductive materials. In some cases, memory cells 208 may further have a defined source 230 and a defined drain 232. Memory cells 208 have their control gates 236 connected to (and in some cases form) a word line 202.

[0029] A column of the memory cells 208 may be a NAND string 206 or a plurality of NAND strings 206 selectively connected to a given bit line 204. A row of the memory cells 208 may be memory cells 208 commonly connected to a given word line 202. A row of memory cells 208 can, but need not, include all memory cells 208 commonly connected to a given word line 202. Rows of memory cells 208 may often be divided into one or more groups of physical pages of memory cells 208, and physical pages of memory cells 208 often include every other memory cell 208 commonly connected to a given word line 202. For example, memory cells 208 commonly connected to word line 202_N and selectively connected to even bit lines 204 (e.g., bit lines 204₀, 204₂, 204₄, etc.) may be one physical page of memory cells 208 (e.g., even memory cells) while memory cells 208 commonly connected to word line 202_N and selectively connected to odd bit lines 204 (e.g., bit lines 204₁, 204₃, 204₅, etc.) may be another physical page of memory cells 208 (e.g., odd memory cells). Although bit lines 204₃-204₅ are not explicitly depicted in Figure 2A, it is apparent from the figure that the bit lines 204 of the array of memory

cells 200A may be numbered consecutively from bit line 204_0 to bit line 204_M . Other groupings of memory cells 208 commonly connected to a given word line 202 may also define a physical page of memory cells 208. For certain memory devices, all memory cells commonly connected to a given word line might be deemed a physical page of memory cells. The portion of a physical page of memory cells (which, in some embodiments, could still be the entire row) that is read during a single read operation or programmed during a single programming operation (e.g., an upper or lower page of memory cells) might be deemed a logical page of memory cells. A block of memory cells may include those memory cells that are configured to be erased together, such as all memory cells connected to word lines 202_0 - 202_N (e.g., all NAND strings 206 sharing common word lines 202). Unless expressly distinguished, a reference to a page of memory cells herein refers to the memory cells of a logical page of memory cells.

[0030] Memory devices may be configured to operate using more than one (e.g., two) nominal levels of the supply voltage V_{cc} . For example, a memory device might be configured to operate using either a V_{cc} having a nominal level of 1.8V (e.g., corresponding to a range of 1.65V-1.95V) or a V_{cc} having a nominal level of 3.3V (e.g., corresponding to a range of 2.7V-3.6V). In some cases, a memory device configured to operate using one of multiple nominal levels of the supply voltage V_{cc} might further be configured to generate an internal voltage supply having a voltage level corresponding to (e.g., equal to) a voltage level within the range of acceptable values corresponding to a particular nominal level, e.g., corresponding to the higher (e.g., highest) nominal level, such that operation of certain devices can remain relatively uniform regardless of which of the acceptable ranges of supply voltage V_{cc} is presently connected to that memory device. For example, during a sensing operation (e.g., a read operation) on a string of series-connected memory cells, e.g., NAND string 206_0 , the select gates 210_0 and 212_0 might be configured to each receive a select gate voltage (e.g., V_{sg}) having a particular voltage level regardless of the voltage level of the power supply V_{cc} . Generation of different voltage levels for internal use by the memory device is well understood such as through the use of a voltage generator, e.g., a charge pump.

[0031] Figure 2B is another schematic of a portion of an array of memory cells 200B as could be used in a memory of the type described with reference to Figure 1, e.g., as a portion of array of memory cells 104. Like numbered elements in Figure 2B correspond to the description as provided with respect to Figure 2A. Figure 2B provides additional detail of one example of a

three-dimensional NAND memory array structure. The three-dimensional NAND memory array 200B may incorporate vertical structures which may include semiconductor pillars where a portion of a pillar may act as a channel region of the memory cells of NAND strings 206. The NAND strings 206 may be each selectively connected to a bit line 204_0 - 204_M by a select transistor 212 (e.g., that may be drain select transistors, commonly referred to as select gate drain) and to a common source 216 by a select transistor 210 (e.g., that may be source select transistors, commonly referred to as select gate source). Multiple NAND strings 206 might be selectively connected to the same bit line 204. Subsets of NAND strings 206 can be connected to their respective bit lines 204 by biasing the select lines 215_0 - 215_L to selectively activate particular select transistors 212 each between a NAND string 206 and a bit line 204. The select transistors 210 can be activated by biasing the select line 214. Each word line 202 may be connected to multiple rows of memory cells of the memory array 200B. Rows of memory cells that are commonly connected to each other by a particular word line 202 may collectively be referred to as tiers.

[0032] In prior art erase operations, the large magnitude (e.g., absolute value) of the erase voltages (e.g., 25V) applied to the data lines and source is stressful, which can lead to reliability concerns in the periphery circuitry of a memory. Such erase voltages typically require the use of high-voltage isolation techniques and high-voltage switching to decode and supply the desired voltage levels to a block of memory cells selected for erasure without adversely affecting unselected blocks of memory cells. This can lead to increased size of the periphery circuitry, e.g., decode circuitry and its drivers. Various embodiments seek to mitigate these issues by reducing the magnitude of the erase voltages applied to the data lines and source.

[0033] Figure 3 is a cross-sectional view of a portion of an array of memory cells 300 as could be used in a memory of the type described with reference to Figure 1, e.g., as a portion of array of memory cells 104. Like numbered elements in Figure 3 correspond to the description as provided with respect to Figure 2A. Similar to Figure 2A, the array of memory cells 300 depicts N access lines, e.g., word lines 202. A memory cell (not depicted in Figure 3) might be formed at each intersection of an word line 202 and a pillar 340 (e.g., pillars 340_0 - 340_M) of semiconductor material. The pillars 340 may form channels for the memory cells and select gates.

[0034] Figure 3 depicts that the array of memory cells 300 might utilize more than one select gate at each end of a string of series-connected memory cells, controlled by select lines 214 (e.g., 214₀ and 214₁) and select lines 215 (e.g., 215_{0y}, 215_{1y} and 215_{2y}, where y = 0 to M). In this example, a select gate (e.g., source select transistor) might be formed at the intersection of the select line 214₀ and the pillar 340₀, and another select gate (e.g., source select transistor) might be formed at the intersection of the select line 214₁ and the pillar 340₀. Similarly, a select gate (e.g., drain select transistor) might be formed at the intersection of the select line 215₀₀ and the pillar 340₀, another select gate (e.g., drain select transistor) might be formed at the intersection of the select line 215₁₀ and the pillar 340₀, and still another select gate (e.g., drain select transistor) might be formed at the intersection of the select line 215₂₀ and the pillar 340₀. Remaining pillars 340 may provide similar structure in their intersections with select lines 214 and 215. Each pillar 340 may be connected to the data line, e.g., bit line 204, through a contact 342, and further connected to the source 216.

[0035] Memory cells formed at intersections of the word lines 202 and the pillars 340 might be operated to store data at different densities, e.g., storing differing numbers of bits per memory cell. The number of bits might be some value zero or greater, either integer or fractional. For example, memory cells formed at the intersections of word lines 202₀ and 202_N with the pillars 340 might be operated to store data at a first density. The first density might be zero bits per memory cell, e.g., dummy memory cells that are not operated to store user data. Memory cells formed at the intersections of word lines 202₁ and 202_{N-1} might be operated to store data at a second density greater than or equal to the first density. For example, the second density might be one bit per memory cell. Memory cells formed at the intersections of word lines 202₂ and 202_{N-2} might be operated to store data at a third density greater than or equal to the second density. For example, the third density might be two bits per memory cell. And memory cells formed at the intersections of word lines 202₃ through 202_{N-3} might be operated to store data at a fourth density greater than or equal to the third density. For example, the fourth density might be three bits per memory cell.

[0036] As referenced with respect to Figure 2A, local access lines, e.g., word lines 202, may be connected to global access lines in a many-to-one relationship. Figure 4A is a schematic of a portion of an array of memory cells as could be used in a memory device of the type described

with reference to Figure 1 and depicting this many-to-one relationship between local access lines (e.g., word lines 202) and global access lines (e.g., global word lines 402).

[0037] As depicted in Figure 4A, a plurality of blocks of memory cells 458 may have their local access lines (e.g., word lines 202) commonly selectively connected to a plurality of global access lines (e.g., global word lines 402). A block of memory cells 458 may include a plurality of NAND strings 206 commonly coupled to a particular set of word lines 202. For example, the NAND strings 206₀-206_M of Figure 2A, or some portion thereof, may represent a block of memory cells 458. Although Figure 4A depicts only blocks of memory cells 458₀ and 458₁ (Block 0 and Block 1), additional blocks of memory cells 458 may have their word lines 202 commonly connected to global word lines 402 in a like manner. Similarly, although Figure 4A depicts only four word lines 202, blocks of memory cells 458 may include fewer or more word lines 202. In applying the structure of Figure 4A to the array structure of Figure 3, it is clear that there would be N global word lines 402, i.e., GWL 402₀ to 402_N.

[0038] To facilitate memory access operations to specific blocks of memory cells 458 commonly coupled to a given set of global word lines 402, each block of memory cells 458 may have a corresponding set of block select transistors 454 in a one-to-one relationship with their word lines 202. Control gates of the set of block select transistors 454 for a given block of memory cells 458 may have their control gates commonly connected to a corresponding block select line 456. For example, for block of memory cells 458₀, word line 202₀₀ may be selectively connected to global word line 402₀ through block select transistor 454₀₀, word line 202₀₁ may be selectively connected to global word line 402₁ through block select transistor 454₀₁, word line 202₀₂ may be selectively connected to global word line 402₂ through block select transistor 454₀₂, and word line 202₀₃ may be selectively connected to global word line 402₃ through block select transistor 454₀₃, while block select transistors 454₀₀-454₀₃ are responsive to a control signal received on block select line 456₀.

[0039] Block select transistors may be high-voltage devices, i.e., configured to switch voltage levels in excess of the voltage level of the select gate voltage V_{sg}, e.g., voltage levels in excess of two times the voltage level of the select gate voltage V_{sg}. Such switching devices may require increased isolation. Figure 4B is a cross-sectional view of a block select transistor 454, having a control gate 468 and source/drain regions 466, wherein the control gate 468 is

connected to a block select line 456. The block select transistor 454 may be formed in first well of semiconductor material 464, The first well of semiconductor material may be separated from a semiconductor substrate 460 by a second well (e.g., deep well) of semiconductor material 462. The semiconductor substrate 460, as well as the first well of semiconductor material 464, may have a first conductivity type, e.g., a p-type conductivity. The second well of semiconductor material 462, as well as the source/drain regions 466, may have a second conductivity type different than (e.g., opposite) the first conductivity type, e.g., the second well of semiconductor material may have an n-type conductivity. This structure is commonly referred to as a triple-well construction and may be used to provide isolation of high-magnitude and/or negative voltage levels applied to the global word line 402 during access operations. For a selected block of memory cells 458, e.g., selected for an erase operation, the block select line 456 might be connected to receive a pass voltage V_{pass} sufficient to pass the voltage level of the global word line 402 to the local word line 202, which might be the reference potential or 0V, for example. For the unselected blocks of memory cells 458, the block select line 456 might be connected to receive a voltage level sufficient to inhibit current flow, allowing the local word line 202 to electrically float. For example, the block select line 456 of an unselected block might be connected to receive a voltage level substantially equal to (e.g., equal to) the voltage level of the global word line 402 having the most negative voltage level.

[0040] In erasing memory cells, e.g., a string of series-connected memory cells or a block of memory cells containing a number of strings of series-connected memory cells, various voltage levels may be applied to various nodes described with reference to Figures 2A, 2B, 3, and 4A. As noted previously, various embodiments facilitate a reduction in magnitude of the voltage levels applied to the data line and source during an erase operation. By increasing the magnitude of voltage levels applied to access lines during the erase operation, the magnitude applied to the data line and source can be reduced. This reduction in magnitude of voltage levels applied to the data line and source may facilitate easing of design rules for isolation of such structures, e.g., may facilitate a reduction in isolation requirements. Furthermore, as access lines are typically subjected to high-magnitude voltages during programming operations, it may be possible to perform erase operations in accordance with embodiments without altering design rules for the isolation of the access lines. This can lead to a reduction in size of the periphery circuitry.

Table 1 provides two examples of voltage levels applied to various nodes during an erase operation.

[0041]

Table 1

Node \ Voltage	Example 1	Example 2
BL 204	3V	10V
SGD2 215 _{2y}	0V	7V
SGD1 215 _{1y}	-2V	5V
SGD0 215 _{0y}	-2V	5V
WLN 202 _N	-12V	-5V
WLN-1 202 _{N-1}	-19V	-12V
WLN-2 202 _{N-2}	-19V	-12V
WLN-3 202 _{N-3}	-22V	-15V
WL _x +1 202 _{x+1}	-22V	-15V
WL _x 202 _x	-22V	-15V
WL _x -1 202 _{x-1}	-22V	-15V
WL3 202 ₃	-22V	-15V
WL2 202 ₂	-19V	-12V
WL1 202 ₁	-19V	-12V
WL0 202 ₀	-12V	-5V
SGS1 214 ₁	-2V	5V
SGS0 214 ₀	0V	7V
SRC 216	3V	10V
GWL 402 ₀ and 402 _N	-12V	-5V
GWL 402 ₁ , 402 ₂ , 402 _{N-2} , and 402 _{N-1}	-19V	-12V
GWL 402 ₃ to 402 _{N-3}	-22V	-15V
BSL 456 (selected)	0V	0V
BSL 456 (unselected)	-22V	-15V

[0042] In general, during an erase operation, voltage levels applied to some portion of the word lines 202, e.g., word lines 202₃ through 202_{N-3}, might have a magnitude greater than the magnitude of the voltage levels applied to the bit line 204 and the source 216. For some embodiments, the voltage levels applied to the bit line 204 and the source 216 are substantially the same (e.g., the same or intended to be the same). Voltage levels applied to another portion of the word lines 202, e.g., word lines 202₁, 202₂, 202_{N-2} and 202_{N-1}, might have a magnitude less than the magnitude of the voltage levels applied to the word lines 202₃ through 202_{N-3}. Voltage levels applied to still another portion of the word lines 202, e.g., word lines 202₀ and 202_N, might have a magnitude less than the magnitude of the voltage levels applied to the word lines 202₁, 202₂, 202_{N-2} and 202_{N-1}. Voltage levels applied to some portion of the select lines, e.g., select lines 214₁, 215_{0y} and 215_{1y}, might be selected to induce gate induced drain leakage (GIDL) in order to raise the voltage level of the pillars 340 during the erase operation, and thus might have fixed ΔV with respect to the voltage level applied to the source 216 and data line 204, respectively. For example, the voltage levels applied to the select line 214₁ might be 5V less than the voltage level applied to the source 216, and the voltage levels applied to the select lines 215_{0y} and 215_{1y} might be 5V less than the voltage level applied to the data line 204. Voltage levels applied to another portion of the select lines, e.g., select lines 214₁ and 215_{2y}, might be selected to reduce stress during the erase operation, and thus might have some value between the voltage level applied to an adjacent select line, e.g., select line 214₀ or 215_{1y}, respectively, and the voltage level applied to the data line 204 or source 216, respectively.

[0043] Figure 5A is a flowchart of a method of operating a memory. For example, Figure 5A may represent a portion of an erase operation. At 570, a first voltage level may be applied to a source (e.g., source 216 of Figure 3) connected to a first end of a string of series-connected memory cells. The source may further be connected to additional strings of series-connected memory cells. For example, the source may be connected to the strings of memory cells of a block of memory cells. At 572, a second voltage level may be applied to a data line (e.g., bit line 204 of Figure 3) connected to a second end (e.g., opposite end) of the sting of memory cells. Similarly, the data line may be connected to additional strings of series-connected memory cells. For some embodiments, the first voltage level and the second voltage level are the same voltage level. For some embodiments, the first voltage level and the second voltage level are each less than or equal to V_{cc} or V_{sg} .

[0044] At 574, a third voltage level is applied to a first access line coupled to a first memory cell of the string of series connected memory cells. The first access line may further be coupled to corresponding memory cells of additional strings of series-connected memory cells. For example, the first access line might be any one of the word lines 202_3 through 202_{N-3} of Figure 3. The third voltage level has a magnitude greater than the magnitude of the first voltage level and greater than the magnitude of the second voltage level. The third voltage level further has a polarity (e.g., negative polarity) and magnitude that are expected to decrease a threshold voltage of the first memory cell when applied concurrently with the first voltage level to the data line and the second voltage level to the source. As used herein, a first act and a second act occur concurrently when the first act occurs simultaneously with the second act for at least a portion of a duration of the second act. For example, for at least a portion of the time of applying the third voltage level to the first access line, the first voltage level, the second voltage level and the third voltage level are being applied simultaneously to their respective, data line, source or first access line.

[0045] Optionally, at 576, a fourth voltage level is applied to a second access line coupled to a second memory cell of the string of series connected memory cells. The second access line may further be coupled to corresponding memory cells of additional strings of series-connected memory cells. For example, the second access line might be any one of the word lines 202_1 , 202_2 , 202_{N-2} and 202_{N-1} of Figure 3. The fourth voltage level has a magnitude less than the magnitude of the third voltage level. The fourth voltage level further has a polarity (e.g., negative polarity) and magnitude that are expected to decrease a threshold voltage of the second memory cell when applied concurrently with the first voltage level to the data line and the second voltage level to the source. The fourth voltage level might be applied to the second access line concurrently with applying the third voltage level to the first access line.

[0046] Optionally, at 578, a fifth voltage level is applied to a third access line coupled to a third memory cell of the string of series connected memory cells. The third access line may further be coupled to corresponding memory cells of additional strings of series-connected memory cells. For example, the third access line might be any one of the word lines 202_0 and 202_N of Figure 3. The fifth voltage level has a magnitude less than the magnitude of the fourth voltage level. The fifth voltage level further has a polarity (e.g., negative polarity) and magnitude that are expected to decrease a threshold voltage of the third memory cell when

applied concurrently with the first voltage level to the data line and the second voltage level to the source. The fifth voltage level might be applied to the third access line concurrently with applying the third voltage level to the first access line, and concurrently with applying the fourth voltage level to the second access line.

[0047] The method of Figure 5A might represent one cycle of an erase operation. For example, the erase operation may include a number of cycles of applying voltage levels to reduce the respective threshold voltages of one or more memory cells, and verifying whether those memory cells have reached a desired threshold voltage. Figure 5B is a flowchart of a method of operating a memory device facilitating such an erase operation.

[0048] Reference numbers 570, 572 and 574 of Figure 5B might correspond to the description as provided with reference to Figure 5A. After applying the third voltage level to the first access line at 574, which might be referred to as an erase pulse, a decision might be made at 580 whether the first memory cell is deemed to have a desired threshold voltage. The determination does not require that the first memory cell have the desired threshold voltage. For example, determining whether the first memory cell is deemed to have a desired threshold voltage may include applying an erase verify voltage to the word lines 202 of the string of series-connected memory cells, wherein the erase verify voltage might be expected to activate any memory cell of the string of series-connected memory cells having a threshold voltage less than or equal to the desired threshold voltage, and determining if there is current flow through the string of series-connected memory cells.

[0049] If the first memory cell is deemed to have the desired threshold voltage at 580, the method might end at 582. If the first memory cell is not deemed to have the desired threshold voltage at 580, a decision might optionally be made at 584 whether the third voltage level is deemed to have a particular value. The particular value may represent a maximum magnitude for the erase operation. For example, the particular value might correspond to a voltage level of -22V for Example 1 of Table 1 or -15V for Example 2 of Table 1. Determining whether the third voltage level is deemed to have the particular value might include counting a number of times an erase pulse has been applied at 574.

[0050] If the third voltage level is deemed to have the particular value at 584, the method might indicate a failure of the erase operation at 586. If the third voltage level is not deemed to

have the particular value at 584 or otherwise, the magnitude of the third voltage level might be increased at 588 before returning to 570/572/574 to repeat the method for another cycle.

Increasing the magnitude of the third voltage level having a negative polarity might include decreasing the third voltage level. Decreasing the third voltage level might include decreasing the third voltage level by some ΔV (e.g., constant ΔV) for each cycle 570/572/574/580/584/588. For example, the third voltage level might be -20V for one cycle, -21V for a next subsequent cycle, and -22V for a still next subsequent cycle.

[0051] For embodiments applying the fourth voltage level at 576 in Figure 5A and/or applying the fifth voltage level at 578 in Figure 5A, the method of Figure 5B may further include the processes of 576 and 578 as well. Similar to Figure 5A, applying the first, second, third, fourth and fifth voltage levels may be concurrent.

CONCLUSION

[0052] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the embodiments will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the embodiments.

What is claimed is:

1. A method of operating a memory device, comprising:
applying a first voltage level to a source connected to a first end of a string of series-connected memory cells;
applying a second voltage level to a data line connected to a second end of the string of series-connected memory cells; and
applying a third voltage level to a first access line coupled to a first memory cell of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line;
wherein a magnitude of the third voltage level is greater than a magnitude of the first voltage level and greater than a magnitude of the second voltage level; and
wherein a polarity and the magnitude of the third voltage level are expected to decrease a threshold voltage of the first memory cell when concurrently applying the third voltage level to the first access line, the first voltage level to the source and the second voltage level to the data line.
2. The method of claim 1, wherein applying the first voltage level to the source and applying the second voltage level to the data line comprises applying a same voltage level to the source and to the data line.
3. The method of claim 1, wherein applying the first voltage level to the source and applying the second voltage level to the data line comprises applying voltage levels that are each less than or equal to a select gate voltage applied during a sensing operation on the string of series-connected memory cells.
4. The method of claim 1, wherein applying the first voltage level to the source and applying the second voltage level to the data line comprises applying voltage levels that are each less than or equal to a supply voltage V_{cc} of the memory device.

5. The method of claim 4, wherein applying the first voltage level to the source and applying the second voltage level to the data line comprises applying voltage levels that are each greater than or equal to a reference potential V_{ss} of the memory device.
6. The method of claim 1, further comprising:
applying a fourth voltage level to a second access line coupled to a second memory cell of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line;
wherein a magnitude of the fourth voltage level is less than the magnitude of the third voltage level; and
wherein a polarity and the magnitude of the fourth voltage level are expected to decrease a threshold voltage of the second memory cell when concurrently applying the fourth voltage level to the second access line, the first voltage level to the source and the second voltage level to the data line.
7. The method of claim 6, wherein the polarity of the third voltage level and the polarity of the fourth voltage level are each negative.
8. The method of claim 7, wherein a polarity of the first voltage level and a polarity of the second voltage level are each positive.
9. The method of claim 6, further comprising:
applying a fifth voltage level to a third access line coupled to a third memory cell of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line;
wherein a magnitude of the fifth voltage level is less than the magnitude of the fourth voltage level; and
wherein a polarity and the magnitude of the fifth voltage level are expected to decrease a threshold voltage of the third memory cell when concurrently applying the fifth voltage level to the third access line, the first voltage level to the source and the second voltage level to the data line.

10. The method of claim 9, wherein the polarity of the third voltage level, the polarity of the fourth voltage level, and the polarity of the fifth voltage level are each negative, and wherein a polarity of the first voltage level and a polarity of the second voltage level are each positive.
11. The method of claim 10, wherein the magnitude of the fifth voltage level is less than or equal to the magnitude of the first voltage level and less than or equal to the magnitude of the second voltage level.
12. The method of claim 9, wherein the magnitude of the first voltage level, the magnitude of the fourth voltage level and the magnitude of the fifth voltage level are each greater than the magnitude of the first voltage level and greater than the magnitude of the second voltage level.
13. A method of operating a memory device, comprising:
 - applying a first voltage level to a source connected to a first end of a string of series-connected memory cells;
 - applying a second voltage level to a data line connected to a second end of the string of series-connected memory cells;
 - applying a third voltage level to a first access line coupled to a first memory cell of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line; wherein a magnitude of the third voltage level is greater than a magnitude of the first voltage level and greater than a magnitude of the second voltage level;
 - and
 - wherein a polarity and the magnitude of the third voltage level are expected to decrease a threshold voltage of the first memory cell when concurrently applying the third voltage level to the first access line, the first voltage level to the source and the second voltage level to the data line;
 - determining whether the first memory cell is deemed to have a desired threshold voltage;

if the first memory cell is not deemed to have the desired threshold voltage, increasing the magnitude of the third voltage level before repeating applying the first voltage level to the source, applying the second voltage level to the data line and applying the third voltage level to the first access line.

14. The method of claim 13, wherein the string of series-connected memory cells is a first string of series-connected memory cells of a plurality of strings of memory cells, the method further comprising:
wherein applying the first voltage level to the source comprises applying the first voltage level to the source connected to a first end of each string of series-connected memory cells of the plurality of strings of series-connected memory cells;
wherein applying the second voltage level to the data line comprises applying the second voltage level to the data line connected to a second end of each string of series-connected memory cells of the plurality of strings of series-connected memory cells; and
wherein applying the third voltage level to the first access line comprises applying the third voltage level to the first access line coupled to a first memory cell of each string of series-connected memory cells of the plurality of strings of series-connected memory cells.
15. The method of claim 13, wherein applying the first voltage level to the source connected to the first end of the string of series-connected memory cells comprises applying the first voltage level to the source connected to a string of series-connected memory cells selected for an erase operation.
16. A method of operating a memory device, comprising:
applying a first voltage level to a source connected to a first end of a string of series-connected memory cells;
applying a second voltage level to a data line connected to a second end of the string of series-connected memory cells;

applying a third voltage level to a first plurality of access lines coupled to respective memory cells of a first plurality of memory cells of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line;

applying a fourth voltage level to a second plurality of access lines coupled to respective memory cells of a second plurality of memory cells of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line; and

applying a fifth voltage level to a third plurality of access lines coupled to respective memory cells of a third plurality of memory cells of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line;

wherein a magnitude of the third voltage level is greater than a magnitude of the first voltage level and greater than a magnitude of the second voltage level;

wherein a magnitude of the fourth voltage level is less than or equal to the magnitude of the third voltage level;

wherein a magnitude of the fifth voltage level is less than or equal to the magnitude of the fourth voltage level; and

wherein a polarity and the magnitude of the third voltage level are expected to decrease a threshold voltage of the first memory cell when concurrently applying the third voltage level to the first access line, the first voltage level to the source and the second voltage level to the data line.

17. The method of claim 16, wherein the first plurality of memory cells collectively comprise a first contiguous portion of the string of series-connected memory cells.
18. The method of claim 17, wherein the first contiguous portion of the string of series-connected memory cells is located in the string of series-connected memory cells between memory cells of the second plurality of memory cells, and wherein the first plurality of memory cells and the second plurality of memory cells collectively comprise a second contiguous portion of the string of series-connected memory cells.

19. The method of claim 18, wherein the second contiguous portion of the string of series-connected memory cells is located in the string of series-connected memory cells between memory cells of the third plurality of memory cells, and wherein the first plurality of memory cells, the second plurality of memory cells and the third plurality of memory cells collectively form the string of series-connected memory cells.
20. An apparatus, comprising:
an array of memory cells; and
a controller to perform access operations on the array of memory cells;
wherein the controller, during an erase operation on a string of series-connected memory cells selected for the erase operation, is configured to:
 apply a first voltage level to a source connected to a first end of the string of series-connected memory cells;
 apply a second voltage level to a data line connected to a second end of the string of series-connected memory cells; and
 apply a third voltage level to a first access line coupled to a first memory cell of the string of series-connected memory cells concurrently with applying the first voltage level to the source and applying the second voltage level to the data line;
wherein a magnitude of the third voltage level is greater than a magnitude of the first voltage level and greater than a magnitude of the second voltage level;
and
wherein a polarity and the magnitude of the third voltage level are expected to decrease a threshold voltage of the first memory cell when concurrently applying the third voltage level to the first access line, the first voltage level to the source and the second voltage level to the data line.

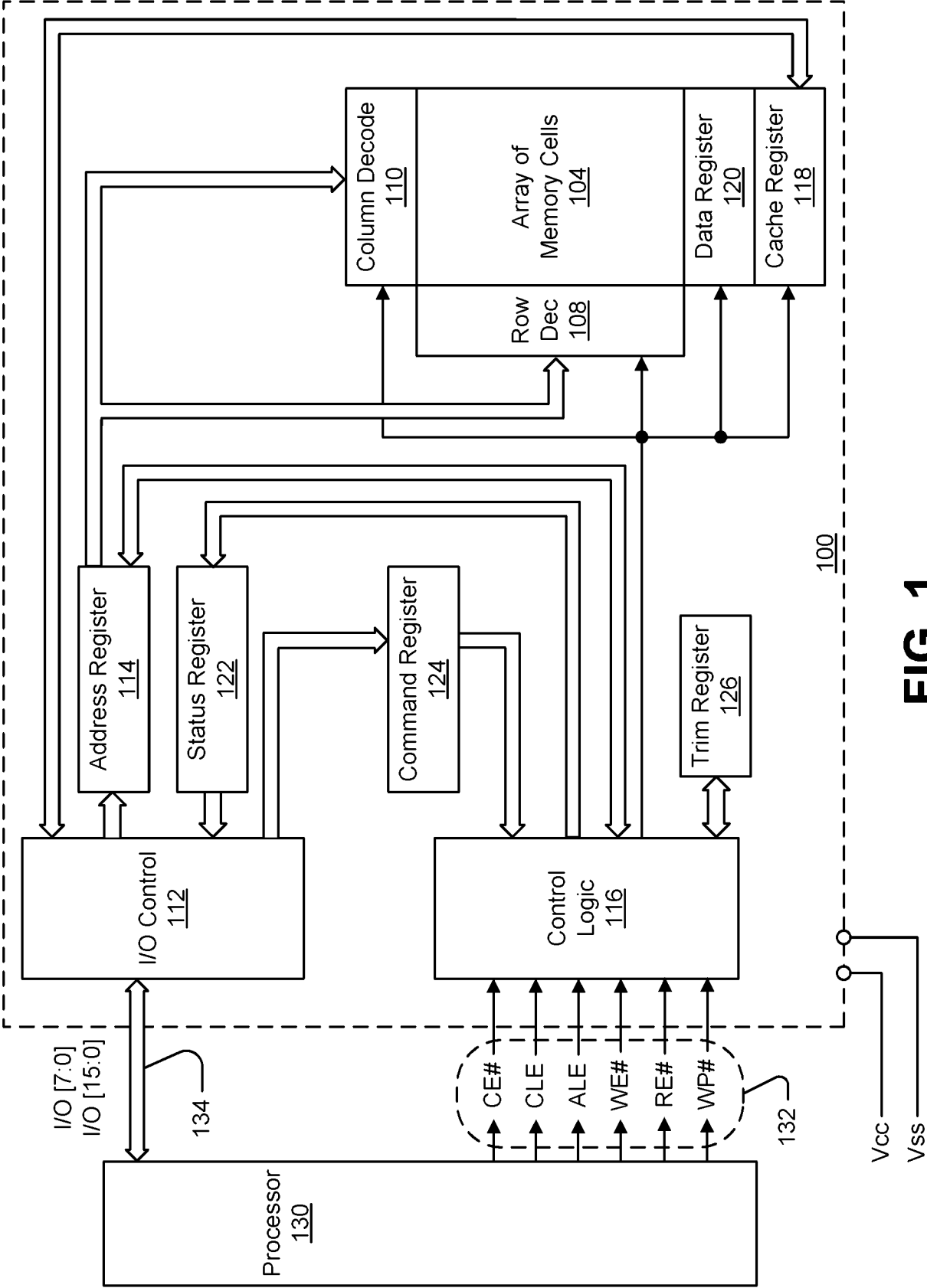
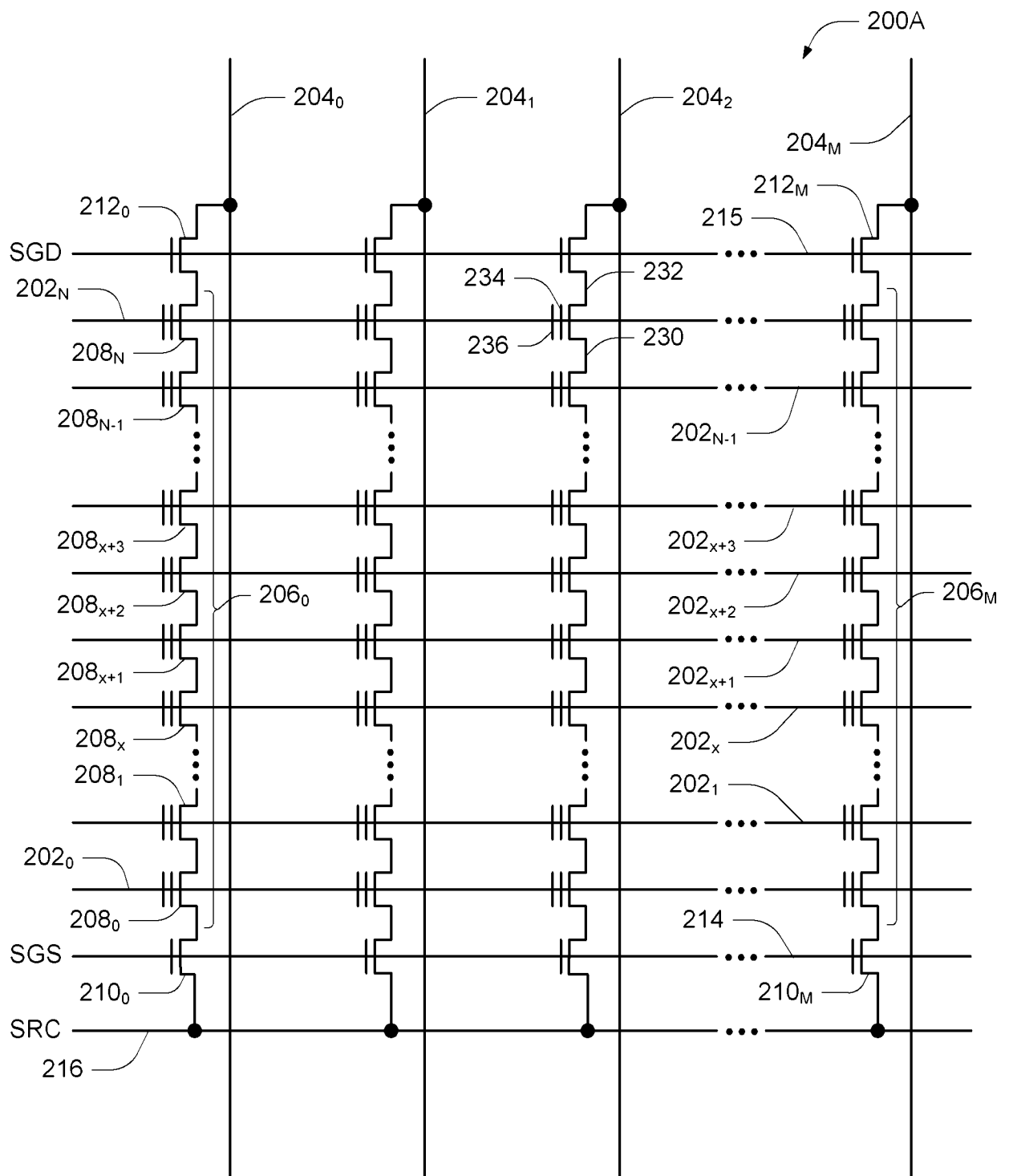


FIG. 1

**FIG. 2A**

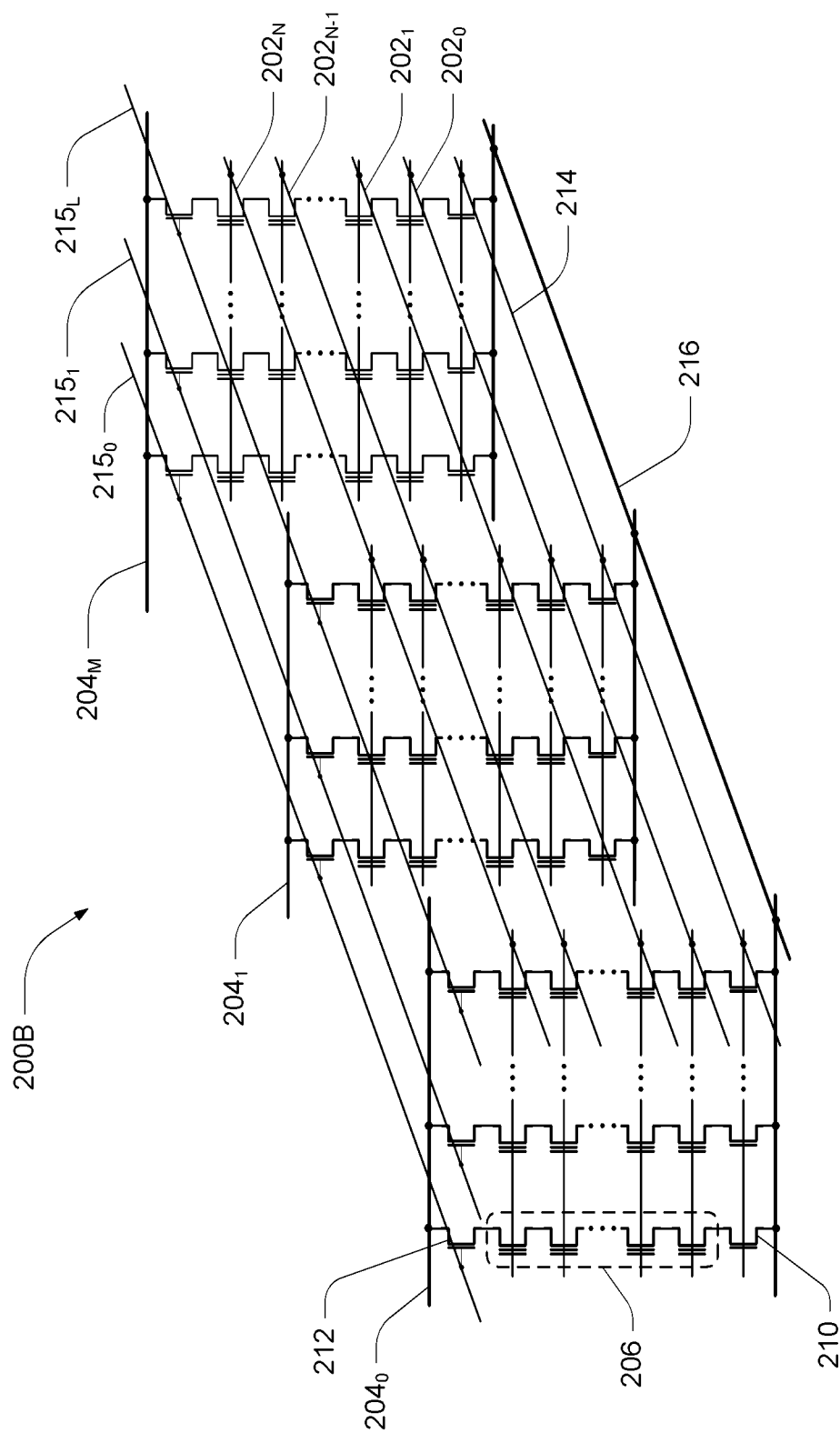


FIG. 2B

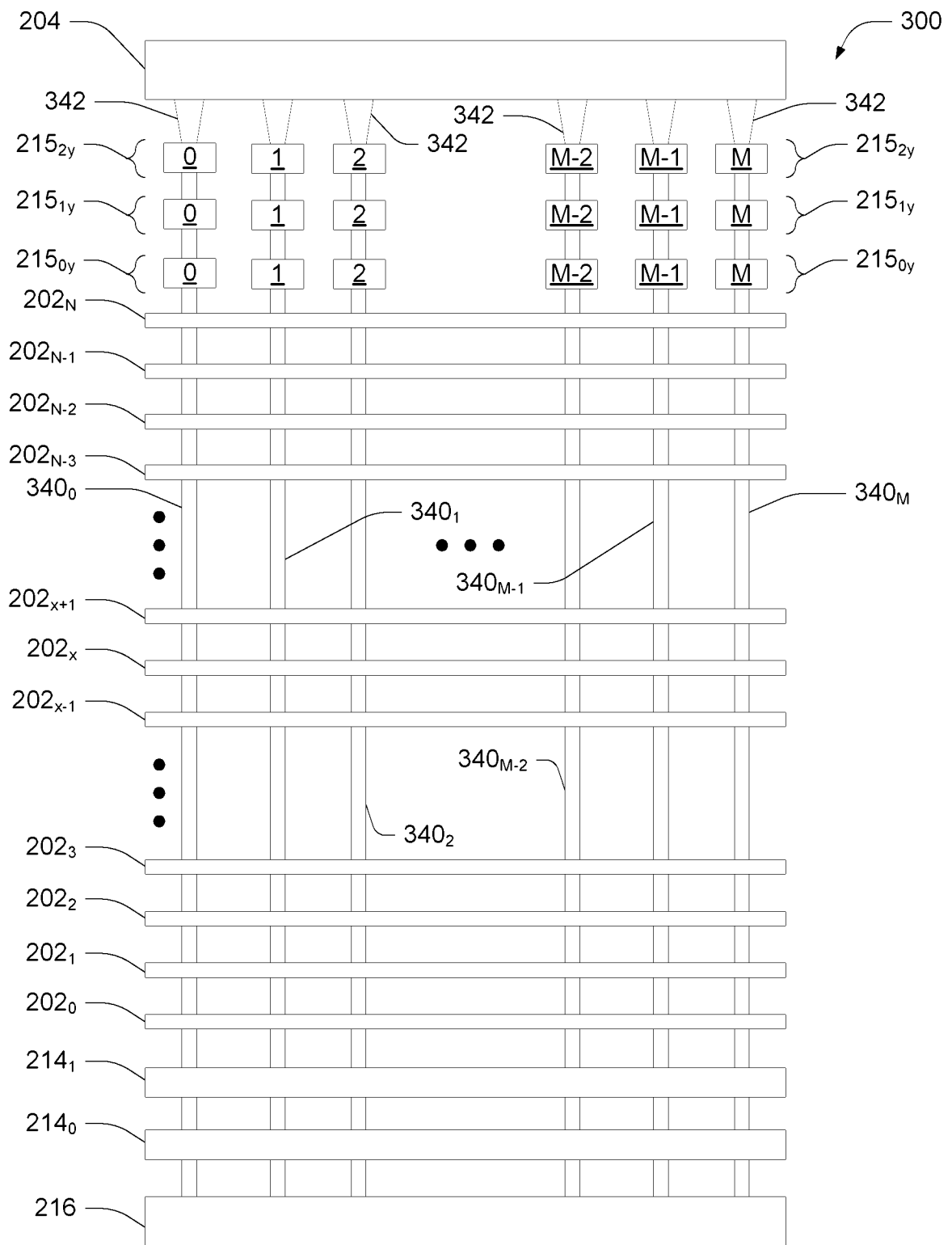


FIG. 3

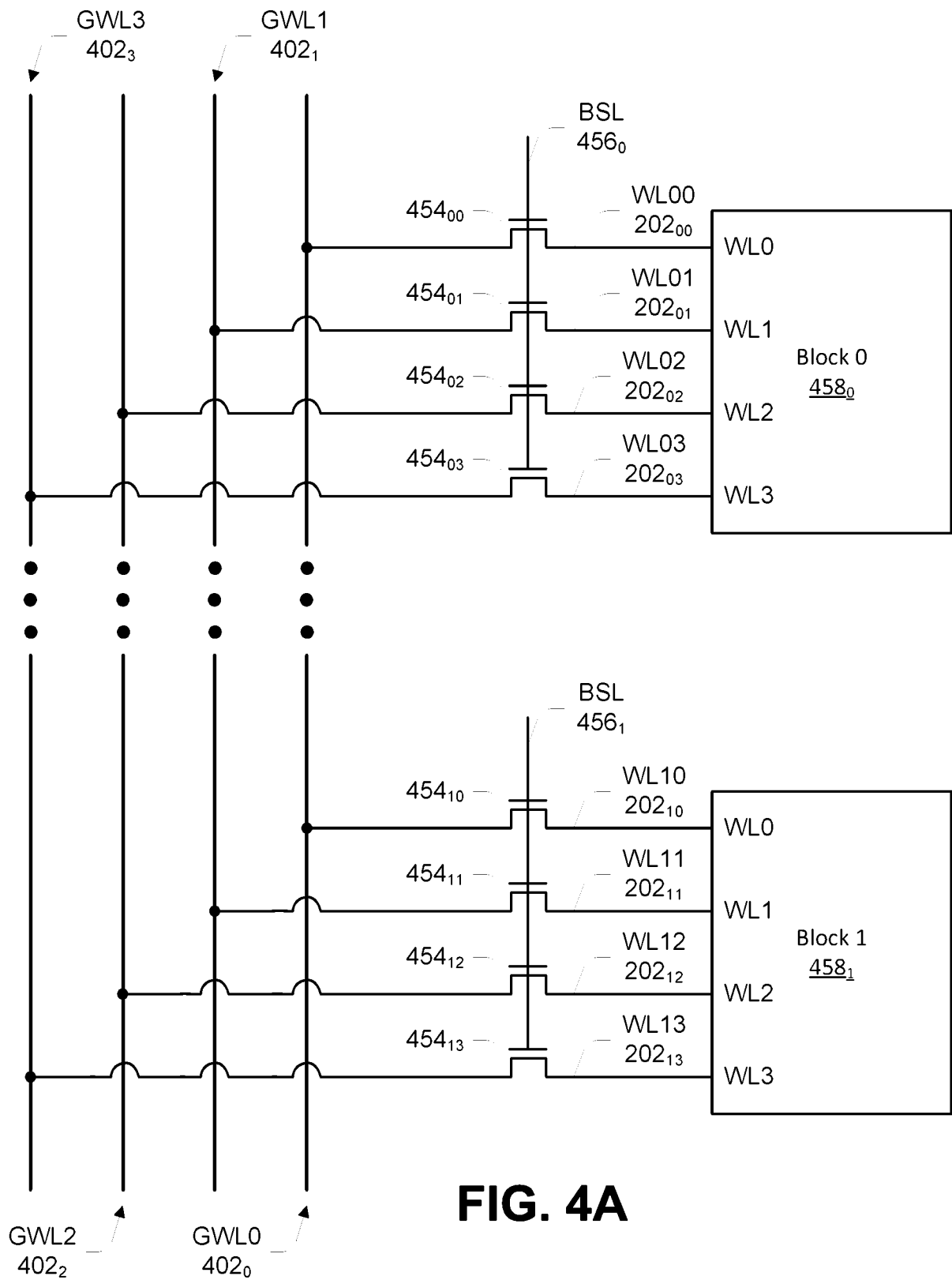


FIG. 4A

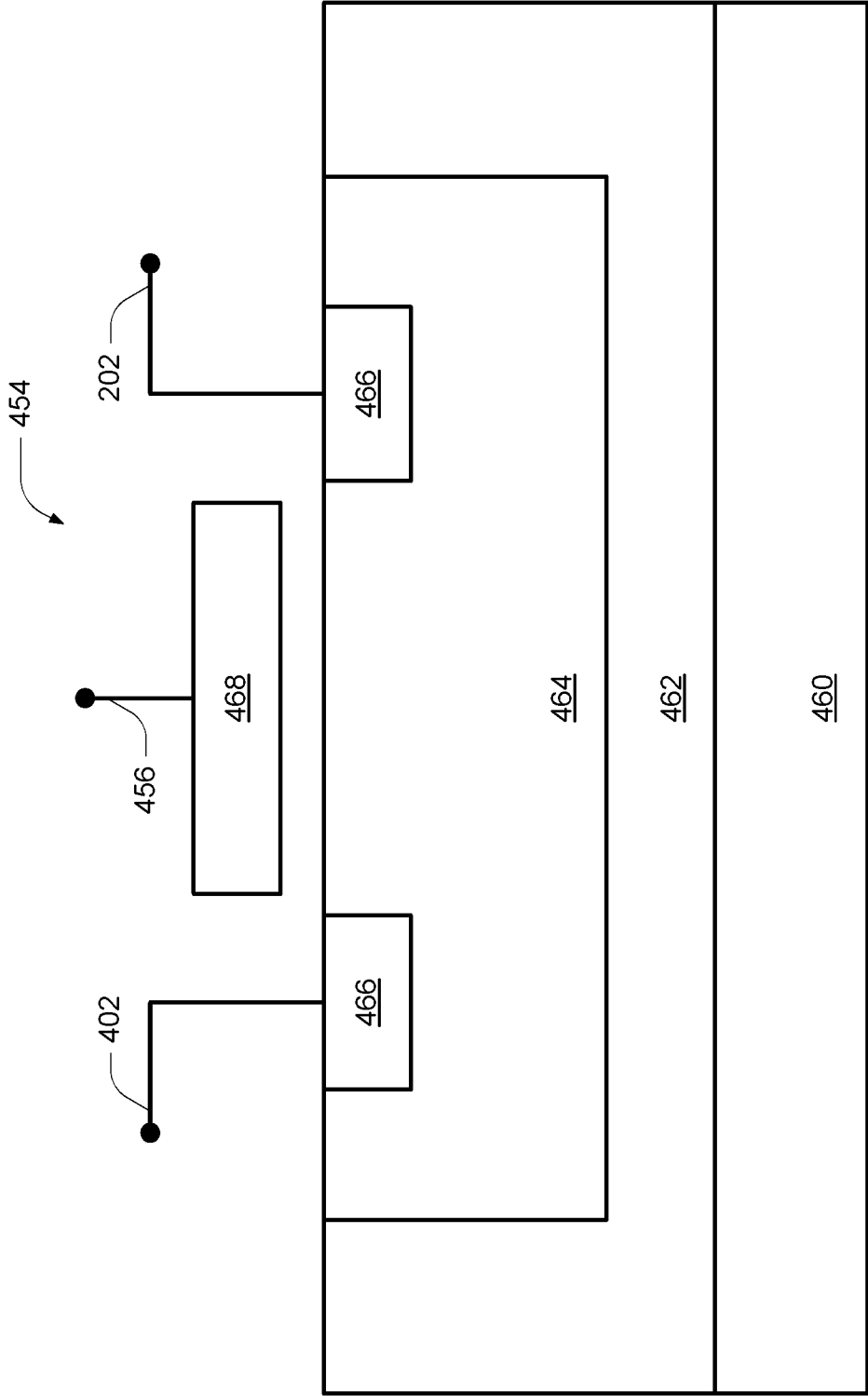
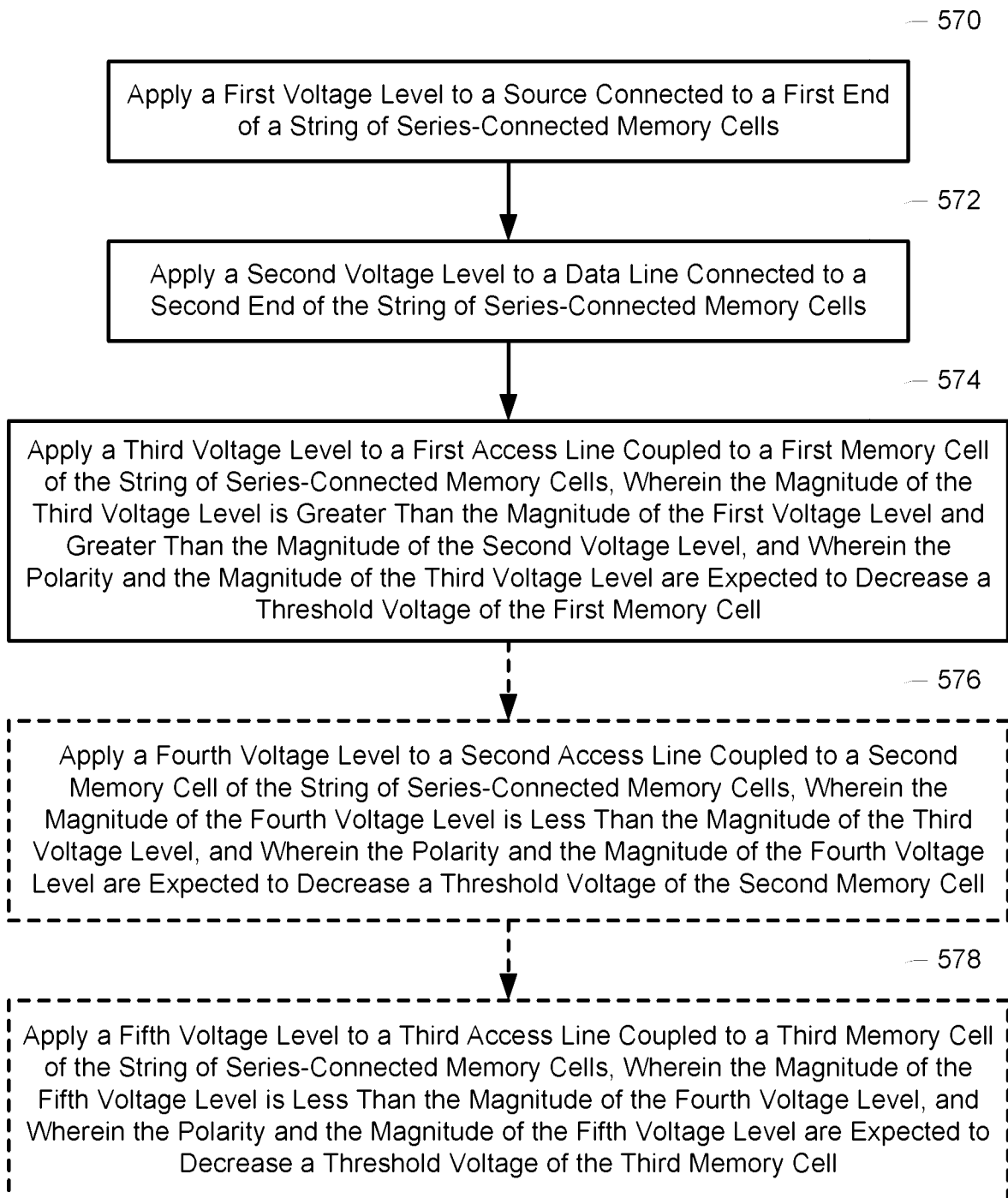
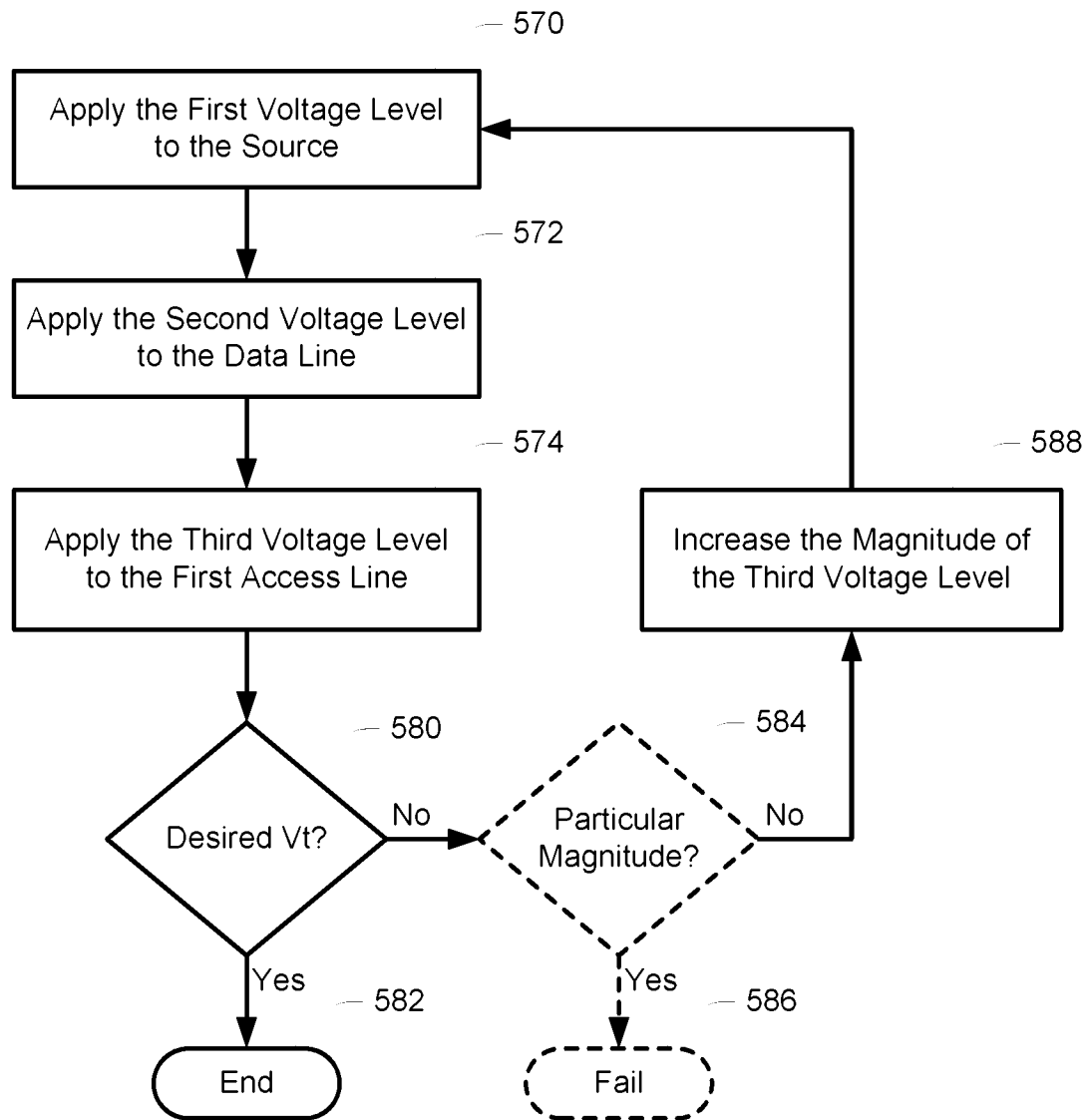


FIG. 4B

**FIG. 5A**

**FIG. 5B**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2016/103586

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/34(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, CNPAT, WPI, EPODOC: memory, cell, erase, data, line, bit, source, voltage, first, second, third, polarity, magnitude, level, decrease, threshold

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009244969 A1 (MAEJIMA, HIROSHI) 01 October 2009 (2009-10-01) claim 1, and figure 1	1-20
A	US 2010091566 A1 (KABUSHIKI KAISHA TOSHIBA) 15 April 2010 (2010-04-15) the whole document	1-20
A	US 2010124121 A1 (SEO, JI HYUN) 20 May 2010 (2010-05-20) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search

04 July 2017

Date of mailing of the international search report

26 July 2017

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2016/103586

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