MULTIPLEX CHARACTER GENERATOR

ABSTRACT: A display system including a symbol generator which consists of a group of segment generators. Each segment generator generates a portion of the symbol to be displayed in time sequence so that the segment generator which generates the first portion of the symbol will be free to generate the first portion of a following symbol or the first portion of a symbol on another display device while the other segment generators are generating the remainder of the first symbol. The outputs from this group of segment generators is transmitted through a group of multiplex gates which assemble the symbols into video data signals for a group of display devices.

The segmented character generator permits the generation of lower case characters, the generation of color symbols and words and expansion or reduction of display cluster sizes with high efficiency.


**FIG. 11**

**HEXADECIMAL REPRESENTATION OF VIDEO DATA - ROW 1 ODD**

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**HEXADECIMAL REPRESENTATION OF VIDEO DATA - ROW 1 EVEN**

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<td>DISPLAY 2</td>
<td>DISPLAY 3</td>
<td>DISPLAY 4</td>
<td>CHAR LINE BFR 2 TO CHARLINE BFR 1 GATE OPEN/CLOSE</td>
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</table>

**FIG. 16**
MULTIPLEX CHARACTER GENERATOR

CROSS-REFERENCE TO RELATED APPLICATIONS


BACKGROUND OF THE INVENTION

This invention relates to computer connected input/output systems and more particularly to systems for generating symbols for display on display devices in response to information signals from a central processor unit.

In the prior art, symbol generators have been described in which a group of display devices received inputs from a corresponding group of synchronous refresh storage devices such as delay lines or rotating magnetic disks. These synchronous storage devices received as inputs a stream of video information generated by a corresponding group of character generators wherein each character generator generated the complete character for one or possibly two display devices. The inputs to this group of character generators was in the form of parallel digital information usually from some form of temporary storage.

Systems of this nature require many character generators and many synchronous storage elements to generate information for presentation on a large cluster of display devices. Due to limitations of cost and size, systems of this nature were usually limited to a maximum of eight display devices per control unit.

Accordingly, it is an object of this invention to more efficiently generate symbols for presentation on a large cluster of input/output devices.

It is another object of this invention to generate symbols for a large cluster of input/output devices using a single segmented character generator.

Further, it is another object of this invention to generate both upper case and lower case symbols with common apparatus for presentation on input/output devices.

Another object of this invention is to generate graphic symbols for presentation on input/output devices.

Another object of this invention is to generate color information corresponding to each symbol generated.

In an alternate embodiment, it is another object of this invention to generate color information corresponding to each word of symbols generated.

It is a still further object of this invention to generate symbols for a wide-range of I/O device cluster sizes.

SUMMARY OF THE INVENTION

Accordingly, the invention comprises a system for information display which includes a central processing unit for transmitting information and receiving information from a group of input/output devices, a control unit connected to the central processor unit at one interface and to a group of input/output devices at a second interface for receiving the information to be displayed, storing the information to be displayed, and generating video signals representative of the information to be displayed.

The control unit comprises an interface control means for communicating with the processor unit, storage means for temporarily storing the information received from the processor unit, segment character generation means which includes a group of segment generators each of said segment generators being connected to one of a group of outputs of the storage means wherein each of said segment generators simultaneously generates predetermined segments of the video representation of symbols to be displayed on a plurality of the input/output devices, and gating means for distributing the outputs from the group of segment generators to the respective input/output devices in proper time sequence.

In one embodiment, a symbol font in which each symbol occupies a block of 10 horizontal spaces and sixteen vertical lines of a scanned raster display device is employed. In this embodiment, a segmented character generator which comprises five segment generators is capable of producing video signals for 32 display devices.

Another embodiment, in which two groups of segment generators are employed where one group is operative with the even horizontal lines and the other group is operative with the odd horizontal lines, during a first field and then reversed, odd for even, and vice versa, during a second field of each frame, expands the total capability of the character generation means to provide video signals for 64 display devices using standard television synchronization signal timing.

A still further embodiment contemplates the addition of segment generators to allow for the generation of lower case characters including those characters which have portions below the base line as well as upper case characters to improve the overall efficiency of the display system.

Still other embodiments contemplate the generation of color information to display individual characters or symbols in a range of colors or alternatively to generate color information which corresponds to a given word of symbols to be displayed.

Due to the great flexibility of this invention, apparatus employing the basic segmented character generator can be used to generate video information for raster scan display devices, directed beam display devices, or digital plotters.

The various embodiments and features of the invention and details of operation are defined with particularity in the following specification.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a graphical illustration of the formation of individual symbol patterns for a group of eight display terminals.

FIG. 2 is a block diagram showing a systems environment embodying the invention;

FIG. 3 is a block diagram of a terminal control unit embodying the invention;

FIG. 4 is a block diagram illustrating a segmented character generator with a refresh storage connected to the inputs of the various segment generators;

FIG. 5 shows a block diagram which illustrates an embodiment of a single segment generator;

FIG. 6 is a block diagram showing the connections between the segmented character generator and a group of parallel to serial registers;

FIG. 6A shows in more detail the construction of a representative parallel to serial register;

FIG. 7 is a block diagram showing the generation of the various synchronization and control signals necessary for the operation of the multiplexed character generator;

FIG. 8 is a timing diagram showing the relationship between the vertical synchronization signals used to drive the group of display terminals;

FIG. 9 is a chart illustrating how the video signals for display terminal No. 1 and display terminal No. 20 are multiplexed;

FIG. 10 shows the gating circuits which perform the multiplexing of the signals shown in the chart of FIG. 9 to generate the video signals for representative video terminals No. 1 and No. 20;

FIG. 11 shows a hexadecimal representation of the video data for a row of characters on the odd and even scan, showing the data that is being generated by each of the segment generators at any instant of time; the first eight symbols shown are the letter A the ninth symbol generated is the letter B. This corresponds to the illustration shown in FIG. 1;

FIG. 4A is a block diagram showing how the basic symbol generator can be expanded to accommodate lower case characters;

FIG. 12 is a block diagram which illustrates how the system can be expanded by using a separate set of segment generators for the odd and even fields of an interlaced TV frame;
FIG. 13 is a block diagram showing how information indicating the color of complete words may be added to the multiplexed character generator; FIG. 14 is a block diagram showing how the multiplexed character generator may be expanded to included information representative of the color of each individual character; FIG. 15 is a block diagram showing another embodiment of the refresh buffer and segment generators for use with a smaller number of display terminals; FIG. 16 is a chart showing how the embodiment of FIG. 15 would be multiplexed.

DETAILED DESCRIPTION OF THE INVENTION

System Environment

Referring now to FIG. 2, a group of display terminals 101 through 132 are connected to a terminal control unit (TCU) 200 by means of lines 201. TCU 200 communicates with a central processing unit (CPU) 50 by lines 52. For illustrative purposes the symbols A and B are shown to be the first two symbols of the first row of characters on each of the first eight display terminals 101 through 108.

Terminal Control Unit

Referring now to FIG. 3, TCU 200 is shown in block diagram form. Incoming information is presented to I/O unit 204 on lines 202. I/O unit 204 then transfers in parallel the appropriate signals to refresh storage 300 on lines 206. Refresh storage 300 has a plurality of output lines 208, 210, 212, 214 and 216 which are connected respectively to segment generators PCG1 410, PCG2 430, PCG3 440, PCG4 450 and PCG5 460. The data transferred between refresh storage 300 and character generator 400 along each of the lines mentioned in parallel byte form. The segmented character generator has a plurality of output lines, one group of lines in parallel from each of the five segment generators. PCG1 is connected to multiplex generator 500 by line 428, PCG2 by line 438, PCG3 by line 448, PCG4 by line 458 and PCG5 by line 468. Multiplex video generator 500 accepts the video signals from said segmented character generator 400 and synchronization signals from timing & control unit 600 and generates appropriate video scanning signals which are distributed to the plurality of display terminals by lines 252. Timing the control unit 600 is connected to 1/0 unit 204 by lines 601, to refresh storage 300 by lines 602, to segmented character generator 400 by lines 603 and to multiplex video generator 500 by lines 604.

Refresh STORAGE

Referring now to FIG. 4, refresh storage 300 has two major sections. Information bytes in binary form are presented to core storage 302 by line 206 which connects the I/O unit 204 (see also FIG. 3) to the refresh storage 300. Core storage 302 stores command and data information in parallel in byte form for transmission to a group of line buffers. Core storage 302 is connected to the first line buffer 310 by lines 304. In an exemplary embodiment line buffer 310 contains four parallel, six bit, 64 character buffers 312, 316, 319, 316 and 316. Four parallel buffers allow simultaneous generation of video symbols for four times as many terminals as if a single six bit, 64 character buffer were used. Line buffers 320, 330, 340 and 350 are connected to line buffer 310. The outputs of line buffer 310 are connected to the inputs of segment generator PCG1 410 and also to the inputs of line buffer 320. In like manner, the outputs of line buffer 320 are connected by lines 210 to the inputs of segment generator 430 and to the inputs of line buffer 330. The outputs of line buffer 330 are connected by lines 212 to the inputs of segment generator 440 and to the inputs of line buffer 340. The outputs of line buffer 340 are connected by lines 214 to the inputs of segment generator 450 and to the inputs of line buffer 350. The outputs of line buffer 350 are connected by lines 216 to segment generator 460. It can be seen that in like manner, if the number of segment generators PCGs are increased, the number of line buffers can be also be increased to adapt the system to any font of symbols desired.

Segmented Symbol Generator

Referring now to FIG. 5, an exemplary segment generator 410 is shown. Lines 208 which are the outputs of the four buffers which make up line buffer 310 (see also FIG. 4) are connected to a plurality or OR circuits 411, 412, 413, 414, 415, and 416. The output 421 of OR-circuit 411 represents symbol data bit 1. The output 422 of OR-circuit 412 represents symbol data bit 2. The output 423 of OR-circuit 413 represents symbol data bit 3. The output 424 of OR-circuit 414 represents symbol data bit 4. The output 425 of OR-circuit 415 represents symbol data bit 5 and the output 426 of OR-circuit 416 represents symbol data bit 6. It can be seen that a number of data bits used to encode the symbol information could be either contracted or expanded depending upon the specific group of symbols involved. For example, an eight bit code could be used wherein additional OR circuits and inputs to read-only storage 420 would be necessary.

The odd/even signal is presented to read-only storage 420 on line 427. This signal is generated by flip-flop 417 which has as its input the vertical synchronization signal which appears on line 658.

Read-only storage 420 accepts as its input a data byte representative of a particular symbol to be generated. The output lines 428 of read-only storage 420 represent a single horizontal line segment of the symbol to be generated, which in the exemplary case is an eight-bit parallel byte.

Read-only storage output lines 428 from PCG1 are connected to parallel-to-serial register P/S 1 505 (see FIG. 6). In like manner, the outputs 438, (see also FIG. 4) 448, 458 and 468 from segment generators 430, 440, 450, and 460 respectively, are connected to P/S 2 506, P/S 3 507, P/S 4 508 and P/S 5 509, respectively.

Referring now to FIG. 6A, an exemplary P/S register is shown. Register P/S 1 505 contains four n-bit shift registers where n is equal to the number of bits in the data byte from the read-only storage elements. Since in the preferred embodiment being described, 32 display terminals are being controlled by one terminal control unit, four distinct shift lines are necessary which correspond to the four distinct buffers in each of the line buffers 310, 320, 330, 340, and 350 (see also FIG. 4). Line 428 is connected in parallel to n-bit shift registers 510, 530, 530, and 540. Referring also to FIG. 7, group shift lines are generated in group shift counter 630 which is connected to basic clock 610 by lines 613. Line shift 1 631 is connected to shift input of shift register 510 (see also FIG. 6A). Line shift 2 is connected to shift register 520 on line 632. Line shift 3 is connected to shift register 530 on line 633. Line shift 4 is connected to shift register 540 on line 634. The serial outputs from the shift registers are presented to the multiplexed video gates, an example of which is shown in FIG. 10 as AND-circuits 552, 554, 556, 558, 560, 572, 574, 576, 578 and 580.

Multiplexed Video Generator

Referring to FIGS. 6, 6A, 9 and 10, the multiplexed data connections necessary to generate the video signals for representative terminals 1 and 20 of a group of 32 terminals are shown.

In order to generate the correct video signals for display terminal 1, it can be seen from FIG. 9 that at line count 1 times the segment generator output PCG1GR (see also FIG. 6) must be gated to the video line, and at line count 2 PCG2GR must be gated to the video line. In like manner PCG3GR at line count 3, PCG4GR1 at line count 4, and PCG5GR1 at line count 5 must be gated to the video line for each field of data to achieve a complete horizontal line row of symbols for display terminal 1.

In like manner, to generate the video signals for display terminal 20, at line count 19, segment generator PCG1GR3 is gated; and at line count 5, PCG2GR3 is gated; at line count 6 PCG3GR3 is gated; at line count 7, PCG4GR3 is gated; and at line count 8, PCG5GR3 is gated to the video line for display terminal 20.

The outputs from P/S registers 505, 506, 507, 508, 509, are presented to the multiplex video gates according to the chart shown in FIG. 9.
For display terminal 1, P/S register output 511 (see also FIG. 6) is connected to AND-circuit 552 (see also FIG. 10) as one input. Line 641 (see also FIG. 7) is connected from 8 line counter 640 to a second input of AND-circuit 552 (FIG. 10) such that the information presented on line 511 will be gated to OR-circuit 562 along output line 563 at count LCI. In like manner, output line 512 representing PCG5GR1 is connected to a first input to AND-circuit 554 while line 642 is connected from 8 line counter 640 to a second input of AND-circuit 554. The output 555 of AND-circuit 554 is connected to a second input of OR-circuit 562 and represents the second horizontal line which field to be displayed on display terminal 1. Line 643 is connected to a third input of AND-circuit 556 along with PCG3GR1 513. The output 557 of AND-circuit 556 is connected to a third input of OR-circuit 562 and represents the third horizontal line in each field for each row of symbols to be generated on display terminal 1. Line 644 is connected to an input of AND-circuit 558 as is PCG4GR1 514. The output 559 of AND-circuit 558 is connected to a fourth input to OR-circuit 562 which represents the fourth field to be generated in each field of each row of symbols to be generated on display terminal 1. Line 645 is connected to a second input of AND-circuit 560 while PCG5GR1 515 is connected to a second input of AND-circuit 560. The output 561 of AND-circuit 560 is connected to a fifth input of OR-circuit 562 to provide the fifth line of each field of row of symbols to be generated on display terminal 1.

It is clear that if a different symbol set were used, the number of segment generators or the line count outputs could be increased or decreased to meet the requirements of a particular symbol set. In such a case the number of AND-circuits 552 through 560 would accordingly be increased or decreased as well as the number of inputs to OR-circuits 562.

The output 563 of OR circuit 562 is connected to one input of sync mixer 564. The second input to sync mixer 564 is vertical sync 1 651 (see FIG. 7) which is generated by vertical sync counter 650.

Sync mixer 564 can be any one of a number of circuits known in the television art to add a synchronization signal to an information signal for proper display on a display terminal. The output 565 of sync mixer 564 is then connected to the No. 1 display terminal 101 (FIG. 2). Referring to FIG. 9, it can be seen that the video signals for display terminals 1 through 8 are generated from the GR1 signals of segment generators PCG1, 2, 3, 4, and 5. GR2 provides a gating signal for the generation of the video signals for display terminals 9 through 16. GR3 provides the gating signals for the generation of video signals for display terminals 17 through 24 and GR4 generates the gating signals for the generation of video signals for display terminals 25 through 32.

Referring again to FIG. 10 and to FIG. 9, the video signals for display terminal 20 (not shown) is generated in AND-circuit 572 by line count 4 644 and PCG1GR3 531, in AND-circuit 574 by line count 5 645 and CGG2GR3 532, in AND-circuit 576 by line count 6 646 and PCG3 533, ANDing in AND-circuit 577 by line count 7 647 and PCG4 GR3 534 and in AND-circuit 580 by line count 8 648 and PCG5 GR3 535. The outputs 573, 575, 577, 579, 581 of AND-circuits 572, 574, 576, 578, 580 respectively are connected to respective inputs of OR-circuit 562 along with a cursor input as in the circuitry for generating the video signals for No. 1 display terminal 101 (FIG. 2).

The cursor can be generated by any conventional means and is shown into the video stream at AND-circuits 562 or 682. The output 583 of OR-circuit 583 is connected to sync mixer 584 which has as another input vertical sync 4 654 which is generated by vertical sync counter 650. Sync mixer 584 is an identical circuit to sync mixer 564 and circuits of this type are well known in the art. The output 585 of sync mixer 584 is connected to display terminal 20 120.

Timing and control

Referring now to FIGS. 7, 8 and 12, a clock signal generator 610 generates a basic timing signal which is used to generate all the necessary timing signals for the terminal control unit 200. The output of clock generator 610 is connected to sync generator 620 by line 612 and to group shift counter 630 by line 613. Sync generator 610 generates the horizontal synchronization signals which are presented on line 621 and a base vertical synchronization signal which is presented on line 628.

Sync generator 620 is connected to vertical sync counter 650 by line 625 and to S line counter 640 by line 621.

Eight line counter 640 generates signal line count 1 through line count 8 which are required for the multiplex video gating. Vertical sync counter 650 generates a series of vertical synchronization signals each of which is staggered in time by one horizontal time period. Vertical sync 1 through vertical sync 8 are presented on lines 651 through 658. The time displacement of the vertical synchronization signals is shown clearly in FIG. 8. Where h is equal to one horizontal time line, including trace and retrace.

The time displacement of vertical synchronization signals 2 through 8 allows the video signals for each of the 32 display terminals 101 (see FIG. 2) to 132 to begin at the same relative position on the face of the display device. Referring to FIG. 11, it can be seen that if the vertical synchronization signals were not displaced in time, at a first instance in time, a video signal would appear only on display terminals 1, 9, 17, and 25. At the beginning of a second horizontal line scan in each field, a video signal would appear in addition only on display terminals 2, 10, 18, and 26, on the third horizontal line scan display terminals 3, 11, 19 and 27 and so on with an additional four displays beginning with each successive horizontal line until all 32 displays are presenting symbols.

The staggering of the vertical synchronization signals allows the video signal for each of the 32 display terminals to begin the first horizontal line of each field at the same relative position on each display device.

Group shift counter 630 provides four shift signals shift 1, 631, shift 2, 632, shift 3 633 and shift 4 634. These shift signals are presented to P/S registers to gate the video information for the proper display terminal to the multiplex gate at the correct time.

Lower Case Character Generation

Referring now to FIGS. 1, 4A and 11, the system previously described is capable of generating a symbol set which occupies 10 horizontal lines for symbol generation plus an additional six horizontal lines for blank space between rows of symbols.

It is most common in alphanumeric display systems to use a symbol font which contains only upper case characters. The apparatus of the instant invention has the capability with the addition of two additional 64 character three-bit line buffers, six-bit to three-bit parallel converter logic and two read-only storage segment generators of generating lower case characters which have tails below the bottom line of the upper case symbols. That is, the tails of the lower case characters would extend into horizontal lines 11 through 14.

Referring now to FIG. 4A, line buffer 5, 350 is connected by line 216 to a 64 character three-bit line buffer 360, which includes six-bit to three-bit parallel converter logic at the input, in addition to segment generator 460. The output 218 of line buffer 360 is connected to segment generator 470 and also to the input of line buffer 370. Line buffers 360 and 370 are capable of storing a fully 64 character row of three-bit characters. Since a three-bit character will allows eight combinations, and since there are five lower case characters in a normal alphabet which extend below the base line (i.e., f, p, q, y), with a single code reserved for upper case and lower case characters which do not extend below the line to blank out segment generator 470 and segment generator 480, there are two unused codes available for additional symbols in raster lines 11, 12, 13 and 14 of each horizontal row of symbols. The output 478 of segment generator 470 and the output 488 of segment generator 480 are then connected to additional P/S registers which must be added to accommodate the lower case symbols.
Additional logic is required to implement the P/S registers and additional multiplex AND gates which are required for lower case character generation.

System Expansion

Referring now to FIG. 12, the number of display terminals which can be accommodated by apparatus embodying the instant invention, can be expanded from 32 to 64 by the division of a set of segment generators 410, 430, 440, 450, 460 into two sets 491, 492 which would be used to generate the odd and even field of the two sets of display terminals simultaneously.

Odd/even flip-flop 417 gates lines 208, 210, 212, 214, 216 to set segment generator 491 or 492 alternate fields to achieve 100 percent utilization of the ROS elements 420 (see FIG. 5) of each segment generator.

The complete duplicate structure is not shown since it is clear from the preceding description of the basic embodiment.

Generation of Color Information

Referring now to FIGS. 13 and 14, the instant invention also includes embodiments for generating color information for display on a display terminal either on a character-by-character basis as shown in FIG. 14 or on a word-by-word basis as shown in FIG. 13.

Word-by-Word Color

Buffer output lines 208, 210, 212, 214, and 216 in addition to being connected to the segment generators as shown in FIG. 14, is also connected to an AND-gate 710 (FIG. 13) which generates an active output signal to color latch 1, 720 when the information on lines 208 represent a color code signal. This color code signal would occur only during the space between words in the flow of information to be displayed. Color latch 1, 720 is necessary when the signals on lines 208 are not present for a sufficient length of time to provide proper generating signals to AND-gate 730. The output 721 of color latch 1, 720 is connected to a first input of each of a group of AND circuits which comprise the AND-group 730. A second input of each of these AND circuits is from 8 line counter 640 which is this illustrative example would be lines 641, 642, 643, 644, 645, 646, 647, and 648. In like manner, an AND circuit and color latch in a group of AND gates will be required to accommodate each of the segment generators 410, 430, 440, 450, 460 shown in FIG. 4. These are not shown in detail here since they are duplicates of the logic necessary to generate the color information for the first two lines of each symbol represented by the output from PGC1. The output 751 of the first AND circuit in AND-group 730 is connected to a first input of a first line OR-circuit 780. Outputs 2 through 8 of AND-group 730 would be connected to other OR circuits to generate color information for display terminals other than display terminal 1. In like manner, the second output 742 from AND-group 740 is connected to a second input of OR-circuit 780, the third output 753 from AND-group 750 the fourth output 764 from AND-group 760 and the fifth output 775 from AND-group 770 are connected to respective inputs OR-circuits 780 to provide complete color information for a word of symbols of each of which occupy ten horizontal lines on a display device.

The output 781 of OR 780 is connected to AND-circuit 784 and to inverter 782. The output 783 of inverter 782 is connected to a first input of AND-circuit 786. A second output of AND-circuits 784 and 786 is from the appropriate multiplex video gates 562 on output line 563 as shown in FIG. 10. The output of AND-circuit 784 provides a shift signal to the three-bit color shift register 790. The output 787 of AND-circuit 786 provides a gating input to color gates 794, 795, and 796. The three primary colors generated there are selected by output 792, 793 which is connected to second inputs of color gates 794, 795, and 796. Outputs 795, 797, and 799 of color gates 794, 796, and 798 are connected to color/grayscale encoder and sync mixer 810. Vertical sync 1, 651 is connected to color/grayscale level encoder and sync mixer 810 to provide the appropriate synchronization signals. Outputs 811 of encoder and sync mixer 810 provides video signals for display terminal 1 which can contain, in addition to the information to be displayed, color word information or grayscale scale information.

The apparatus described for defining the color of words on the display device inherently have the capability also of defining the gray scale rendition of the information to be displayed.

Character by Character Basis

Referring now to FIG. 14, exemplary apparatus is shown which allows generation of color information on a character-by-character basis rather than a word-by-word basis. Basically, this mode of operation requires in addition to the symbol code byte three additional bits in parallel which carry a color code for each symbol. Lines 208 (FIG. 3) from refresh storage in addition to being connected to the segment generators are now expanded to include three additional lines which are connected to a group of AND-circuits 820 which represents in this case three AND circuits each of which produces an active output when the inputs represent a color code. Output lines 821 from AND-circuits 820 are connected to additional three-bit section 822 of parallel to serial register 805.

The portions of the apparatus are not described in detail here, but have been previously described in detail either in the description of the basic embodiment of the invention or in the embodiment for generating color words.

The color information contained in the three-bit section 805 of parallel to serial register 805 is now placed directly on the data line for video generation. Circuits 730, 780, 790 are the same as described previously. Counter 824 has as its input shift line 631. Counter 824 provides a running count to 11 with an output whenever the counter exceeds three. This output 825 is connected to AND-circuit 830 and to inverter 826. When the count exceeds three, symbol information rather than color information is being presented. At this time, output line 825 from counter 824 activates AND-circuit 830 to allow the color information to be presented to gates 832, 834 and 836. The outputs 833, 835 and 837 of these gates are connected in turn to first inputs of OR-circuits 840, 842 and 844 which are in turn coned to encoder and sync mixer 810.

It is to be noted, that in each of the embodiments described, the signal path was shown only for display terminal 101. Identical circuitry would be used for each of the other 21 displays in the typical system with the connections made according to the chart shown in FIG. 9.

Reduced System

In those applications where a small number of display terminals will be attached to the terminal control unit, a minimum system is desired to eliminate unnecessary hardware. Referring now to FIGS. 15 and 16, a reduced embodiment is shown in which the character generator is generating symbol information for only four display terminals.

In this embodiment, the output of core storage 302 (FIG. 4) is connected to the input of segment generator PGC1, 410 and to a group of OR-circuits 308. The output of OR-circuits 308 provides the inputs to line buffer 310. The outputs from line buffer 310 are connected to segment generator PGC2/4, 430 and to line buffer 320. The outputs from line buffer 320 are connected to PGC3/5, 440 and to AND-circuits 306. Counter 660, which is an 8 line counter similar to line counter 640 with additional gates to generate outputs C2, C3, C4, and C5, has its input connected to horizontal sync 621 (FIG. 7) and presents outputs C2, C3, C4 and C5. C2 and C4 are connected to PGC2/4, 430 to control the operation of PGC2/4 to generate either the third and fourth lines of a symbol or the seventh and eighth lines of a symbol. In like manner, output lines C3 and C5 are connected to PGC3/5, 440 to activate PGC3 to g blue are reset lines 5 and 6 of a symbol or to generate lines 9 and 10 of a symbol respectively. Line C3 is also connected to each of the AND circuits in AND-group 306 to allow recirculation of the symbol information. The outputs of AND-group 306 are connected to second sets of inputs in OR-circuits 308 to provide recirculation of the symbol information to line buffer 310. The Boolean expression for the outputs C2, C3, C4 and C5 is:

$$C2 = LC2 + LC3 + LC6 + LC7$$
Since there are not only three sets of outputs from the segment generators, the amount of multiplex logic that is needed is greatly reduced. Some of the details of the embodiments of the invention described have not been shown since these details would be clear to those skilled in the art.

As has been shown in the detailed description of the invention, there are many combinations of apparatus which can be built utilizing the instant invention.

**OPERATION**

Referring now to FIGS. 2, 3, 4 and 5, the operation of an preferred embodiment of the invention will be described.

Information to be displayed is transmitted from CPU 50 (FIG. 2) to terminal control unit 200 along lines 52. Terminal control unit 200 then generates appropriate video signals for the various display terminals in response to the information from the CPU 50. These video signals are transmitted to display terminals 101 through 132 along lines 201.

The terminal control unit 200 receives the information from CPU 50 in 1/0 control 204 (FIG. 3) which performs all necessary interface communications with the CPU 50. The information is then transmitted to refresh storage 300 and stored in core storage 302. At the appropriate time under the control of timing and control element 600 (FIG. 3), information byte representing symbols to be displayed are transmitted to a first line buffer 310. Line buffer 310 acts as a buffer between core storage 302 and the first segment generator PGCG 410. Line buffer 310 is not necessary in applications where the operating speed of the core storage and the segment generator are comparable. Segment generator 410 generates the first scan line of a symbol in each row of symbols on the odd horizontal scans and the second line of a symbol in each row of symbols on the even horizontal scans in response to the information byte from line buffer 310.

Each of the line buffers 310, 320, 330, 340 and 350 provides a delay of one horizontal line scan time so that the output signals from line buffer 310 to line buffer 320, from line buffer 320 to line buffer 330, from line buffer 330 to line buffer 340 and from line buffer 340 to line buffer 350 begin at the start of a row of symbols. Thus, in response to the inputs from the respective line buffers, PCG2 430 generates the third line of each symbol in a row on the odd horizontal scans and the fourth line of each symbol in a row on the even horizontal scans, PCG3 440 generates the fifth line of each symbol in a row on the odd horizontal scans and the sixth line of each symbol in a row on the even horizontal scans. PCG4 450 generates the seventh line of each symbol in a row on the odd horizontal scans and the eighth line of each symbol in a row on the even horizontal scans and the PGCG 460 generates the ninth line of each symbol in a row on the odd horizontal scans and the tenth line of each symbol in a row on the even horizontal scans.

It is clear that this apparatus could be extended to accommodate larger character sizes or reduced to accommodate smaller character sizes or reduced to sizes by adding or deleting line buffers and segment generators.

Timing and control circuitry 600 controls the gating of each of the four groups of information signals from the line buffers to the segment generators along lines 208 and also controls the timing of the output signals from the read-only storage elements 210 to multiplex video generator 500.

The outputs from character generator 400 present a parallel signal which contains the video information. Timing and control unit 600 also provides control signals and timing signals along lines 604 to multiplex video generator 500. Multiplex video generator 500 transmits the video signals to the appropriate display terminal for visual display.

Referring now to FIGS. 1, 2, 3, and 11, the generation of representative symbols will be explained.

If for example, as shown in FIG. 2, it is desired to generate the symbol upper case A in the first symbol position in the first row of symbols on each of the first eight display devices, and the symbol upper case B in the second symbol position on the first row of symbols on each of the first display devices, the apparatus embodying the invention would operate in the following manner.

A group of information signals in parallel byte form representing the symbol A is transmitted from CPU 50 to terminal control 200 and stored in core storage 302. Each of these information bytes takes the binary form 000001, which is the binary representation for the symbol A. At the appropriate instant of time, in synchronism with the raster scan for the display devices, the information byte representing the symbol A for the first row of symbols of the first display device is gated to the sequential line buffers (FIG. 4).

The binary representation 000001 acts as an address for a particular group of storage elements in segment generator 410 which have stored therein the video representation for the first line of the symbol A.

In eight-bit binary form, the video representation for the first line of the symbol A is 00010100. This binary information is here presented in hexadecimal notation as '8.'

The eight-bit binary representation is transmitted on line 428 to P/S converter 505 (FIGS. 4, 6A, 6B).

P/S converter 505 serializes the eight-bit binary representation and presents this serial representation along line 511 to multiplex video generator gates 552 (FIG. 10).

Since this example deals only with the data generated for the first eight display devices 101 through 108, the other outputs 521, 531 and 541 of P/S converter 505 will not be explained in detail. These outputs represent the video signals for display devices 109 through 116, 117 through 124, and 125 through 132 respectively.

Due to the speed of operation of the core storage 302 and the segment generators 410 through 460, are generated four groups of signals in parallel through a single set of line buffers and a single segmentated character generator.

Referring now to FIGS. 6 and 10 the output line 511 which transmits the video signals for the first segment of each symbol to be displayed on display devices 101 through 108, multiplex gate 552 is turned on by signal LC1 on line 641 during line 1 of each row of symbols on odd horizontal scans and line 2 of each row of symbols on even horizontal scans. The video being presented on line 511 at the time of the first line of an odd horizontal scan is hexadecimal '18;' which is transmitted to sync mixer 564 (FIG. 10) through OR-gate 566.

In sync mixer 564 synchronization signals are added to the video signals to form a composite video signal for transmission to display terminal 101. The sync vertical signal 1 represents a set of scanning synchronization signals which cause the raster on display devices 101, 109, 117, 125 to begin one horizontal scanning line time in advance of the beginning of the raster scan, for display devices 102, 110, 118, and 126, which is in synchronism with sync signal vertical sync 2.

This "staggering" of the synchronization signals, and therefore the raster scan of the groups of display devices, allows the visual image presented by each display device to begin at the same relative location on the face of each display device.

If the synchronization signals were not "staggered" the visual impression obtained on viewing eight display devices side by side would be that each row of characters in the second and subsequent display devices would be displayed vertically down two horizontal lines from the preceding display device. This would result in an effect similar to that shown in FIG. 1 if the first symbol from each display device were placed side by side on a single composite display device.

In a similar manner as described above, one horizontal line time after the information byte has passed through line buffer 320, the binary representation 000001 is presented to segment generator 430 which then in response to this input address signal and ODD/EVEN flip-flop 471 in ODD state, generates the binary representation 01111110 which represents line 3 of the symbol A. At the same time, the information signals...
representative of the first symbol on display devices 102, 110, 118 and 126 are presented to segment generator 410.

For simplicity of explanation, the symbol A will be generated also as the first symbol in the first line of symbols on display device 102.

In a similar manner to that described above, the video signal from segment generator 420 (FIG. 4) is serialized and presented to gate 554 which is turned on by LC2 during the second line of each row of symbols in each horizontal scan. Thus, the video representation 01111110 is transmitted to display device 101 in proper time sequence.

As can be seen from FIG. 1, the data representing the first line of the first row of symbols for the display device 102 is similarly presented to the display device at the same time. However, the second symbol on display device 102 is not presented since the chart of FIG. 9 sets out the appropriate gating conditions for each of the display terminals for each line count and segment generator.

In like manner, on horizontal line time later the information signal, representing upper case A, is presented to segment generator 440 (FIG. 4) which responds by generating video replications of display device 120 is corrected to the fifth position of the symbol A. At the same time, line 3 of the first symbol on display device 102 is being generated and line 1 of the first symbol for display devices 103, 111, 119 and 127 are being generated.

In like manner, lines 7 and 9 of the first symbol in the first row of symbols for display device 101 is generated on the first odd horizontal scan. The video representation for line 7 being 11111111 and for line 9 being 11000011.

At the time line 7 is being generated on display device 101, line 5 is being generated for display device 102, line 3 is being generated for display device 103 and line 1 is being generated for display devices 104, 112, 120 and 128. It may be noted at this point, that when the first symbol to be generated on each display is being displayed, the segment generators 418, 430, 440, 450 and 460 (FIG. 4) are operated in a staggered manner, as shown in FIG. 11, with segment generator 460 not act to generate line 9 for the first display device 101 until PGC1 segment generator 410 is generating the first line of the first symbol for display devices 105, 113, 121 and 129.

In the manner described above, the first line of the first symbol to be displayed on each of the display devices 101 through 108 is corrected to the first eight multiplexed symbol positions. In the ninth symbol position, the first scan line of the first symbol in the second row of symbols on display device 101 can be generated since segment generator 410 is free. In like manner, on horizontal line time later the third line of the first symbol in the second row to be generated on the first display device 101 is generated while the first scan line of the first symbol in the second row to be generated on display device 102 is generated. Similarly, the second and further symbols on each row of symbols for each display device are generated in the staggered manner described above.

Referring to FIGS. 9 and 10, the multiplexing of the video representations to form the visual images on a representative display device 120 is shown.

Display device 120 is contained in the third group of eight multiplexed video display devices. It can be seen that the video signals representing the video to be displayed on display device 120 are represented in each case by PCG1GR3 on line 531, PGC2GR3 on line 532, PGC3GR3 on line 533, PGC4GR3 on line 534 and PGC5GR3 on line 535.

Since display device 120 is the fourth unit in the third group, the staggered synchronization signals are the same as for display device 104.

Thus, the first line of video for each symbol to be generated on display device 120 is gated by signal LC4 along line 644. This means that while the fourth segment (lines 7 on odd or 8 on even scans) of each symbol on display device 101 is being generated, the first segment (lines 1 on odd or 2 on even scans) of each symbol on display device 120 is being generated. In like manner, the second segment is generated at LCS time, the third segment is generated at LC6 time, the fourth segment is generated at LC7 time and the fifth segment is generated at LC8 time.

The video signals are mixed in sync mixer 584 with vertical sync 4 to allow the visual image presented to begin at the same relative location on the display device as each of the other display devices.

The particular font of characters employed requires eight spots in the horizontal direction and ten lines in the vertical direction with an additional six vertical lines providing the space between rows of symbols and two spots providing the horizontal space between characters in each row. This format, of course, is completely flexible and the invention as described above could be used with any symbol format.

While the operation of the invention has primarily described for an odd horizontal field, operation on the even horizontal field would be identical with line counts 1 through 8 representing horizontal lines 2, 4, 6, 8, 10, 12, 14 and 16 respectively, rather than lines 1, 3, 5, 7, 9, 11, 13, and 15 for each row of symbols.

Lower Case Characters

Referring now to FIG. 4A, the apparatus embodying the instant invention has the capability of expansion to generate "-tails" for those lower case characters which have portions below the upper case character base line. For example, the lower case characters g, j, p, q, and y have that portion of the character above the base line generated in the manner described above, and that portion of the character below the base line, that is, the tail, generated by additional segment generators 470 and 480 which together have the capability of generating information on four additional lines of each symbol block.

Line buffers 360 and 370 store 64 three-bit symbols which represent the lower case information of a symbol being generated or the absence of lower case information. For example, the three bit character 000 could be used to represent all upper case characters and lower case characters which do not extend below the base line in which case segment generators 470 and 480 would not be used at all since the three bit character 000 would not address any of the active locations of either of these segment generators.

The three bit character 001 might represent lower case g, 010-j, 001-p, 100q and 101-y. This information would be gated through the multiplex video generator in a manner similar to that described for upper case characters. The details of the implementation for lower case characters could readily be added by one skilled in the art in view of the prior disclosure regarding upper case character generation.

System Expansion

Referring now to FIG. 12, it is seen that the number of display devices serviced by the multiplexed character generator can be doubled by dividing the set of segment generators into odd and even subsets 491, 492 so that one subset of segment generators 491 can be generating an odd horizontal field of a first group of 32 display terminals while a second set of segment generators 492 is generating video information for an even horizontal field for a second set of 32 display devices.

Generation of Color Information

Referring now to FIGS. 13 and 14, it can be seen that a character containing only color information can readily be handled by the apparatus during the time of a space between words on any line of symbols.

A word color signal is received and detected by AND-gate 710 (FIG. 13) which sets color latch 1, 720. This color latch then remains set for the entire word to be displayed in a particular color. The video information from the segmented character generators is then gated with the color latch signal through a series of logic gates to a color shift register 790. The output of the color shift register determined which combination of the three gates 832, 834, 836 will be encoded in encoding and sync mixer 810 and transmitted to the display devices.

It may be noted that in place of color information, gray scale information can be transmitted and handled by the same apparatus.
In the character by character color embodiment (FIG. 14), apparatus essentially the same as for the word by word color embodiment is employed with the exception that the color code is presented in parallel with each symbol to be displayed and carried along as an additional three bits through the parallel to serial converters.

A counter 824 is connected to shift line 631 to distinguish between color information which is present during the first three bits and video information which is present during bits 4 through 11. Counter 824 is reset on a count of eleven since this count represents one fully character of color and video information.

When the count from counter 824 is less than three, the information from the parallel to serial converters 505 and 822 are transmitted to a color register 790 which then decodes the color information and generates signals to activate the proper primary color signals. When the count from counter 824 exceeds three, the video information is gated through AND-circuit 830 to the color gates 832, 834 and 836. The video information present on lines 833, 835 and 837 is then gated with a cursor signal in gates 840 842, and 844 and presented to color/gray level encoder and sync mixer 810. The composite video color signal including cursor information is then presented to the display device on line 811.

As mentioned above, the same apparatus can be employed to achieve a gray scale rendition rather than color rendition of the video information to be displayed. Also, color/gray scale information may be encoded in more or less than three bits within the scope of the invention.

Reduced System

Referring now to FIGS. 15 and 16, a reduced system is described for those applications where a small cluster of display devices will be attached to a terminal control unit.

In this embodiment, three segment generators 410, 430 and 440 are used where segment generator 410 always generates the first line of a symbol in each horizontal scan, and where segment generator 430 generates the second and fourth line of each symbol in each horizontal scan and segment generator 440 generates the third and fifth line of each symbol in each horizontal scan. To achieve this reduction, the information bytes representing the symbols to be generated must be recirculated an additional time through line buffers 310 and 320. After the first line of each symbol is generated by segment generator 410, the information signals are presented to segment generator 430 and control line 2 is activated indicating that the second line of each symbol will be generated. In like manner, one horizontal line period later control line 3 is activated which allows segment generator 440 to generate the third line for each symbol in each horizontal scan.

Since the entire symbol is not complete at this point, when control line 3 is activated, the information present at the output of line buffer 320 is recirculated through gates 306 to OR-circuit 308 which then transmits this information to line buffer 310. This allows segment generator 430 on the second pass of the information signals to generate the fourth line of each symbol to be generated with control line 4 active and control line 2 inactive. Similarly, one horizontal line time later, control line 5 is activated and control line 3 is inactive allowing segment generator 440 to generate the fifth line of each symbol in each horizontal scan. At this time since control line 3 is inactive, the information signals are not recirculated through gates 306.

Referring now to FIG. 16, the multiplexing of data between the five segment generators and the four display devices is shown. At count 1 segment 1 of display 1 is generated. At count 2 segment 2 of display 1 is generated and segment 1 of display 2, etc., as in the basic system. The condition of recirculate gate 3 is shown for each count time by GATE OPEN/CLOSE with C3 active on "I"'s and inactive on "O"'s. While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A system for information display comprising:
   processing means for transmitting information to and receiving information from a plurality of input/output devices;
   storage means connected to said processing means for receiving the information therefrom and for storing said information, said storage means having a plurality of output lines;
   symbol generation means comprising a plurality of segment generators wherein each of said segment generators is connected to one of said plurality of outputs from said storage means, and wherein each of said segment generators simultaneously generates a portion of a symbol for a different one of said plurality of input/output devices, said segment generators being independently accessible at the respective outputs thereof;
   a plurality of gating means connected to the outputs of said symbol generation means for assembling and distributing symbol segments generated by said plurality of segment generators;
   and
   a plurality of input/output devices connected to said plurality of gating means for utilization of the information presented.

2. A system for information display according to claim 1, wherein:
   said storage means comprises:
   an asynchronous storage element which communicates with said processing means; and
   a synchronous storage element having its input connected to the output of said asynchronous storage element and having a plurality of output lines corresponding to the number of segment generators, wherein said synchronous storage element is divided into a plurality of storage elements, each said storage element providing temporary storage for the information signals corresponding to a line of symbols to be displayed.

3. A system for information display according to claim 1 wherein said symbol generation means further comprises:
   a plurality of fixed storage elements, each of said fixed storage elements containing the video representation of one segment of a symbol to be displayed.

4. A system for information display according to claim 1, further comprising:
   synchronization means for generating a plurality of sets of synchronization signals, wherein each of said sets of synchronization signals synchronizes a set of said plurality of input/output devices, and wherein each of said synchronization signals generated is separated in time from the synchronization signal immediately preceding it by an integral number of horizontal line time periods, thereby causing the display of information to begin at the same relative point on each of said plurality of input/output devices.

5. A system for information display according to claim 4 wherein said plurality of input/output devices is divided into eight sets of four input/output devices per set and wherein said synchronization means generates eight sets of synchronization signals, each of said sets of synchronization signals displaced from the preceding set of synchronization signals by an incremental time period.

6. A system for information display according to claim 1, wherein said processing means comprises a central processing unit of a digital computer;
   said storage means comprises a magnetic storage apparatus to store information from said central processing unit in parallel byte form and a plurality of sequential line buffer storage elements wherein each of said sequential line buffer storage elements stores the information signals representing one row of symbols to be displayed on a plurality of input/output devices;
   each of said segment generators comprising a plurality of read-only storage elements wherein each of said read-only storage elements stores the video representation of a segment of a symbol, and wherein each of said segment
generators simultaneously generates a portion of a symbol to be displayed on a different one of said plurality of input/output devices; said gating means comprises a plurality of parallel to serial converters connected to respective outputs of said segment generators, and a plurality of gates for assembling the complete video representation for each symbol to be displayed from the outputs of said segment generators in proper time sequence; and synchronization means for controlling the operation of said storage means and said character generation means and for generating synchronization signals to be combined with said video representations to form composite video signals for presentation to said plurality of input/output devices.

7. Apparatus according to claim 1, further comprising: means connected to said plurality of gating means for generating information representative of a visual characteristic of each symbol to be displayed.

8. A system for information display, according to claim 7, wherein said generating means generates information representative of a color of each symbol to be displayed.

9. A system for information display according to claim 7, wherein said generating means generates information representative of a degree of luminance of each symbol to be displayed.

10. Apparatus according to claim 1, further comprising: means connected to said plurality of gating means for generating information representative of a visual characteristic of each set of symbols to be displayed.

11. Apparatus according to claim 10, wherein said means for generating, generates information representative of a color of each set of symbols to be displayed.

12. Apparatus according to claim 10, wherein said generating means generates information representative of a degree of luminance of each set of symbols to be displayed.

13. A symbol generator, comprising: a plurality of symbol segment generating means, each for simultaneously generating a portion of a symbol for a different one of a plurality of input/output devices each being independently accessible to generate a segment of each symbol to be displayed in proper time sequence; multiplexing means connected to outputs of said plurality of symbol segment generating means for assembling symbols to be displayed from a plurality of symbol segments generated by said plurality of symbol segment generating means and transmitting assembled symbols to a plurality of display devices in proper time sequence.

14. A symbol generator according to claim 13, wherein said plurality of symbol segment generating means generates segments of alphanumeric characters.

15. A symbol generator according to claim 13, wherein said plurality of symbol segment generating means generates segments of graphic symbols.

16. A symbol generator according to claim 13, wherein said plurality of symbol segment generating means comprises: a first group of symbol segment generating means for generating a first set of symbols and a first portion of a second set of symbols; and a second group of symbol segment generating means for generating a second portion of said second set of symbols.

17. A symbol generator according to claim 16, wherein: said first set of symbols comprise upper case alphanumeric symbols; and said second set of symbols comprise lower case alphanumeric symbols.

18. A symbol generator according to claim 13, further comprising: means for gating input signals into a feedback path for transmission of said input signals to inputs of said plurality of symbol segment generating means a plurality of times.

19. A symbol generator according to claim 18, wherein said plurality of symbol segment generating means comprises: a first group of symbol segment generating means for generating a first set of segments for each symbol to be displayed; and a second group of symbol segment generating means for generating a plurality of segments in each of said second group of symbol segment generating means under the control of said means for gating input signals to generate symbols for a plurality of display devices whereby each of said second group of symbol segment generating means generates a plurality of segments of each symbol to be displayed.

20. A symbol generator accordingly to claim 13 wherein each of said segment generator means comprises a plurality of storage means, each of said storage means storing a binary representation of one segment of a symbol to be generated.

21. A multiplexed symbol generator, according to claim 20, wherein each of said storage elements comprises: a read-only storage device which contains the binary representation of a segment of a symbol to be generated.

22. A multiplexed symbol generator, accordingly to claim 20, wherein each of said storage elements comprises: a plurality of programmable semiconductor storage elements.

23. A multiplexed symbol generator, according to claim 20, wherein each of said storage elements comprises: a plurality of magnetic storage devices for storing the binary representation of a segment of a symbol to be generated.

24. A system for information display comprising: means for transmitting information; storage means, connected to said means for transmitting, for receiving and storing said information, said storage means having a plurality of output lines; symbol generator means comprising a plurality of segment generators wherein each of said segment generators is connected to one of said plurality of output lines; and wherein each of said segment generators simultaneously generates a segment of a plurality of symbols to be displayed on a plurality of display devices said segment generators being independently accessible at the respective outputs thereof; multiplexing means connected to said outputs of said symbol generator means for assembling and distributing symbol segments generated by said plurality of segment generators; and a plurality of display devices connected to said multiplexing means for displaying the information transmitted.

25. A system for information display according to claim 24, wherein said storage means comprises: an asynchronous storage element which communicates with said processing means; and a synchronous storage element having its input connected to the output of said asynchronous storage element and having a plurality of output lines corresponding to the number of segment generators, wherein said synchronous storage element is divided into a plurality of storage elements, each said storage element providing temporary storage for the information signals corresponding to a line of symbols to be displayed.

26. A system for information display accordingly to claim 24 wherein said symbol generation means further comprises: a plurality of fixed storage elements, each of said fixed storage elements containing the video representation of one segment of a symbol to be displayed.

27. A system for information display according to claim 24 further comprising: synchronization means for generating a plurality of sets of synchronization signals, wherein each of said sets of synchronization signals synchronizes a set of said plurality of input/output devices, and wherein each of said synchronization signals generated is separated in time from the synchronization signal immediately preceding it by an integral number of horizontal line time periods, thereby causing the display of information to begin at the
same relative point on each of said plurality of input/output devices.

28. A system for information display according to claim 27 wherein said plurality of input/output devices is divided into eight sets of four input/output devices per set and wherein said synchronization means generates eight sets of synchronization signals, each of said sets of synchronization signals displayed from the preceding set of synchronization signals by an incremental time period.

29. A system for information display accordingly to claim 10 wherein said processing means comprises a central processing unit of a digital computer;

said storage means comprises a magnetic storage apparatus to store information from said central processing unit in parallel byte form and a plurality of sequential line buffer storage elements wherein each of said sequential line buffer storage elements stores the information signals representing one row of symbols to be displayed;

each of said segment generators comprises a plurality of read-only storage elements wherein each of said read-only storage elements stores the video representation of a segment of a symbol, and wherein each of said segment generators is independently accessible;

said gating means comprises a plurality of parallel to serial converters connected to respective outputs of said segment generators, and a plurality of gates for assembling the complete video representations for each symbol to be displayed from the outputs of said segment generators in proper time sequence; and

synchronization means for controlling the operation of said storage means and said character generation means and for generating synchronization signals to be combined with said video representations to form composite video signals for presentation to said plurality of input/output devices.

30. Apparatus accordingly to claim 24, further comprising:

means connected to said plurality of gating means for generating information representative of a visual characteristic of each symbol to be displayed.

31. A system for information display, accordingly to claim 30, wherein said generating means generates information representative of a color of each symbol to be displayed.

32. A system for information display according to claim 30, wherein said generating means generates information representative of a degree of luminance of each symbol to be displayed.

33. Apparatus according to claim 24, further comprising:

means connected to said plurality of gating means for generating information representative of a visual characteristic of each set of symbols to be displayed.

34. Apparatus according to claim 33, wherein said means for generating, generates information representative of a color of each set of symbols to be displayed.

35. Apparatus accordingly to claim 33, wherein said generating means generates information representative of a degree of luminance of each set of symbols to be displayed.
UNIVERS STATES PATENT OFFICE
CERTIFICATE OF CORRECTION


Inventor(s) Ancile E. Malden

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, line 53 after "accordingly" please omit--to--.
Column 3, line 5 "included" should be--include--;
  " , line 43 "Timing the" should be--Timing and--;
  " , line 59 after "many" please insert--display--;
  " , line 73 omit the first "be".
Column 5, line 11 insert--in--as the last work in that sentence;
  " , line 16 "or" should be--OR--;
  " , line 56 "GCC" should be--PCG--.
Column 6, line 63 "fully" should be--full--;
  " , line 64 "allows" should be--allow--;
  " , line 66 "f" should be--j--.
Column 7, line 41 "for" should be--a--.
Column 8, line 42 "21" should be--31--.
Column 9, line 61 after "character" omit--or reduced to--.
Column 10, line 61 "staggered" should be--staggered--.
Column 11, line 19 "on" should be--one--;
  " , line 49 "on" should be--one--.
Column 12, line 37 "600" should be--000--;
  " , line 44 "100 q" should be--1000 q--.
Column 13, line 10 "fully" should be--full--.
Column 14, line 64 please insert the following omitted paragraph--said storage means comprises a magnetic storage processing unit of a digital computer--.
Column 15 , line 48 "transmitting aid" should be--transmitting said--.
Column 16 , line 20 "accordingly" should be--according--;
  " , line 22 "accordingly" should be--according--;
  " , line 26 "accordingly" should be--according--;
  " , line 29 "accordingly" should be--according--;
  " , line 30 "accordingly" should be--according--;
  " , line 31 "accordingly" should be--according--;
  " , line 35 "accordingly" should be--according--.

Signed and sealed this 20th day of June 1972.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR. ROBERT GOTTSCHALK
Attesting Officer Commissioner of Patents