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(54) **Title:** IMPROVED COMPOUND SEMICONDUCTOR GROWTH USING ION IMPLANTATION

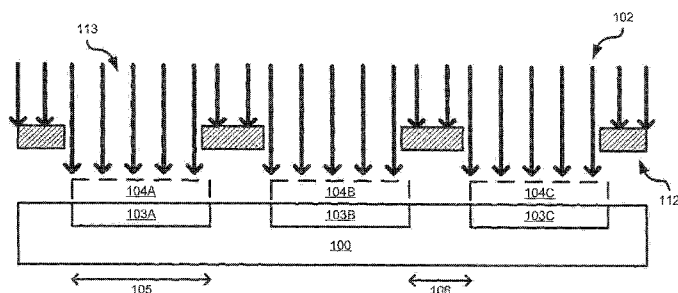


FIG. 4

(57) **Abstract:** A workpiece is implanted to affect growth of a compound semiconductor, such as GaN, implanted regions of a workpiece increase, reduce, or prevent growth of this compound semiconductor. Combinations of implants may be performed to cause increased growth in certain regions of the workpiece, such as between regions where growth is reduced. Growth also may be reduced or prevented at the periphery of the workpiece.

IMPROVED COMPOUND SEMICONDUCTOR GROWTH USING ION IMPLANTATION

FIELD

5 This invention relates to ion implantation and, more particularly, to ion implantation to improve the quality of a layer grown on a workpiece.

BACKGROUND

10 Ion implantation is a standard technique for introducing material into a workpiece. A desired implant material is ionized in an ion source, the ions are accelerated to form an ion beam of prescribed energy, and the ion beam is directed at the surface of the workpiece. The energetic ions in the ion beam penetrate into the bulk of the workpiece material and affect both the surface and depth of the workpiece material under certain conditions.

15 Gallium nitride (GaN) is a material commonly grown on workpieces. GaN is becoming more important for use in light-emitting diodes (LEDs), power transistors, and solid state lasers. The ability to grow high-quality GaN is one limiting factor to improving the quality and lowering the cost of these devices. One method of improving the quality of epitaxially-grown GaN is known as epitaxial layer overgrowth (ELOG). For ELOG, a layer of GaN is grown, hard mask windows of SiO_2 or Si_3N_4 are deposited, and then the high-
20 quality GaN is grown. In some instances, deposition of the hard mask requires removal of the workpiece from the MOCVD tool and then reintroduction of the workpiece to the MOCVD tool after a lithography step, photoresist application, deposition, and photoresist removal. This particular process is cumbersome and costly. Repeated ELOG sequences add even more cost.

25 ELOG of GaN on silicon, sapphire, SiC , AlN , GaN, or other workpieces can be accomplished using implantation instead of SiO_2 or Si_3N_4 deposition. Previously, photoresist was used to mask part of the silicon workpiece and implantation was performed on the unmasked areas. GaN grew laterally over the implanted areas. However, this process is still fairly complex. The use of photoresist adds extra steps, which increases manufacturing costs.
30 What is needed is a faster, less complex, and lower cost method of growing high-quality compound semiconductor layers.

SUMMARY

According to a first aspect of the invention, a method of workpiece processing is provided. The method comprises implanting a first plurality of implanted regions in a
35 workpiece with a first species. A compound semiconductor is grown on the workpiece after the implanting. The compound semiconductor growth is reduced on the first plurality of

implanted regions compared to between the first plurality of implanted regions. At least one device is formed between the first plurality of implanted regions.

According to a second aspect of the invention, a method of workpiece processing is provided. The method comprises implanting a second plurality of regions in a workpiece. A compound semiconductor is grown on the workpiece after the implanting. The compound semiconductor growth is increased on the plurality of implanted regions compared to between the plurality of implanted regions.

According to a third aspect of the invention, a method of workpiece processing is provided. The method comprises implanting a periphery of a workpiece. A compound semiconductor is grown on the workpiece after the implanting. The growth is reduced on the periphery.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present disclosure, reference is made to the accompanying drawings, which are incorporated herein by reference and in which:

FIG. 1 is a cross-sectional side view of a first embodiment of implantation into a workpiece;

FIG. 2 is a cross-sectional side view of a second embodiment of implantation into a workpiece;

FIG. 3 is a cross-sectional side view of a third embodiment of implantation into a workpiece;

FIG. 4 is a cross-sectional side view of a fourth embodiment of implantation into a workpiece;

FIG. 5 is a top perspective view of a fifth embodiment of implantation into a workpiece;

FIG. 6 is a cross-sectional side view of a sixth embodiment of implantation into a workpiece;

FIG. 7 is a top perspective view of a seventh embodiment of an implanted workpiece;

FIG. 8 is a cross-sectional side view of an eighth embodiment of an implanted workpiece;

FIG. 9 is a perspective view of a ninth embodiment of an implanted workpiece;

FIG. 10 is a top perspective view of a tenth embodiment of an implanted workpiece;

FIG. 11 is a block diagram of a plasma processing apparatus having a plasma sheath modifier; and

FIG. 12 is a side view of an embodiment of selective ion implantation.

DETAILED DESCRIPTION

The embodiments are described herein in connection with formation of a compound semiconductor such as GaN, but these embodiments also may be used with other III/V compound semiconductors, II/VI compound semiconductors, or other materials known to a person skilled in the art. While specific types of implanters are disclosed, other ion implantation systems known to those skilled in the art that can focus an ion beam or that can implant particular regions of a workpiece with or without a mask on the workpiece may be used in the embodiments described herein. While LEDs are specifically disclosed, other devices also may benefit from the embodiments described herein. The workpieces herein may be silicon, sapphire, AlN, GaN, other compound semiconductors, or other materials and include a coating or other layers in some instances. Any implant dimensions are exemplary and other dimensions are possible. Thus, the invention is not limited to the specific embodiments described below.

FIG. 1 is a cross-sectional side view of a first embodiment of implantation into a workpiece. In this embodiment, a blanket implant is performed over the entire surface of the workpiece 100 using the ions 102 (illustrated by the arrows). The implanted region 109 is formed in the workpiece 100. The devices 104A-104C, which may be GaN or some other compound semiconductor, are then grown on top of this workpiece 100 after the implantation is completed. The devices 104A-104C are shown with dotted lines in FIG. 1 because these devices 104A-104C were not formed prior to the blanket implant. These devices 104A-104C may have a width 105 of approximately 300 μm in one embodiment, though these devices 104A-104C may be between 100 μm to 3000 μm in dimension. Of course, other dimensions are possible. A distance 106 of approximately 100 μm may separate each pair of devices 104A-104C in one instance. The distance 106 also may be between 10 μm to 300 μm or other distances known to those skilled in the art.

The blanket implant that forms the implanted region 109 improves compound semiconductor growth, such as the growth of GaN. This blanket implant can be combined with a selective or patterned implant, as seen separately in other embodiments herein. The blanket implant and patterned implants can be performed in either order. One possible mechanism that causes the improved growth is that the implant changes the stoichiometry on the surface of the workpiece 100 or relieves the lattice mismatch between the workpiece 100 and the compound semiconductor. Stoichiometry is changed by either adding particular elements through implantation or by preferential sputtering of the elements from the workpiece. For example, preferentially sputtering Al or O in a sapphire workpiece 100, depending on implant species, energy, angle, and dose, may affect the stoichiometry of the workpiece 100. Of course, other mechanisms are possible.

FIG. 2 is a cross-sectional side view of a second embodiment of implantation into a workpiece. In this embodiment, the workpiece 100 is implanted using ions 102 in the implanted regions 103A-103C. Devices 104A-104C are formed on the implanted regions 103A-103C during a later processing step. These devices 104A-104C may have a width 105 of approximately 300 μm and may be separated by a distance 106 of approximately 100 μm , though other dimensions are possible. A plasma processing apparatus having a plasma sheath modifier, such as that illustrated in FIGs. 11-12, or other systems may be used to perform this selective implantation. Thus, parts of the workpiece 100 are not implanted, such as the distance 106 between implanted regions 103A-103C. The implanted regions 103A-103C improve compound semiconductor growth on the workpiece 100 or make the compound semiconductor grow at an increased rate. Some compound semiconductor growth may occur between the implanted regions 103A-103C in one instance, but it may occur at a rate less than the growth on the implanted regions 103A-103C.

FIG. 3 is a cross-sectional side view of a third embodiment of implantation into a workpiece. In this embodiment, only a portion of the areas under the devices 104A-104C are implanted. The ions 102 only implant the implanted regions 110A-110F. Thus, these implanted regions 110A-110F are smaller than a dimension of the devices 104A-104C. For example, the implanted regions 110A-110F may have a width 111 of approximately 20 μm while the devices 104A-104C may have a width 105 of approximately 300 μm , though other dimensions are possible. Again, a plasma processing apparatus having a plasma sheath modifier, such as that illustrated in FIGs. 11-12, or other systems may be used to perform this selective implantation. Such a selective implantation may improve ELOG and the subsequently-grown compound semiconductor may be of higher quality. This also may enable ELOG within a single device. The implanted regions 110A-110C can improve, reduce, or prevent compound semiconductor growth on the workpiece 100. Thus, the compound semiconductor growth may be at a slower rate over the implanted regions 110A-110C in one instance.

One possible mechanism that reduces or prevents compound semiconductor growth is that the compound semiconductor will preferentially deposit on a crystalline portion of the workpiece 100 compared to an amorphous portion of the workpiece 100. An implant may cause amorphization of the workpiece 100. Another possible mechanism that reduces or prevents compound semiconductor growth relates to using a species that interferes with the nucleation of the compound semiconductor. F, Cl, C, or metals may have this effect. Of course, other mechanisms are possible.

FIG. 4 is a cross-sectional side view of a fourth embodiment of implantation into a workpiece. In this embodiment, a blanket implant of the entire workpiece 100 is performed,

but a proximity mask 112 positioned above or a distance from the workpiece 100 is used to block a portion of the ions 102. Thus, the apertures 113 in the proximity mask 112 correspond with the desired implanted regions 103A-103C. The devices 104A-104C may have a width 105 of approximately 300 μm and may be separated by a distance 106 of approximately 100 μm , though other dimensions are possible. The distance 106 may not correspond exactly with the dimensions of the proximity mask 112 and the width 105 may not correspond exactly with the dimensions of the aperture 113 due to the angles of the ions 102. The implanted regions 103A-103C may correspond with the location of the devices 104A-104C that are formed during later processing steps. A beamline ion implanter, plasma doping implanter, or other plasma system may be used with the proximity mask 112.

FIG. 5 is a cross-sectional side view of a fifth embodiment of implantation into a workpiece. In this embodiment, the apertures 113 in the proximity mask 112 are configured such that the ions 102 implant only a portion of the areas under the devices 104A-104C during the blanket implant of the workpiece 100. Thus, these implanted regions 110A-110F are smaller than a dimension of the devices 104A-104C. For example, the implanted regions 110A-110F may have a width 111 of approximately 20 μm while the devices 104A-104C may have a width 105 of approximately 300 μm , though other dimensions are possible. The width 111 may not correspond exactly with the dimensions of the aperture 113 due to the angles of the ions 102. A beamline ion implanter, plasma doping implanter, or other plasma system may be used with the proximity mask.

FIG. 6 is a cross-sectional side view of a sixth embodiment of implantation into a workpiece. In this embodiment, the regions between the devices 104A-104C are implanted. Thus, the ions 102 form the implanted regions 114A-114D. These implanted regions 114A-114D may prevent or reduce GaN growth between the devices 104A-104C during formation of these devices 104A-104C. While a patterned implant of the ions 102 is illustrated, a proximity mask also may be used. This may be combined with a blanket implant (to increase or reduce GaN growth) or other embodiments disclosed herein. In one embodiment, the compound semiconductor is grown on the surface of the workpiece 100, but this growth may be at a reduced rate over the implanted regions 114A-114D compared to between the implanted regions 114A-114D. In another embodiment, compound semiconductor growth over the implanted regions 114A-114D is prevented but growth between the implanted regions 114A-114D still occurs.

FIG. 7 is a top perspective view of a seventh embodiment of an implanted workpiece. In this particular embodiment, multiple implant steps are performed. First, a series of lines are implanted in the workpiece to form the implanted regions 115A-115D, which may be similar to the implant illustrated in FIG. 6 that forms the implanted regions 114A-114D. The

workpiece 100 is then rotated, for example, 90° and a second series of lines are implanted in the workpiece 100 to form the implanted regions 116A-116D (which are shaded in FIG. 7). Of course, other rotation amounts, such as 60°, are possible. These implanted regions 115A-115D and implanted regions 116A-116D overlap. “Islands” or “blocks” (represented by the spaces 117) that may not be implanted are surrounded by implanted “streets” (represented by the implanted regions 115A-115D and implanted regions 116A-116D). The implanted regions 115A-115D and implanted regions 116A-116D may prevent or reduce growth of the compound semiconductor. During compound semiconductor growth, the crystal regions will meet within such a region 117, as represented by the X within each region 117. While the X is illustrated, there may be variation due to non-uniform deposition and the actual pattern of the crystal regions may vary. The defects are reduced and localized in the compound semiconductor, which leads to a higher quality layer of a compound semiconductor, such as GaN. The spaces 117 may have a dimension 119 of approximately 100 to 500 μm. The implanted regions 115A-115D or implanted regions 116A-116D may have a width 118 of approximately 10 to 100 μm. Of course, other dimensions are possible.

In one particular embodiment, the whole surface of the workpiece 100 is implanted. The implanted regions 115A-115D and implanted regions 116A-116D may be implanted with, for example, Ar and the spaces 117 may be implanted with, for example, N. Other embodiments or combination of species is possible. This may be performed using either two or more patterned implants or using a blanket implant (as illustrated in FIG. 1) to implant the spaces 117 with one or more patterned implant to form the implanted regions 115A-115D and implanted regions 116A-116D. For example, a blanket N implant can be combined with two patterned Ar implants to form the structure shown in FIG. 7. The workpiece 100 is rotated between these two Ar implants.

The quality and growth rate of epitaxially-grown GaN on sapphire can be controlled by selection of the implant species. For example, N, Al, or O enhance GaN growth on sapphire while Ar prevents or reduces GaN growth on sapphire. Implanting Al, N, or O can change the stoichiometry on the surface of the sapphire workpiece. For example, if GaN is grown on a sapphire workpiece, the N implant will add N to the sapphire workpiece surface. AlN may have a better match to GaN than sapphire in terms of lattice constant or size. Implanting Ar may change the stoichiometry by preferential sputtering of Al over the O on the sapphire surface, for example. High doses of some species, such as doses above $1 \times 10^{17} \text{ cm}^{-2}$ may prevent or reduce compound semiconductor growth if amorphization occurs on the workpiece. Smaller ions, such as H or He, also may prevent or reduce compound semiconductor growth if amorphization occurs. A dose smaller than $1 \times 10^{17} \text{ cm}^{-2}$ may be used

to amorphize a workpiece and prevent or reduce compound semiconductor growth with other noble gases larger than Ar.

In one instance, two sapphire workpieces were implanted at 40 keV and $1\text{E}17\text{cm}^{-2}$ using Ar and N, respectively. GaN successively grew on the N-implanted workpiece, while Ar caused pitting in the GaN growth. The dose of either N or Ar may be optimized for improved GaN growth or reduction in growth. For example, an N dose below approximately $1\text{E}17\text{cm}^{-2}$ may improve GaN growth. Of course, other species besides N or Ar may be used. P, As, or other species also may enhance GaN growth. Other noble gases, H, O, Al, C, or other species also may prevent or reduce GaN growth. For silicon workpieces, noble gases such as Ar, Xe, and Kr may prevent growth of GaN. O or N may form SiO_2 or SiN regions in a silicon workpiece during an anneal, which also may prevent growth of GaN. These species also may have similar effects on other workpiece materials or with other compound semiconductors.

Compound semiconductor growth, such as GaN growth, on a silicon workpiece also may be enhanced by implanting C or Ge. This may form SiC or SiGe during an anneal. These SiC or SiGe regions modify the lattice parameter of the silicon and may allow better lattice matching to the GaN.

Effects on the surface of the workpiece also may enhance, reduce, or prevent growth of a compound semiconductor. For example, a 0.5 keV Ar implant into a silicon workpiece with a dose of $5\text{E}16\text{cm}^{-2}$ has been shown to sputter approximately 100 nm away from the workpiece. Thus, this is further increased when using a focused beam because the sputter yield may increase as the angle of incidence of the ions increases toward 60 degrees. This may produce a textured workpiece. Besides the chemical effects from the ion implantation, this surface topography modification also may affect the growth of the compound semiconductor. In one instance, the textured surface caused by sputtering will enhance compound semiconductor growth on the workpiece.

FIG. 8 is a cross-sectional side view of an eighth embodiment of an implanted workpiece. The workpiece 100, which also may include a blanket buffer layer (not illustrated), is implanted using a proximity mask or patterned implant as previously described. The implanted regions 114A-114C and implanted regions 110A-110D are designed to reduce or prevent GaN growth. These implanted regions 114A-114C and implanted regions 110A-110D may be implanted with Ar. A compound semiconductor, such as GaN, is grown between these implanted areas to form devices 104A and 104B, which may be LEDs. Defect lines or voids 120 form above the implanted regions 110A-110D. These may encourage ELOG to occur within the individual devices 104A and 104B. Selective area growth (SAG) may occur between the devices 104A and 104B.

FIG. 9 is a perspective view of a ninth embodiment of an implanted workpiece. This embodiment may correspond to the embodiment illustrated in FIG. 8. The workpiece 100 is implanted. The implanted regions 114, of which only one is pointed out in FIG. 9, separate multiple spaces 117. The compound semiconductor preferentially grows in the spaces 117 between the implanted regions 114 because the implanted regions 114 are configured to reduce or prevent growth of a compound semiconductor. At least one space 117 has at least one implanted regions 110, of which only one is pointed out in FIG. 9. The implanted regions 114 and 110 are configured to reduce or prevent growth of GaN. The spaces 117 may be implanted in one instance to improve growth of GaN. Of course, other implant patterns are possible from that illustrated in FIG. 9.

FIG. 10 is a top perspective view of a tenth embodiment of an implanted workpiece. The periphery 121 (shaded in FIG. 10) of the workpiece 100 is implanted to reduce or prevent compound semiconductor growth. During a growth process, GaN or another compound semiconductor may grow thicker or at a faster rate at this periphery 121 than in the center 122. The lattice constant of, for example, GaN may be smaller than that of the sapphire or silicon in a workpiece 100. Thus, the GaN deposits under significant strain at the center 122 of the workpiece 100. At the periphery 121 of the workpiece 100, the GaN deposits more freely or is less constrained and forms an initial layer more quickly. Once the GaN is deposited, additional Ga and N atoms deposit more freely on the GaN at the periphery 121 of the workpiece 100 than filling the center 122 of the workpiece 100. This forms a thicker outer layer of GaN on the workpiece 100. This effect may disappear when a sufficiently thick layer of GaN, such as greater than approximately 100 nm, is formed on the entire surface of the workpiece 100, but the workpiece 100 may still have an uneven layer of GaN due to the initial GaN growth at the periphery 121.

The resulting thicker GaN at the periphery 121 may lead to cracking because of the increased stresses caused by the difference in thickness. The implant at the periphery 121 is configured to reduce compound semiconductor growth so that this compound semiconductor growth is equal on both the periphery 121 and center 122. This results in a workpiece 100 having a compound semiconductor layer with an approximately equal or uniform thickness. Or, alternatively, the implant at the periphery 121 is configured to totally prevent compound semiconductor growth on the periphery 121. In one particular embodiment, the workpiece 100 is rotated 360° under a fixed ion beam that has a width of the implanted area at the periphery 121. In one instance, the periphery 121 that is implanted has a width of approximate 5 mm, though other dimensions are possible. This implant into the periphery 121 may be combined with other implants, such as the resulting implanted workpiece 100 of FIG. 9.

In one particular embodiment, the workpieces may have a blanket implant performed across the entire surface of the workpiece prior to the patterned implant. This may be have a different dose, energy, or species from a patterned implant. The blanket implant may improve compound semiconductor growth.

5 In an alternate embodiment, the compound semiconductor may be grown in a plasma cluster tool. This may be the same tool where the implants were performed or it may be operatively linked to the tool where the implants were performed. Vacuum may not be broken around the workpiece if the tools are operatively linked, which reduces oxide layers, contamination of workpieces, and increases throughput. Ion beam assisted deposition (IBAD)
10 also may assist in GaN growth.

FIG. 11 is a block diagram of a plasma processing apparatus having a plasma sheath modifier. The plasma 140 is generated as is known in the art. This plasma 140 is generally a quasi-neutral collection of ions and electrons. The ions typically have a positive charge while the electrons have a negative charge. The plasma 140 may have an electric field of, for
15 example, approximately 0 V/cm in the bulk of the plasma 140. In a system containing the plasma 140, ions 102 from the plasma 140 are attracted toward a workpiece 100. These ions 102 may be attracted with sufficient energy to be implanted into the workpiece 100. The plasma 140 is bounded by a region proximate the workpiece 100 referred to as a plasma sheath 242. The plasma sheath 242 is a region that has fewer electrons than the plasma 140.
20 Hence, the differences between the negative and positive charges cause a sheath potential in the plasma sheath 242. The light emission from this plasma sheath 242 is less intense than the plasma 140 because fewer electrons are present and, hence, few excitation-relaxation collisions occur. Thus, the plasma sheath 242 is sometimes referred to as "dark space."

The plasma sheath modifier 101 is configured to modify an electric field within the
25 plasma sheath 242 to control a shape of a boundary 241 between the plasma 140 and the plasma sheath 242. Accordingly, ions 102 that are attracted from the plasma 140 across the plasma sheath 242 may strike the workpiece 100 at a large range of incident angles. This plasma sheath modifier 101 may be referred to as, for example, a focusing plate or sheath engineering plate.

30 In the embodiment of FIG. 11, the plasma sheath modifier 101 includes a pair of panels 212 and 214 defining an aperture there between having a horizontal spacing (G). The panels 212 and 214 may be an insulator, semiconductor, or conductor. In other embodiments, the plasma sheath modifier 101 may include only one panel or more than two panels. The panels 212 and 214 may be a pair of sheets having a thin, flat shape. In other embodiments,
35 the panels 212 and 214 may be other shapes such as tube-shaped, wedge-shaped, and/or have a beveled edge proximate the aperture. The panels 212 and 214 also may be positioned a

vertical spacing (Z) above the plane 151 defined by the front surface of the workpiece 100. In one embodiment, the vertical spacing (Z) may be about 1.0 to 10.0 mm.

Ions 102 may be attracted from the plasma 140 across the plasma sheath 242 by different mechanisms. In one instance, the workpiece 100 is biased to attract ions 102 from the plasma 140 across the plasma sheath 242. In another instance, a plasma source that generates the plasma 140 and walls surrounding the plasma 140 are biased positively and the workpiece 100 may be grounded. The biasing may be pulsed in one particular embodiment. In yet another instance, electric or magnetic fields are used to attract ions 102 from the plasma 140 toward the workpiece 100.

Advantageously, the plasma sheath modifier 101 modifies the electric field within the plasma sheath 242 to control a shape of the boundary 241 between the plasma 140 and the plasma sheath 242. The boundary 241 between the plasma 140 and the plasma sheath 242 may have a convex shape relative to the plane 151 in one instance. When the workpiece 100 is biased, for example, the ions 102 are attracted across the plasma sheath 242 through the aperture between the panels 212 and 214 at a large range of incident angles. For instance, ions 102 following trajectory path 271 may strike the workpiece 100 at an angle of $+\theta^\circ$ relative to the plane 151. Ions 102 following trajectory path 270 may strike the workpiece 100 at about an angle of 0° relative to the same plane 151. Ions 102 following trajectory path 269 may strike the workpiece 100 an angle of $-\theta^\circ$ relative to the plane 151. Accordingly, the range of incident angles may be between $+\theta^\circ$ and $-\theta^\circ$ centered about 0° . In addition, some ion trajectories paths such as paths 269 and 271 may cross each other. Depending on a number of factors including, but not limited to, the horizontal spacing (G) between the panels 212 and 214, the vertical spacing (Z) of the panels 212 and 214 above the plane 151, the dielectric constant of the panels 212 and 214, or other process parameters of the plasma 140, the range of incident angles (θ) may be between $+60^\circ$ and -60° centered about 0° .

FIG. 12 is a side view of an embodiment of selective ion implantation. Implanted regions 103 are formed in the workpiece 100 using the ions 102. The workpiece 100 is scanned with respect to the plasma sheath modifier 101 or ions 102, as illustrated by the arrow 108. This may involve moving the plasma sheath modifier 101, workpiece 100, or both. The scanning may be in one dimension or two dimensions. In one particular embodiment, the workpiece 100 is biased when the ions 102 implant the implanted regions 103. The bias scheme is adjusted to produce the desired pattern of implanted regions 103. Thus, the workpiece 100 is not biased when the ions 102 would implant between the implanted regions 103. This eliminates or reduces ions 102 from impacting between the implanted regions 103. In this manner, the implanted regions 103 may be formed without a mask or photoresist layer

on the workpiece 100. Alignment, lithography, or photoresist removal steps may be eliminated.

The location of the implanted regions 103 may be carefully controlled because spacing of the implanted regions 103 may affect growth of the GaN or another compound semiconductor during ELOG. This spacing may be optimized for the improved compound semiconductor growth.

The dose rate and focus of the ions 102 can be varied to form the implanted regions 103. If the workpiece 100 is scanned, then the ions 102 may be switched on and off to form the implanted regions 103, the dose of the ion 102 may be adjusted to reduce implantation between the implanted regions 103, or the ions 102 may be focused when implanting the implanted regions 103. If the ions 102 are focused when implanting the implanted regions 103, the ions 102 may be less focused over other parts of the workpiece 100, which reduces implantation between the implanted regions 103.

The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. These other embodiments and modifications are intended to fall within the scope of the present disclosure. Furthermore, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

What is claimed is:

1. A method of workpiece processing comprising:
implanting a first plurality of implanted regions in a workpiece with a first species;
5 and
growing a compound semiconductor on said workpiece after said implanting,
wherein said compound semiconductor growth is reduced on said first plurality of
implanted regions compared to between said first plurality of implanted regions,
wherein at least one device is formed between said first plurality of implanted
10 regions.
2. The method of claim 1, wherein said first plurality of implanted regions form a grid
and said compound semiconductor grows preferentially in spaces between said first
plurality of implanted regions.
3. The method of claim 1, further comprising implanting a second plurality of
15 implanted regions in said workpiece, wherein each of said second plurality of
implanted regions is between said first plurality of implanted regions.
4. The method of claim 1, further comprising implanting a periphery of said
workpiece, wherein said growing is reduced on said periphery.
5. The method of claim 4, wherein said growing is reduced to zero on said periphery.
- 20 6. A method of workpiece processing comprising:
implanting a plurality of implanted regions in a workpiece; and
growing a compound semiconductor on said workpiece after said implanting,
wherein said compound semiconductor growth is increased on said plurality of
implanted regions compared to between said plurality of implanted regions.
- 25 7. The method of claim 6, wherein further comprising implanting a second plurality of
implanted regions in said workpiece, wherein each of said plurality of implanted
regions is between said second plurality of implanted regions.
8. The method of claim 7, wherein said second plurality of implanted regions form a
grid and said compound semiconductor grows preferentially on said plurality of
30 implanted regions between said second plurality of implanted regions.
9. The method of claim 6, further comprising implanting a periphery of said
workpiece, wherein said growing is reduced on said periphery.
10. The method of claim 9, wherein said growing is reduced to zero on said periphery.
11. The method of claim 6, wherein said implanting textures a surface of said
35 workpiece on said plurality of implanted regions.

12. A method of workpiece processing comprising:
implanting a periphery of a workpiece; and
growing a compound semiconductor on said workpiece after said implanting,
wherein said growing is reduced on said periphery.
- 5 13. The method of claim 12, wherein said growing is reduced to zero on said periphery.
14. The method of claim 12, wherein said growing on said periphery is reduced to be
approximately equal to growing at a center of said workpiece whereby a thickness
of said compound semiconductor is approximately equal across said workpiece.
- 10 15. The method of claim 12, wherein said implanting comprises rotating said
workpiece with respect to an ion beam during said implanting, whereby said ion
beam only implants said periphery.
16. The method of claim 12, wherein further comprising implanting a first plurality of
regions in said workpiece, wherein said compound semiconductor growth is
reduced on said first plurality of implanted regions compared to between said first
15 plurality of implanted regions.
17. The method of claim 16, wherein said first plurality of regions form a grid and said
compound semiconductor grows preferentially in spaces between said first plurality
of regions.
- 20 18. The method of claim 16, further comprising implanting a second plurality of
regions in said workpiece, wherein each of said second plurality of regions is
between said first plurality of regions.

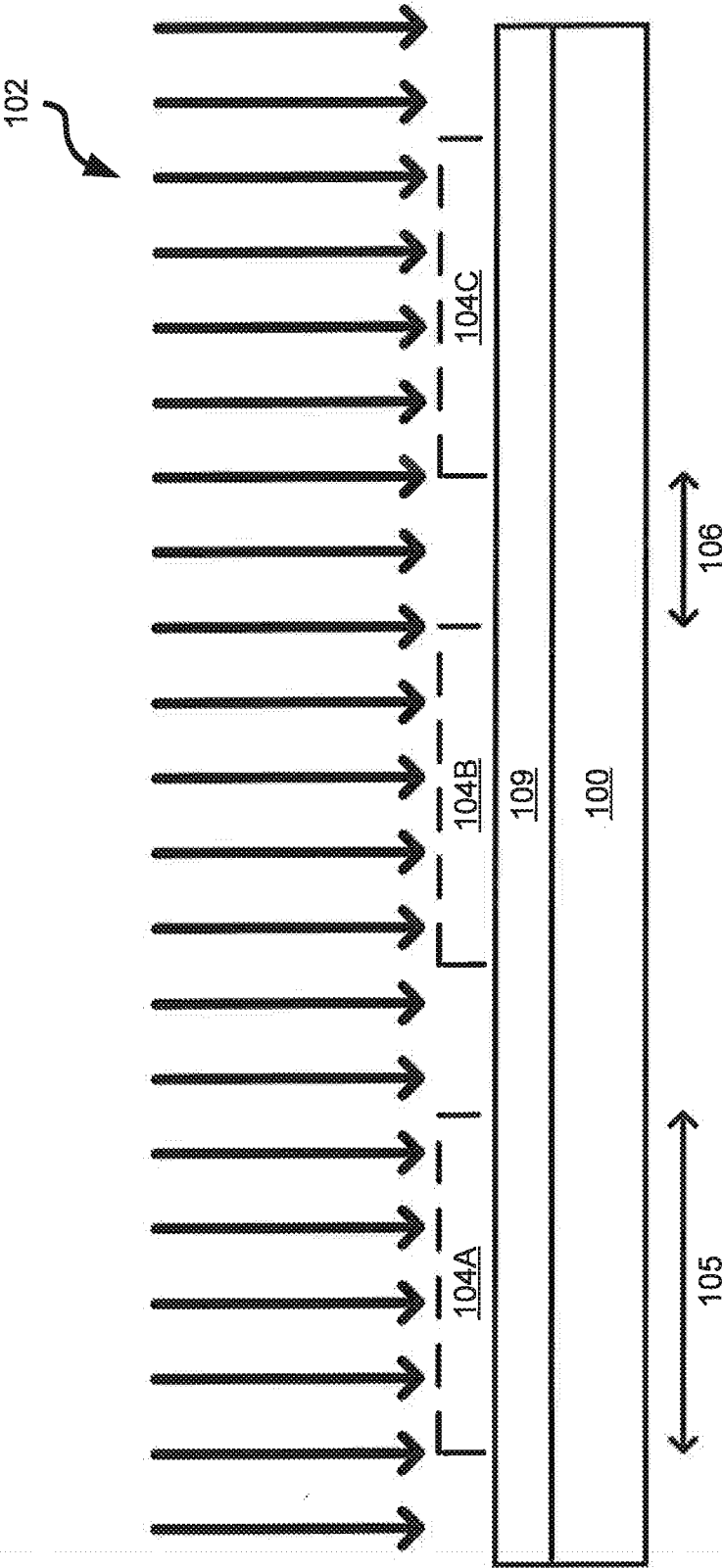


FIG. 1

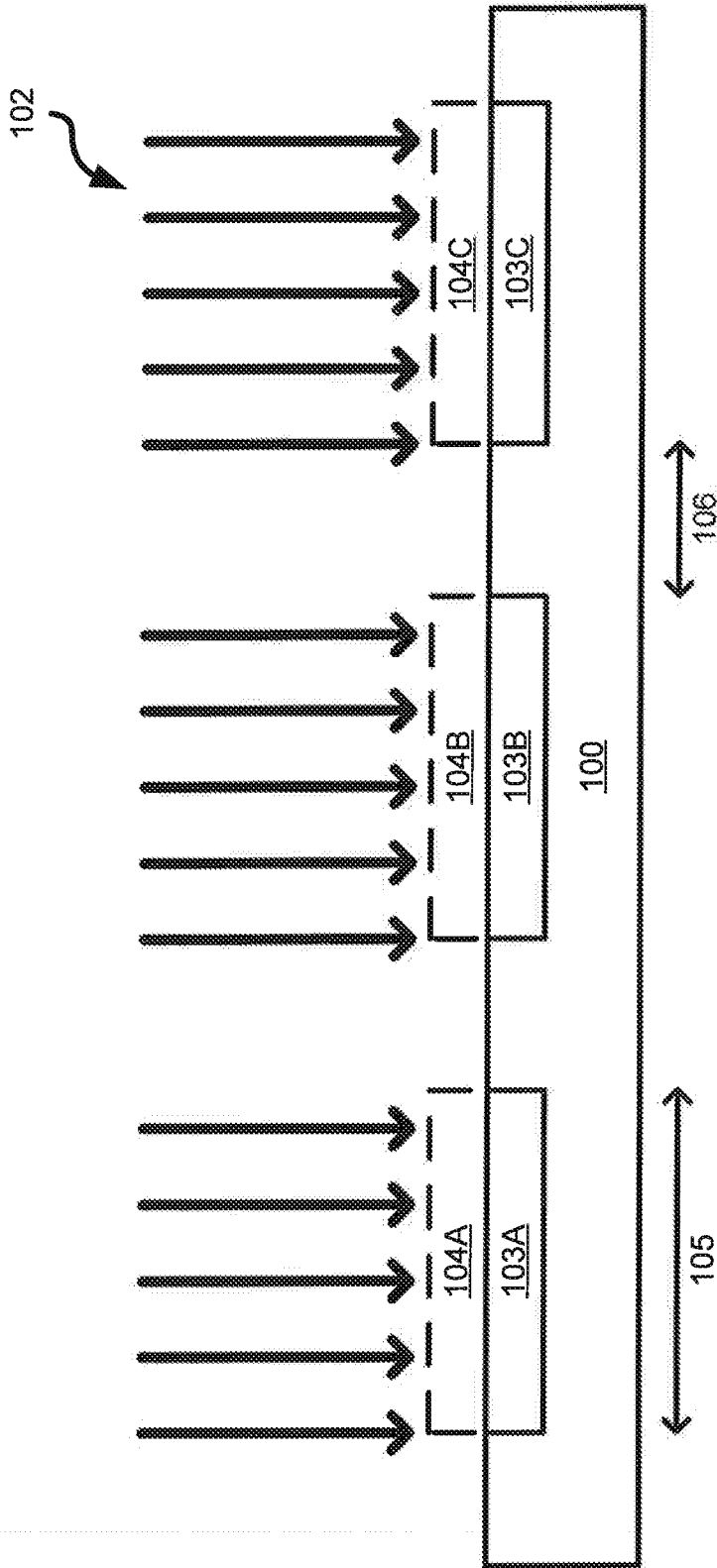


FIG. 2

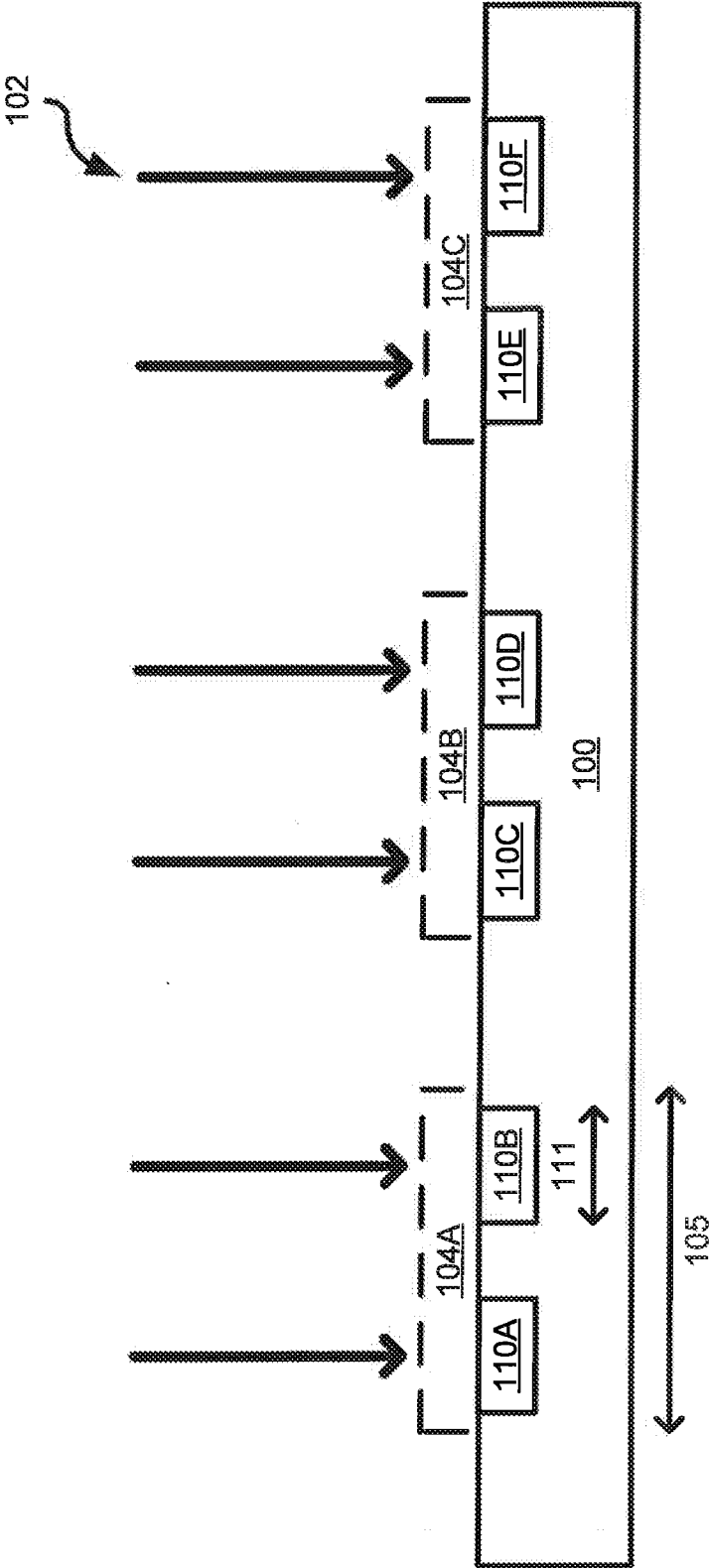


FIG. 3

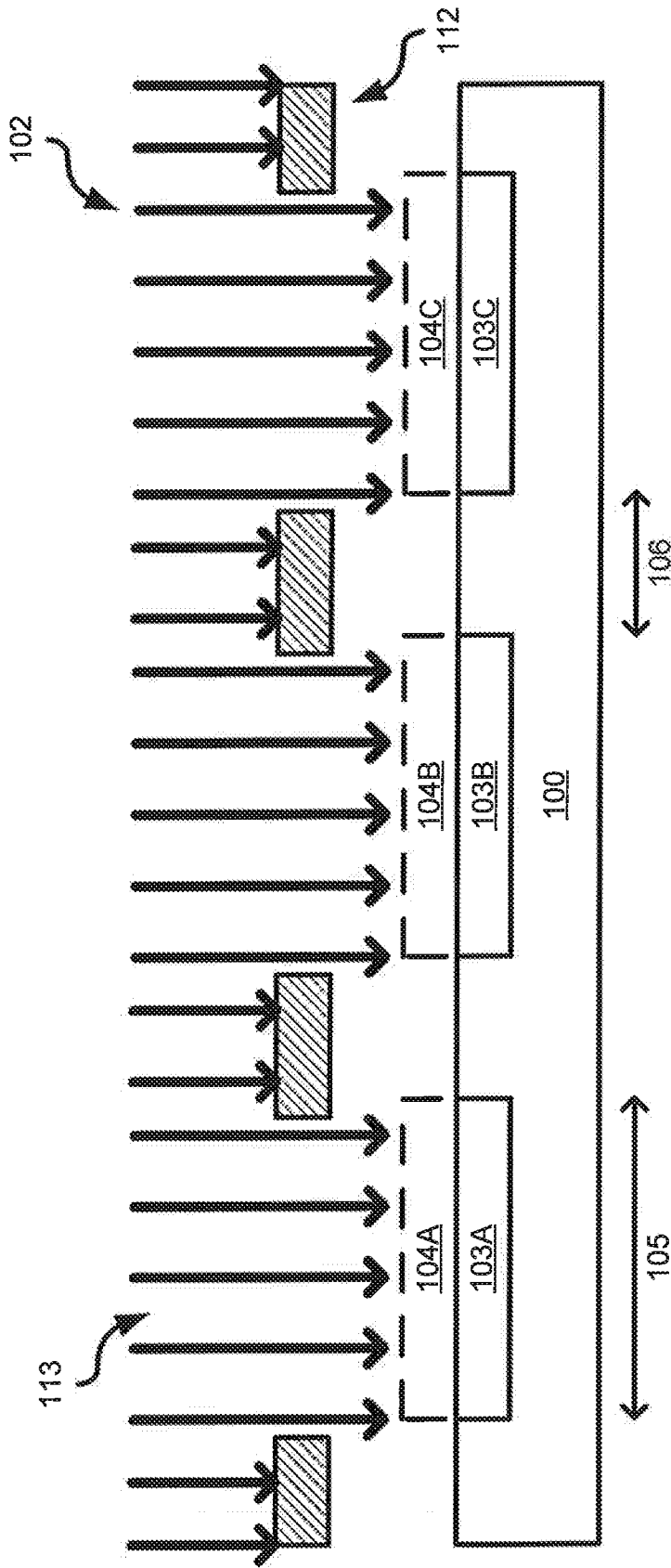


FIG. 4

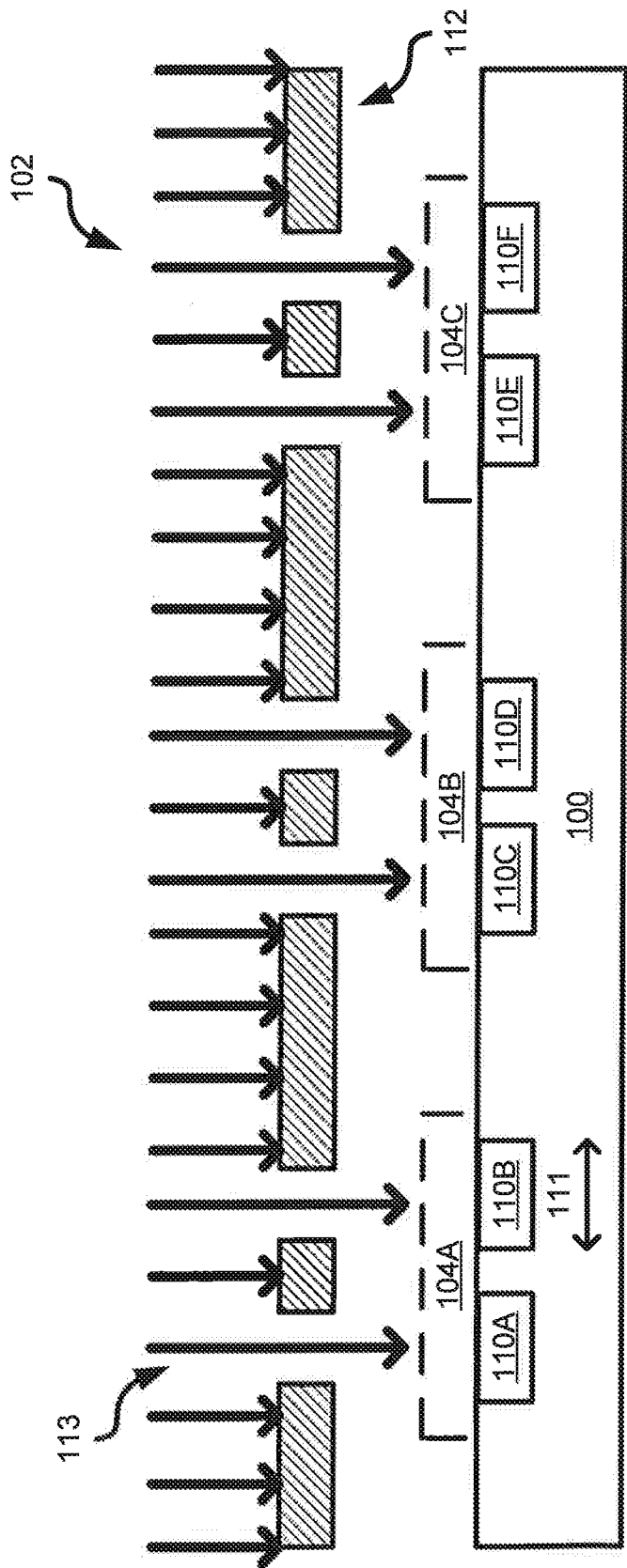


FIG. 5

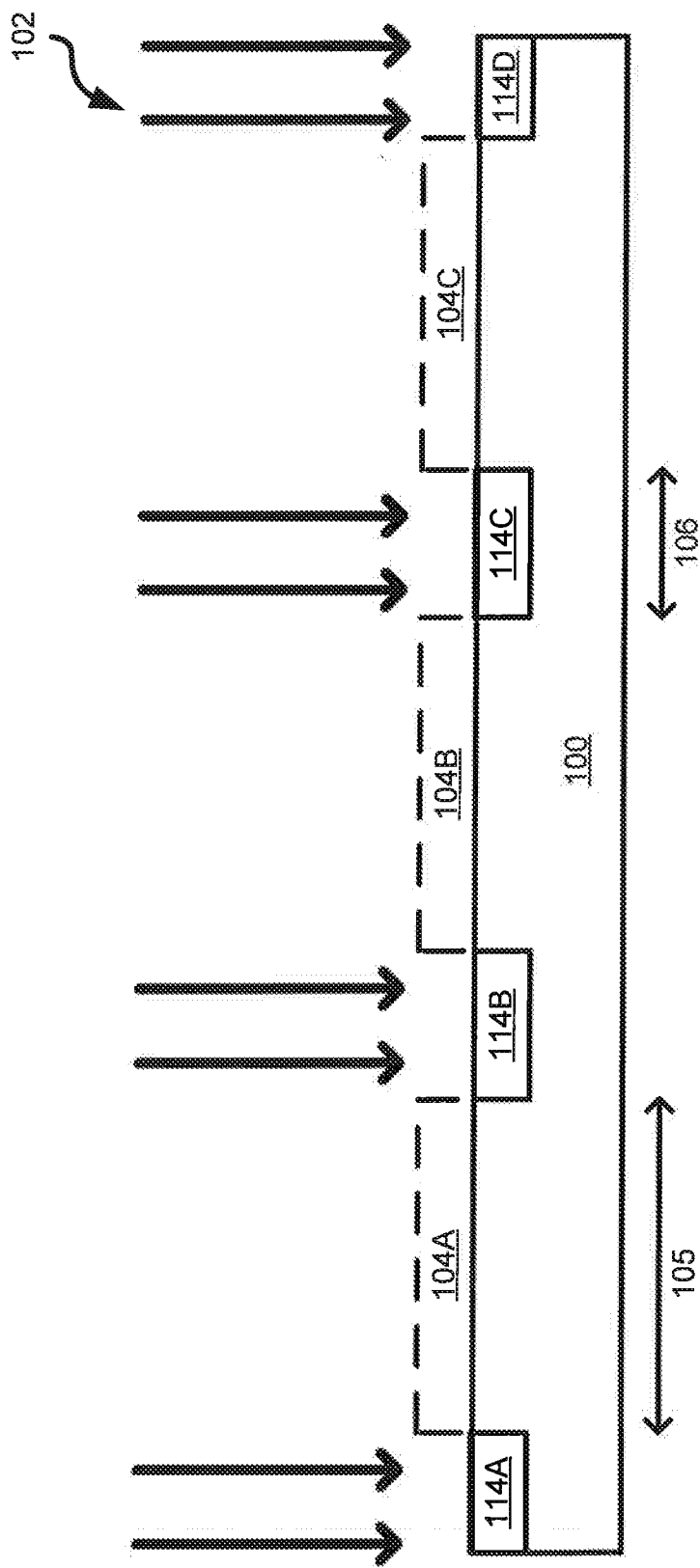


FIG. 6

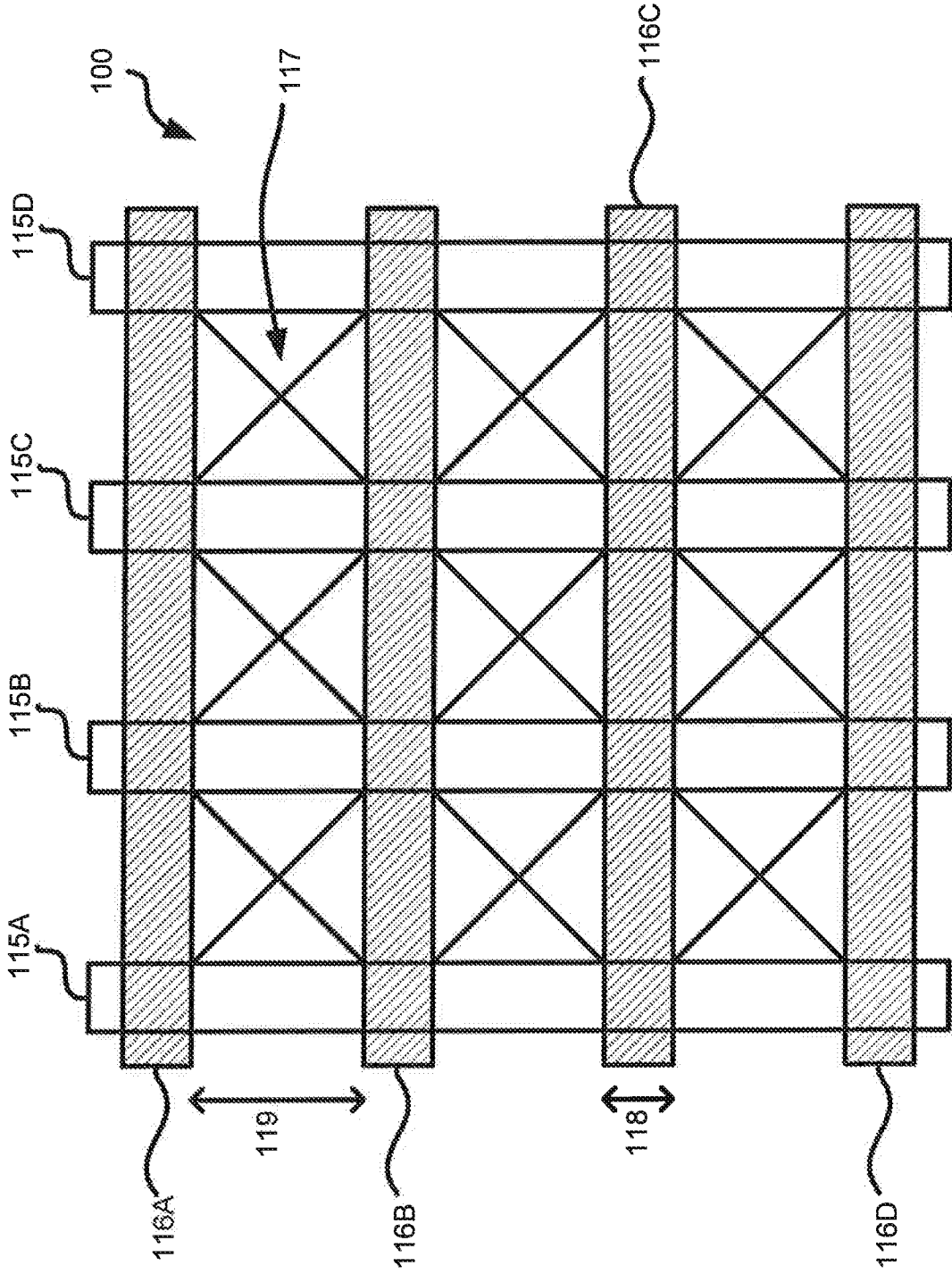


FIG. 7

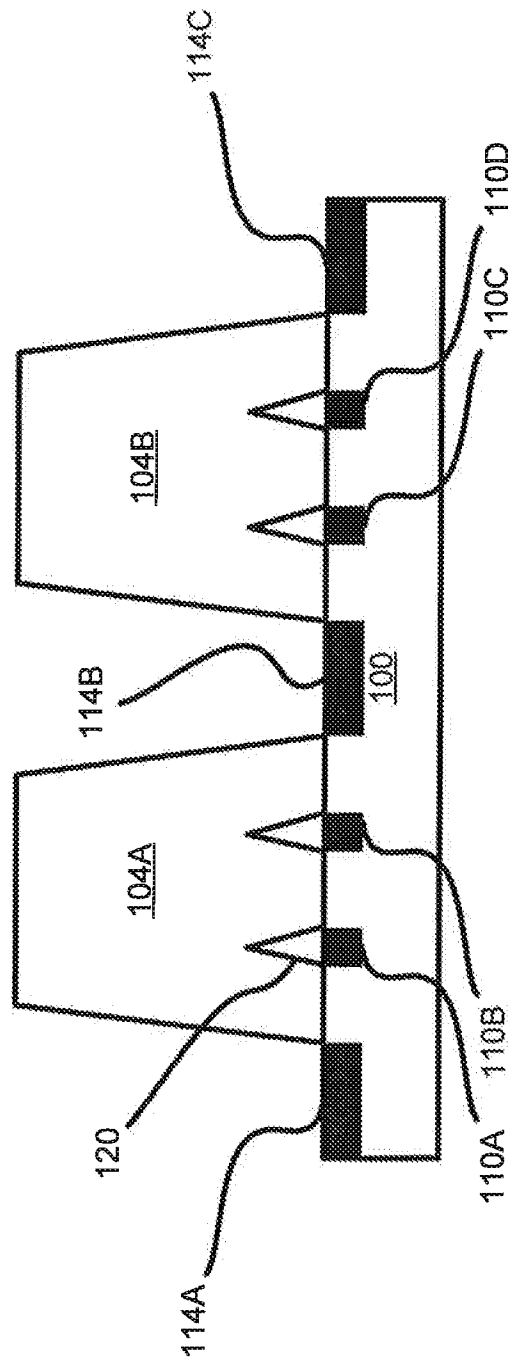


FIG. 8

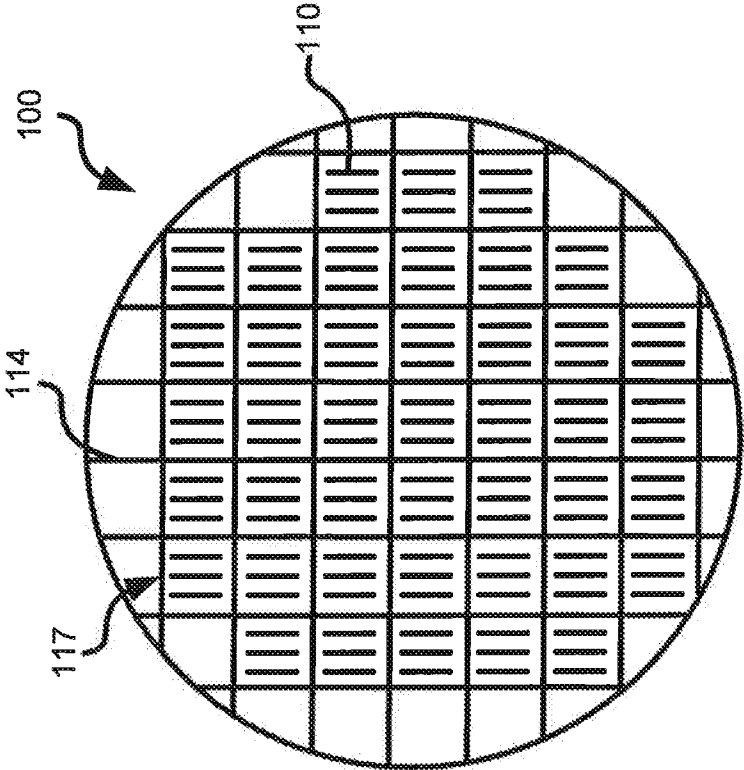


FIG. 9

10/12

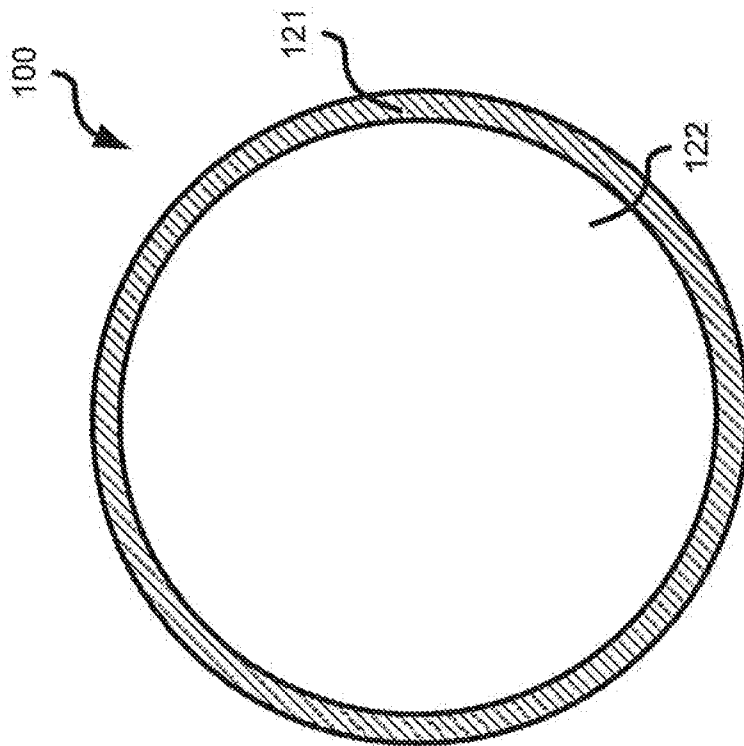
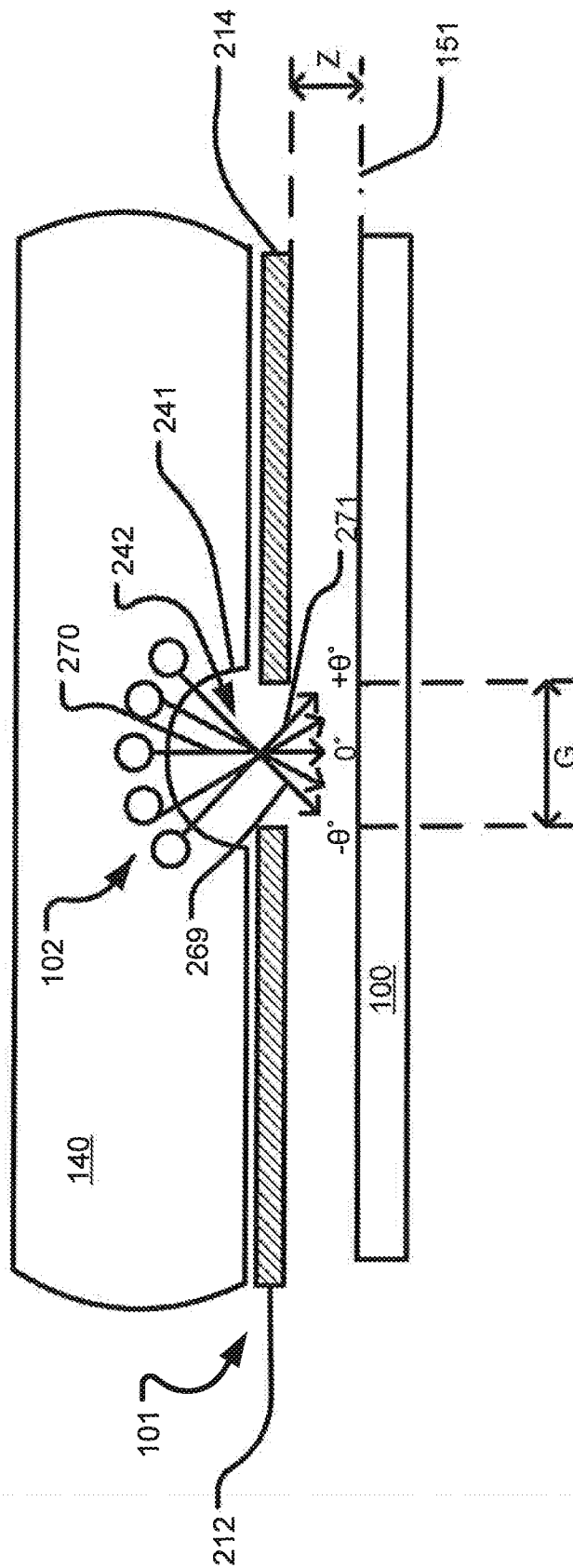


FIG. 10





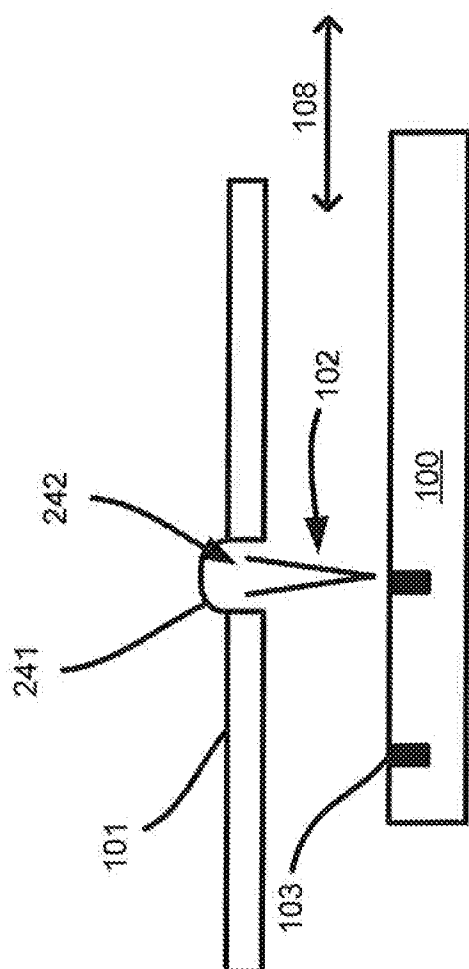


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2012/037811

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/02 H01L21/265
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BUMJOON KIM ET AL: "Epitaxial Lateral Overgrowth of GaN on Si (111) Substrates Using High-dose, N<+> Ion Implantation", CHEMICAL VAPOR DEPOSITION, WILEY-VCH VERLAG, WEINHEIM, DE, vol. 16, no. 1-3, 1 January 2010 (2010-01-01), pages 80-84, XP002678344, ISSN: 0948-1907, DOI: DOI:10.1002/CVDE.200906807 *Sections "Introduction"; "Results and discussion", "4. Experimental" *	1-11
A	US 2010/323508 A1 (ADIBI BABAK [US] ET AL) 23 December 2010 (2010-12-23) the whole document	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

2 July 2012

Date of mailing of the international search report

28/09/2012

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Norga, Gerd

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/037811

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-11

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-11

A method of workpiece processing comprising:
implanting a first plurality of implanted regions in a workpiece with a first species; and growing a compound semiconductor on said workpiece after said implanting, wherein said compound semiconductor growth is reduced or increased on said first plurality of implanted regions compared to between said first plurality of implanted regions

2. claims: 12-18

A method of workpiece processing comprising:
implanting a periphery of a workpiece; and growing a compound semiconductor on said workpiece after said implanting, wherein said growing is reduced on said periphery.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/037811

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010323508 A1	23-12-2010	EP 2446458 A1	02-05-2012
		EP 2489757 A2	22-08-2012
		KR 20120034664 A	12-04-2012
		SG 176547 A1	30-01-2012
		US 2010323508 A1	23-12-2010
		US 2012125259 A1	24-05-2012
		US 2012129325 A1	24-05-2012
		WO 2011005582 A1	13-01-2011
